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SILICON LABORATORIES

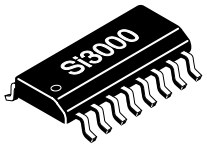
Si3000

VOICEBAND CODEC WITH MICROPHONE/SPEAKER DRIVE

Features

Complete voice codec solution includes the following:

- 84 dB ADC Dynamic Range
- 84 dB DAC Dynamic Range
- 4–12 kHz Sample Rates
- 30 dB Microphone Pre-Amp
- Programmable Input Gain/ Attenuation: –36 dB to 12 dB
- Programmable Output Gain/ Attenuation: –36 dB to 12 dB
- Support for 32 Ω Headphones
- 3:1 Analog Input Mixer
- 3.3–5.0 V Power Supply
- Direct Interface to DSPs
- Direct Connection to Si3034, Si3035, and Si3044 ISOcap™ DAA
- Low profile 16 Pin SOIC Package



Ordering Information:

See page 30.

Applications

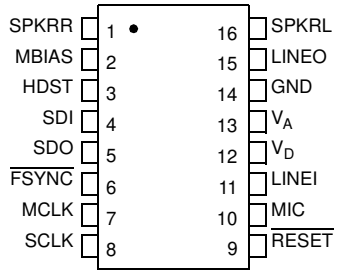
- Modem Voice Channel (DSVD)
- Telephony
- Speech Processing
- General Purpose Analog I/O

Description

The Si3000 is a complete voice band audio codec solution that offers high integration by incorporating programmable input and output gain/ attenuation, a microphone bias circuit, handset hybrid circuit, and an output drive for 32 Ω headphones. The Si3000 can be connected directly to the Si3034, Si3035, and Si3044 ISOcap North American and international DAA chipsets through its daisy-chaining serial interface. The device operates from a single 3.3 to 5 V power supply and is available in a 16-pin small outline package (SOIC).

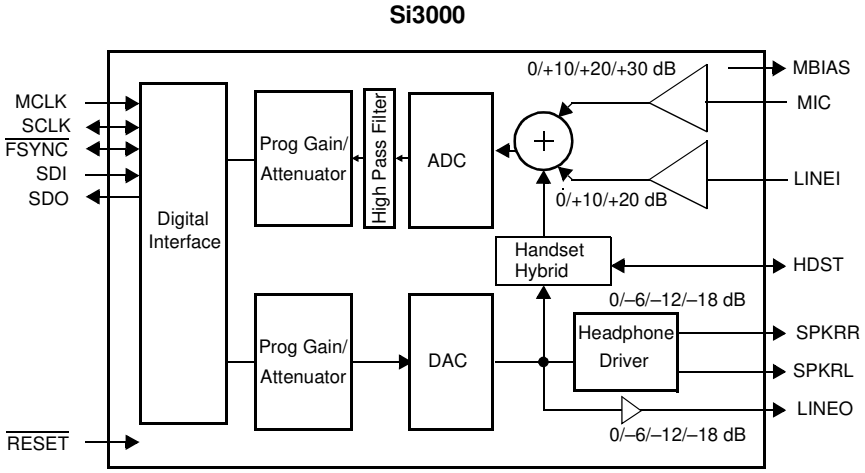
Pin Assignments

Si3000



Functional Block Diagram

Si3000



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Section **Page**

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A	K-grade	0	25	70	°C
Si3000 Supply Voltage, Analog[2]	V_A		3.0	3.3/5.0	5.25	V
Si3000 Supply Voltage, Digital[2,3]	V_D		3.0	3.3/5.0	5.25	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
2. The digital supply, V_D, and analog supply, V_A, can operate from either 3.3 V or 5.0 V. The Si3000 supports interface to 3.3 V logic when operating from 3.3 V. V_D must be within 0.6 V of V_A.
3. The Si3000 specifications are guaranteed using the typical application circuit (including component tolerance) of Figure 13.

Table 2. DC Characteristics, V_A/V_D = 5 V

(V_A = 5 V ±5%, V_D = 5 V ±5%, T_A = 0 to 70°C for K-grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		3.5	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	3.5	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog[1]	I_A	V_A pin	—	6.5	10	mA
Power Supply Current, Digital[2]	I_D	V_D pin	—	10	15	mA
Total Supply Current, Sleep Mode[3]			—	—	1.5	mA

Notes:
1. No loads at DAC outputs, no load at MBIAS, Fs=12.5 kHz.
2. Slave mode operation, Fs = 12.5 kHz.
3. All inputs, except MCLK, are held static, and all outputs are unloaded.

Table 3. DC Characteristics, V_A/V_D = 3.3 V

(V_A = 3.3 V ±10%, V_D = 3.3 V ±10%, T_A = 0°C to 70°C for K-grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.4	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog	I_A	V_A pin	—	6	10	mA
Power Supply Current, Digital[2]	I_D	V_D pin	—	6	10	mA
Total Supply Current, Sleep Mode[3]			—	—	1.5	mA

Notes:
1. No loads at DAC outputs, no load at MBIAS, Fs=12.5 kHz.
2. Slave mode operation, Fs = 12.5 kHz.
3. All inputs, except MCLK, are held static, and all outputs are unloaded.

Table 4. AC Characteristics

(V_A, V_D = 5 V ±5% or 3.3 V ±10%, T_A = 0°C to 70°C for K-grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC Resolution			—	16	—	Bits
ADC Dynamic Range[1,2]	ADCDR	VIN = 1 kHz, –3 dB	80	84	—	dB
ADC Total Harmonic Distortion[3]	ADCTHD	VIN = 1 kHz, –3 dB, MIC/LINEI	—	–80	–62	dB
V_A, V_D = 3.3 V ±10%		VIN = 1 kHz, –3 dB, HDST	—	–80	–62	
ADC Total Harmonic Distortion[3]	ADCTHD	VIN = 1 kHz, –3 dB, MIC/LINEI	—	–80	–76	dB
V_A, V_D = 5 V ±5%		VIN = 1 kHz, –3 dB, HDST	—	–80	–71	
ADC Full Scale Level (0 dB gain)[4]	V_{RX}	Vin = 1 kHz	—	1	—	V_{rms}
ADC Programmable Input Gain			–36	—	12	dB
ADC Input Gain Step Size			—	1.5	—	dB
ADC Freq Response[5]	F_{RR}	Low –3 dB corner	—	33	—	Hz
ADC Freq Response[5]	F_{RR}	300 Hz	–0.1	—	0	dB
ADC Freq Response	F_{RR}	3400 Hz	–0.2	—	0	dB
Line In Preamp Gain			—	0/10/20	—	dB
Mic In Preamp Gain			—	0/10/20/ 30	—	dB
ADC Input Resistance		0 dB Preamp Gain	—	20	—	kΩ
ADC Input Capacitance			—	15	—	pF
ADC Gain Drift	A_T	VIN = 1 kHz	—	0.002	—	dB/°C
DAC Resolution			—	16	—	Bits
DAC Dynamic Range[1,2]	DACDR	VIN = 1 kHz, –6 dB	80	84	—	dB
DAC Total Harmonic Distortion[3]	DACTHD	VIN=1 kHz,–6 dB,LINEO,600 Ω	—	–76	–60	dB
V_A, V_D = 3.3 V ±10%		VIN=1 kHz,–6 dB, SPKR, 60 Ω	—	–72	–60	
		VIN=1 kHz,–6 dB, HDST, 600 Ω	—	–80	–70	
DAC Total Harmonic Distortion[3]	DACTHD	VIN=1 kHz,–3 dB,LINEO,600 Ω	—	–76	–65	dB
V_A, V_D = 5 V ±5%		VIN=1 kHz,–3 dB, SPKR, 60 Ω	—	–72	–65	
		VIN=1 kHz,–3 dB, HDST, 600 Ω	—	–80	–76	
DAC Full Scale Level (0 dB gain)	V_{RX}		—	1	—	V_{rms}
DAC Programmable Output Gain			–36	—	12	dB

Notes:

1. DR = VIN + 20 log (RMS signal/RMS noise). Measurement bandwidth is 300 to 3400 Hz. Valid sample rate ranges between 4000 and 12000 Hz.
2. 0 dB setting for analog and digital attenuation/gain.
3. THD = 20 log (RMS distortion/RMS signal). Valid sample rate ranges between 4000 and 12000 Hz.
4. At 0dB gain setting, 1 V_{rms} input corresponds to -1.5 dB of full scale digital output code.
5. These characteristics are determined by external components. See Figure 13.
6. With a 600 Ω load. Output starts clipping with half of full scale digital input, which corresponds to a 0.5 V_{rms} output.

Table 4. AC Characteristics (Continued)
(V_A, V_D = 5 V ±5% or 3.3 V ±10%, T_A = 0°C to 70°C for K-grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DAC Output Gain Step Size			—	1.5	—	dB
DAC Freq Response[5]	F_{RR}	Low –3 dB corner	—	33	—	Hz
DAC Freq Response[5]	F_{RR}	300 Hz	–0.01	—	0	dB
DAC Freq Response	F_{RR}	3400 Hz	–0.2	—	0	dB
DAC Line Output Load Resistance			600	—	—	Ω
DAC Line Output Load Capacitance			—	—	40	pF
DAC SPKR Output Load Resistance			—	60	—	Ω
DAC Gain Drift	A_T	VIN = 1 kHz	—	0.002	—	dB/°C
Interchannel Isolation (Crosstalk)			—	90	—	dB
HDST Full Scale Level Input			—	0.5	—	V_{rms}
HDST Full Scale Level Output[6]			—	1.0	—	V_{rms}
HDST Output Resistance	Rout	DC	—	600	—	Ω
MIC Bias Voltage	V_{mbias}		—	2.5	—	V
MIC Power Supply Rejection Ratio	PSRR		—	40	—	dB

Notes:
1. DR = VIN + 20 log (RMS signal/RMS noise). Measurement bandwidth is 300 to 3400 Hz. Valid sample rate ranges between 4000 and 12000 Hz.
2. 0 dB setting for analog and digital attenuation/gain.
3. THD = 20 log (RMS distortion/RMS signal). Valid sample rate ranges between 4000 and 12000 Hz.
4. At 0dB gain setting, 1 V_{rms} input corresponds to -1.5 dB of full scale digital output code.
5. These characteristics are determined by external components. See Figure 13.
6. With a 600 Ω load. Output starts clipping with half of full scale digital input, which corresponds to a 0.5 V_{rms} output.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D, V_A	–0.5 to 6.0	V
Input Current, Si3000 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–10 to 100	°C
Storage Temperature Range	T_{STG}	–40 to 150	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Switching Characteristics—General Inputs
(V_A, V_D = 5 V ±5% or 3.3 V ±10%, T_A = 70°C for K-grade, C_L = 20 pF)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle Time, MCLK	t_{mc}		16.67	—	—	ns
MCLK Duty Cycle	t_{dty}		40	50	60	%
Rise Time, MCLK	t_r		—	—	5	ns
Fall Time, MCLK	t_f		—	—	5	ns
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}		250	—	—	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 5 µs or 10 MCLK cycle times.

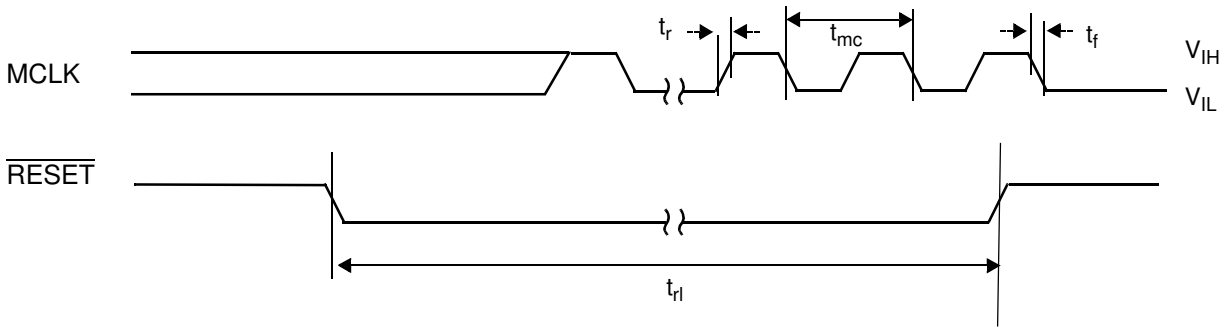


Figure 1. General Inputs Timing Diagram

Table 7. Switching Characteristics—Serial Interface
(V_A, V_D = 5 V ±5% or 3.3 V ±10%, T_A = 70°C for K-grade, C_L = 20 pF)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c		354	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}		—	50	—	%
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d1}		—	—	10	ns
Delay Time, SCLK ↑ to SDO Valid	t_{d2}		—	—	20	ns
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d3}		—	—	10	ns
Setup Time, SDI, before SCLK ↓	t_{su}		25	—	—	ns
Hold Time, SDI, after SCLK ↓	t_h		20	—	—	ns
Setup Time, FSYNC (mode 2) before MCLK ↓	t_{su}		25	—	—	ns
Hold Time, FSYNC (mode 2) after MCLK ↓	t_h		20	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V						

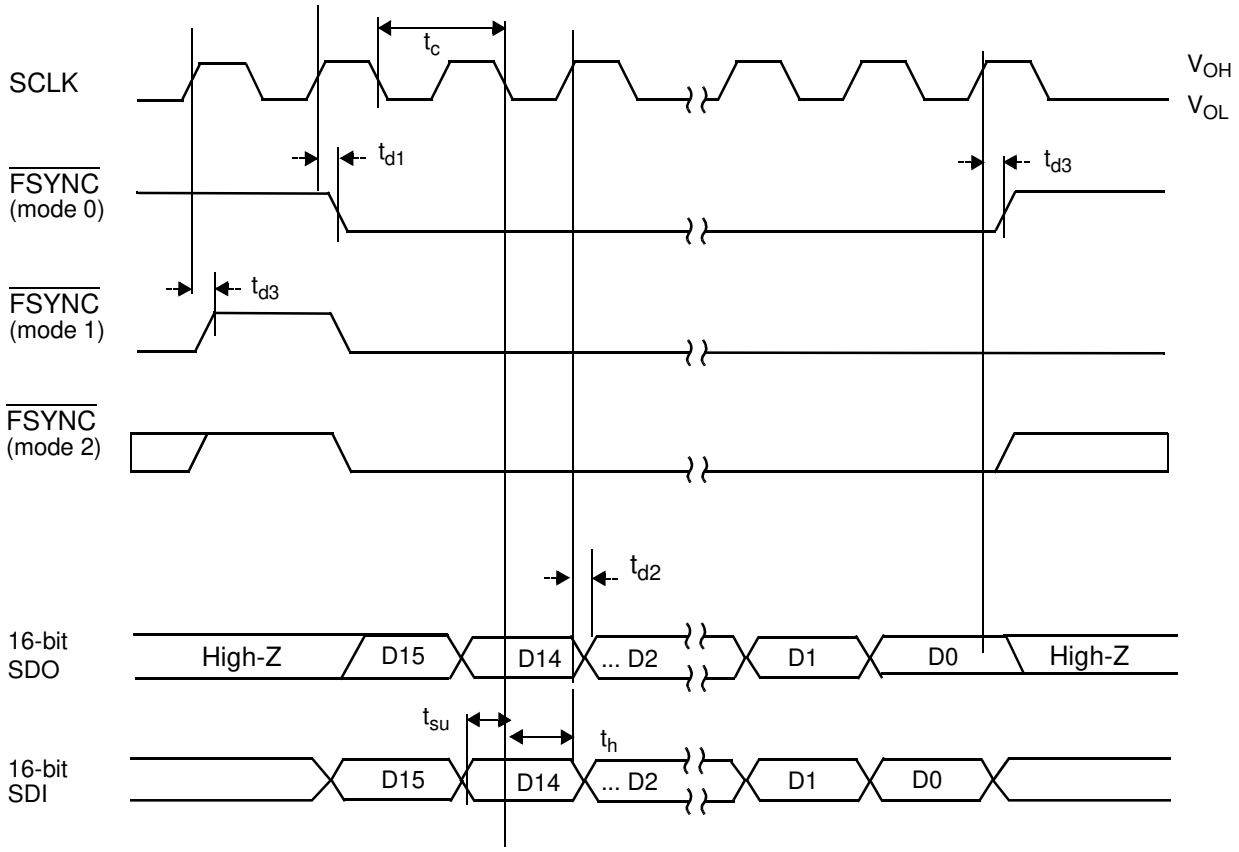


Figure 2. Serial Interface Timing Diagram

Table 8. Digital FIR Filter Characteristics—Transmit and Receive
(V_A, V_D = 5 V ±5% or 3.3 V ±10%, Sample Rate = 8 kHz, T_A = 70°C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB, HPFD = 1)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband (3 dB, HPFD = 0)	$F_{(3\ dB)}$	0.01	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	sec
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 3, 4, 5, and 6.					

Table 9. Digital IIR Filter Characteristics—Transmit and Receive
(V_A, V_D = 5 V ±5% or 3.3 V ±10%, Sample Rate = 8 kHz, T_A = 70°C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB, HPFD = 1)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband (3 dB, HPFD = 0)	$F_{(3\ dB)}$	0.01	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	sec
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 7, 8, 9, and 10. Figures 11 and 12 show group delay versus input frequency.					

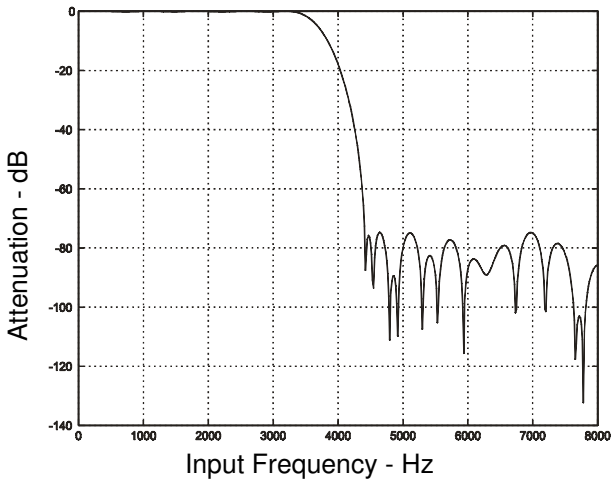


Figure 3. FIR Receive Filter Response

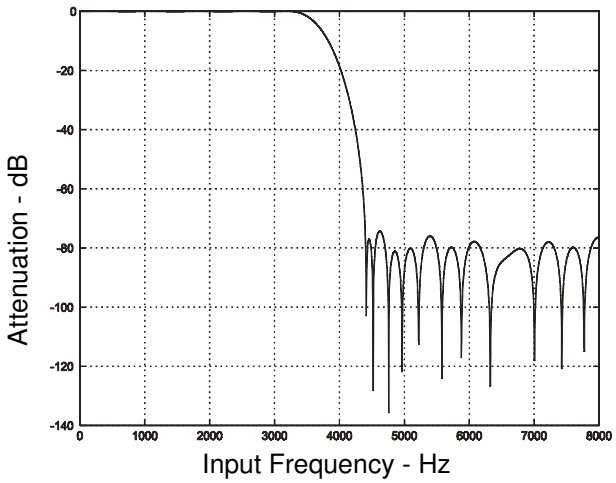


Figure 5. FIR Transmit Filter Response

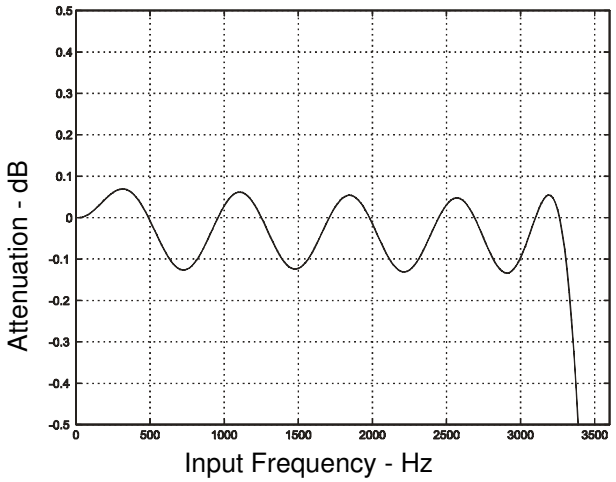


Figure 4. FIR Receive Filter Passband Ripple

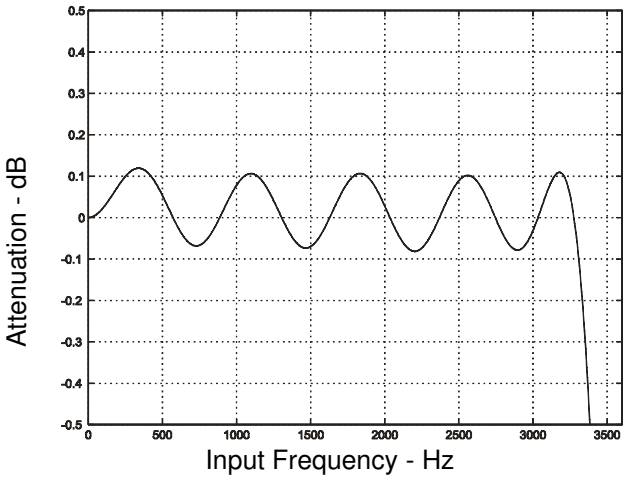


Figure 6. FIR Transmit Filter Passband Ripple

For Figures 3–6, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$$F_{(0.1\ dB)} = 0.4125\ Fs$$

$$F_{(-3\ dB)} = 0.45\ Fs$$

where Fs is the sample frequency.

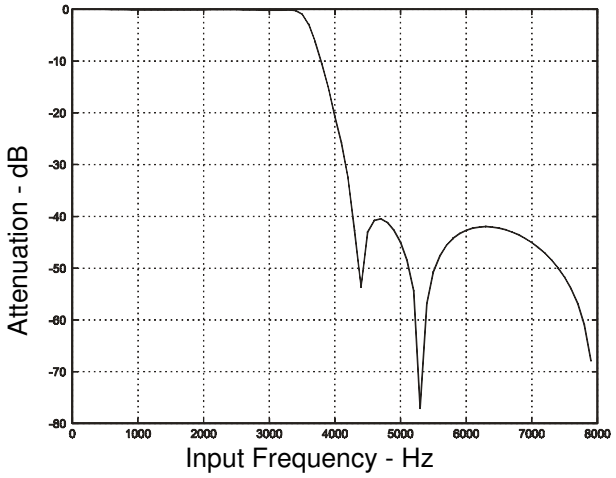


Figure 7. IIR Receive Filter Response

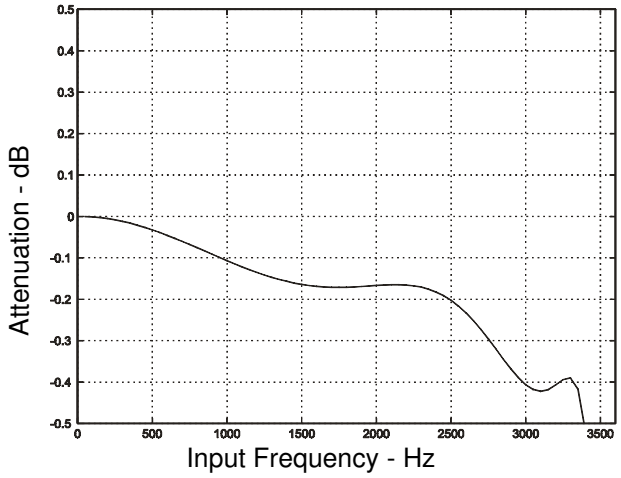


Figure 10. IIR Transmit Filter Passband Ripple

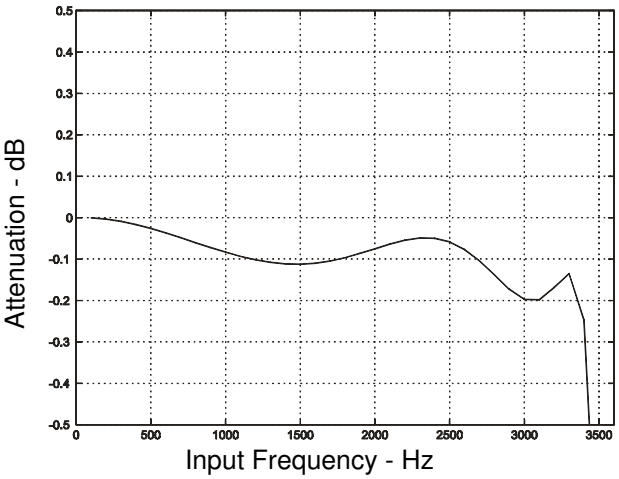


Figure 8. IIR Receive Filter Passband Ripple

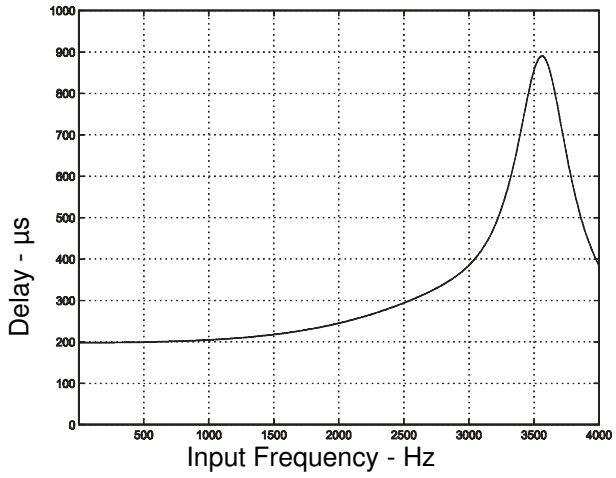


Figure 11. IIR Receive Group Delay

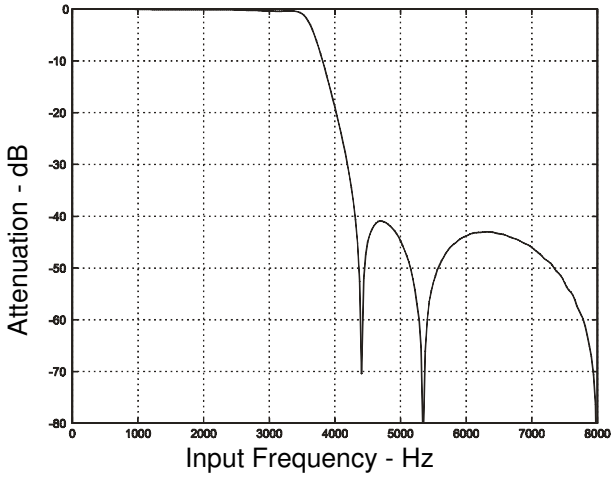


Figure 9. IIR Transmit Filter Response

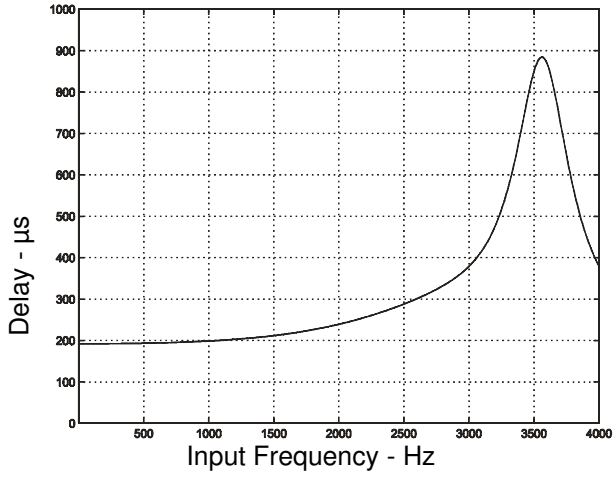
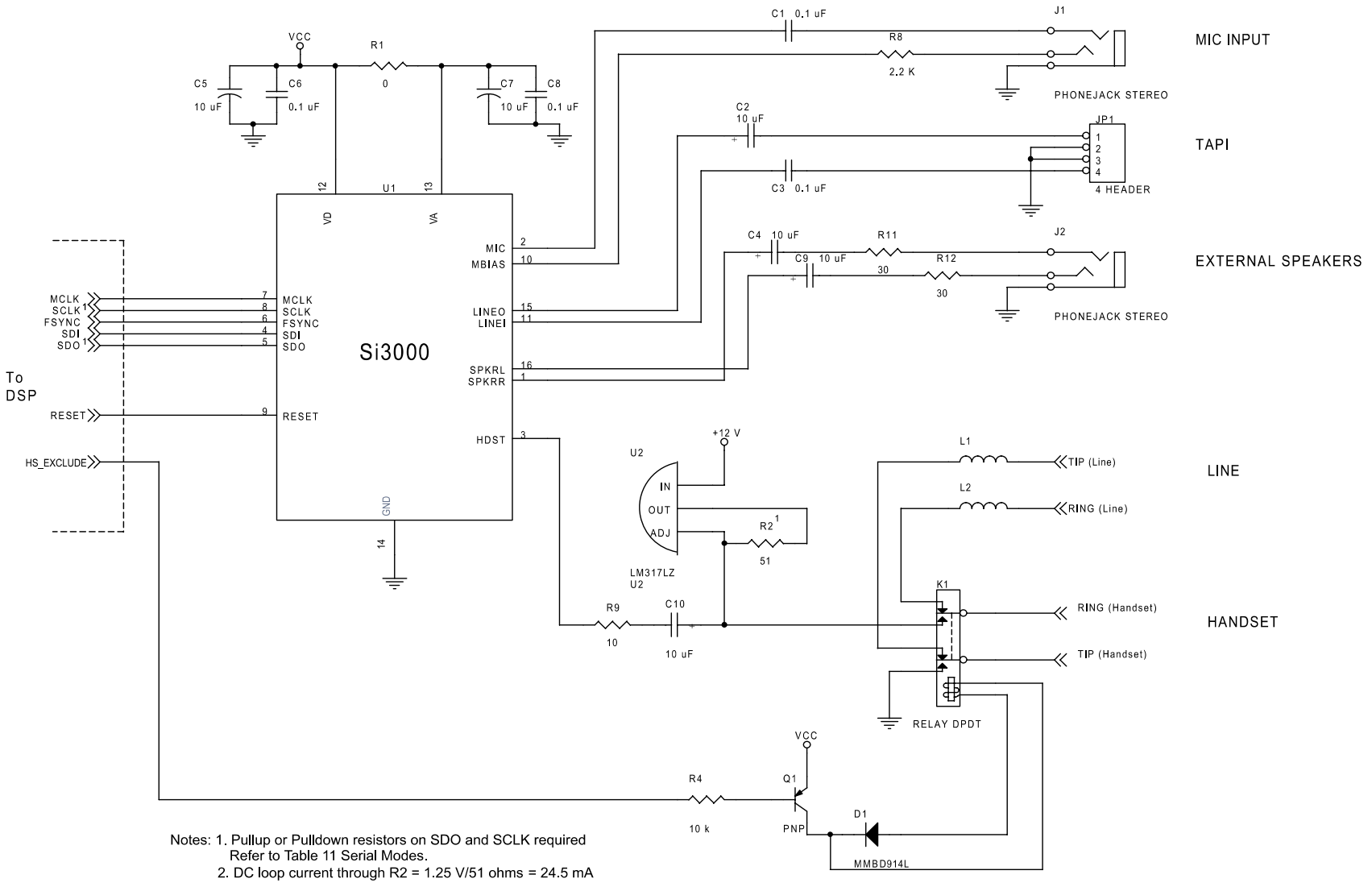


Figure 12. IIR Transmit Group Delay



Notes: 1. Pullup or Pulldown resistors on SDO and SCLK required
Refer to Table 11 Serial Modes.
2. DC loop current through R2 = 1.25 V/51 ohms = 24.5 mA

Figure 13. Si3000 Typical Application Circuit

Table 10. Component Values—Typical Application

Symbol	Value
C1,C3,C6,C8	0.1 µF, 16 V, ±20%
C2,C4,C5,C7,C9,C10	10 µF, 16 V, ±20%
D1	Motorola MMBD914L
J1,J2	Phonejack Stereo
JP1	4 Header
K1	Relay DPDT
L1,L2	Ferrite Bead
R1	0 Ω, 1/4 W ±5%
R2	51 Ω, 1/4 W ±5%
R4	10 kΩ, 1/4 W ±5%
R8	2.2 k, 1/4 W, ±5%
R9	10 Ω, 1/16 W, ±5%
R11,R12	30 Ω, 1/16 W, ±5%
U2	LM317LZ
Q1	PNP Transistor

Functional Description

The Si3000 is a highly integrated voice bandwidth audio codec which contains a single 16-bit A/D converter and D/A converter. The analog input path contains a microphone input with selectable gain, a line level input with selectable gain, and a handset input. Each of the inputs go through a mixer prior to A/D conversion. The result of this A/D conversion is a 16-bit signed number. Following the A/D converter is a digital programmable gain amplifier. The analog output path contains a digital programmable gain amplifier feeding a single 16-bit D/A converter. The DAC output is provided to a line output, a headphone drive output, and a handset output. Control for the various functions available on the Si3000 as well as the audio data are communicated to the device over a serial interface.

The Si3000 can be connected directly to the Si3035, Si3034, Si3044 in modem applications requiring a voice channel, or the device can be used as a stand-alone codec in other voice band applications. The Si3000 offers high integration, and it needs only a few low cost, discrete components as shown in Figure 13.

Analog Inputs

The typical connection diagram (Figure 13) shows the recommended external analog circuitry for the Si3000. The device supports three mono analog inputs—line level, microphone level, and a handset input. Each of these inputs is provided to a mixer circuit prior to A/D conversion. Each analog input may also be muted by writing the appropriate bits in the control registers. Unused analog inputs should be tied to GND through a 0.1 µF capacitor. This prevents any DC current flow.

Pre-amp/Microphone Bias Circuit

An internal amplifier with a selectable gain of 0 dB, 10 dB, 20 dB, or 30 dB is provided for the MIC input and an internal amplifier with a selectable gain of 0 dB, 10 dB, or 20 dB, is provided for the LINEI input. AC coupling is required for both inputs because any DC offset on the input will be amplified if gain is selected. Gain settings for the LINEI and MIC inputs are achieved by writing the RX Gain Control 1 register 5. When gain is disabled, these inputs become line level inputs with a full scale input of 1 Vrms.

A microphone bias circuit is provided on-chip which consists of a 2.5 V reference output capable of sourcing up to 5 mA of current. This circuit can be used for active microphones requiring a bias source.

Programmable Input Gain/Attenuation

The signals from the microphone, line, or handset inputs are mixed and then routed to the A/D converter and a digital programmable gain circuit which provides up to 12 dB of gain or –34.5 dB of attenuation in 1.5 dB steps. Level changes only take effect on zero crossings to minimize audible artifacts. The requested level change is implemented if no zero crossing is found after 256 frames. Write the ADC Volume Control register 6 to set digital input gain/attenuation.

Analog Outputs

The analog outputs of the D/A converter are routed to a line level output (LINEO), a pair of speaker outputs (SPKRL and SPKRR), and a handset. Each analog output can be independently muted.

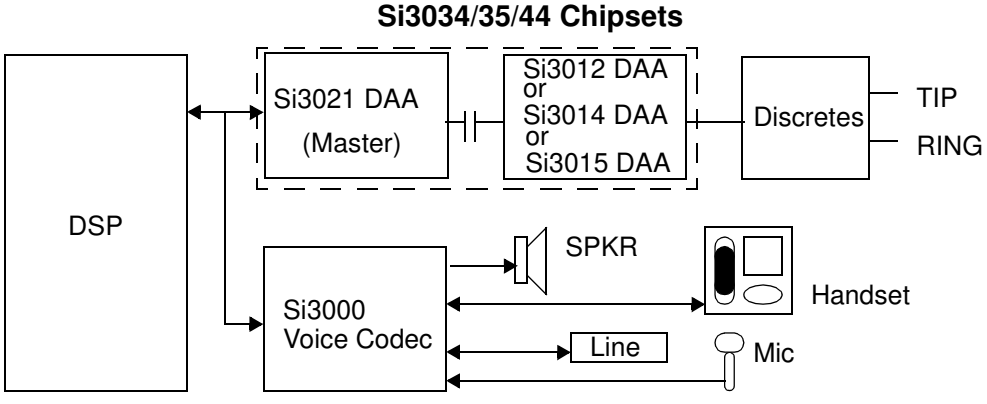


Figure 14. Si3000 with Silicon Labs DAA System Diagram

Programmable Output Gain/Attenuation

Prior to D/A conversion, the Si3000 contains a digital programmable gain/attenuator which provides up to 12 dB of gain or –34.5 dB of attenuation in 1.5 dB steps. Level changes only take effect on zero crossings to minimize audible artifacts. The requested level change is implemented if no zero crossing is found after 256 frames. Write the DAC Volume Control (register 7) to set digital input gain/attenuation.

Line Output

LINEO is a line level analog output signal centered around a common mode voltage. The minimum recommended load impedance is 600 Ω. This output is a fully filtered output with a 1 Vrms full scale range. The only external component required is the 10 µF DC blocking capacitor shown in Figure 13 on page 12. This output may be muted through the LOM bit in register 6 or attenuated by setting the analog attenuation bits in register 9.

Speaker Output

The SPKRL and SPKRR analog outputs are capable of driving a small loudspeaker whose impedance is typically 32 Ω (see Figure 13 on page 12). The speaker outputs may be muted through the SLM and SRM bits in the DAC Gain Control register 7 or attenuated by setting the analog attenuation bits in register 9.

Digital Interface

The Si3000 has two serial interface modes that support most standard modem DSPs. These modes are selected by the addition of a 50 kΩ pull-down/up resistor on the SDO and SCLK pins as shown in Figure 13 on page 12. To determine the mode, the Si3000 reads SDO and SCLK on the first rising edge of MCLK after $\overline{\text{RESET}}$ goes low. The key difference between these two serial modes is the operation of the $\overline{\text{FSYNC}}$ signal. Table 11 summarizes the serial mode definitions.

Table 11. Serial Modes

Mode	SCLK*	SDO*	Description
0	0	0	$\overline{\text{FSYNC}}$ frames data
1	0	1	$\overline{\text{FSYNC}}$ pulse starts data frame
2	1	0	Slave mode
3	1	1	Reserved
***Note:** Pull-up/pull-down states			

The digital interface consists of a single synchronous serial link which communicates audio and control data.

In slave mode, SCLK is connected only to the pullup/pulldown resistor, and MCLK is a 256 Fs input which is internally multiplied using the on-chip phase-locked loop (PLL) to clock the A/D converter and D/A converter. In master mode, the master clock (MCLK) is an input and the serial data clock (SCLK) is an output. The MCLK frequency and the value of the sample rate control registers 3 and 4 determine the sample rate (Fs). The serial port clock, SCLK, runs at 256 bits per frame, where the frame rate is equivalent to the sample rate.

Digital information is transferred between the DSP and the Si3000 in the form of 16-bit Primary Frames and 16-bit Secondary Frames. There are separate pins for receive (SDO) and transmit (SDI) functions, providing simultaneous receive/transmit operation within each frame.

Primary Frames are used for digital audio data samples. Primary Frames occur at the frame rate and are always present.

Secondary Frames are used for accessing internal Si3000 registers. Secondary Frames are not always present and are requested on-demand. When Secondary Frames are present, they occur mid-point between Primary Frames. Hence, no Primary Frames are dropped.

On Primary Frame transmits (DSP to Si3000), the Si3000 treats the LSB (16th bit) as a flag to request a Secondary Frame. Therefore, out of 16-bits of transmit data on SDI, only 15-bits represent actual audio data. When secondary frames are not present, no transmission occurs during this time slot.

On Primary Frames receives (Si3000 to DSP), the Si3000 drives SDO with 16-bits of audio data, if the Si3000 is in either Serial Mode 0 or 1. However, if the Si3000 is in SLAVE mode (Mode 2), the Si3000 supplies 15-bits of Audio Data to the DSP and always drives the LSB zero. This feature is designed to work with the Si3021 register 14 SSEL set to 10. In this system configuration, when the DSP receives Primary Frames, it can check the LSB to determine whether the receive data is from the Si3021 or from the Si3000.

On Secondary Frame receives and transmits; the Si3000 treats the input and output serial stream as 16-bits of data. Figure 15 shows the relative timing of the serial frames.

Figure 16 and Figure 17 illustrate the secondary frame write cycle and read cycle, respectively. During a read cycle, the R/$\overline{\text{W}}$ bit is high and the 5-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed on the SDO signal. During a write cycle, the R/$\overline{\text{W}}$ bit is low and the 5-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on SDI. Only one register can be read or written during each secondary frame. See "Control Registers," on page 20 for the register addresses and functions.

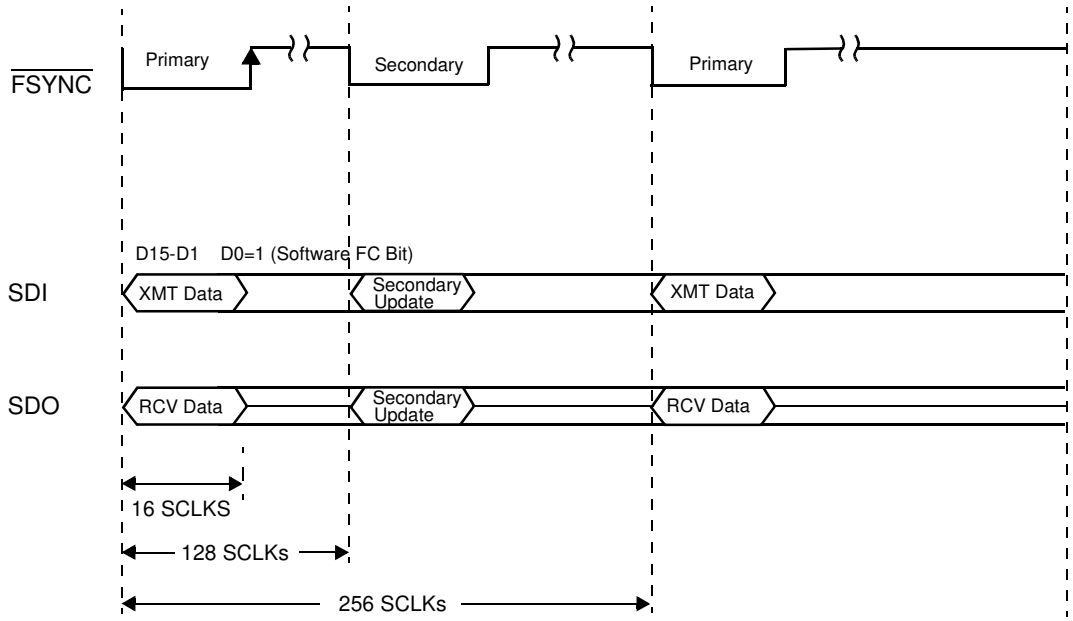


Figure 15. Secondary Request

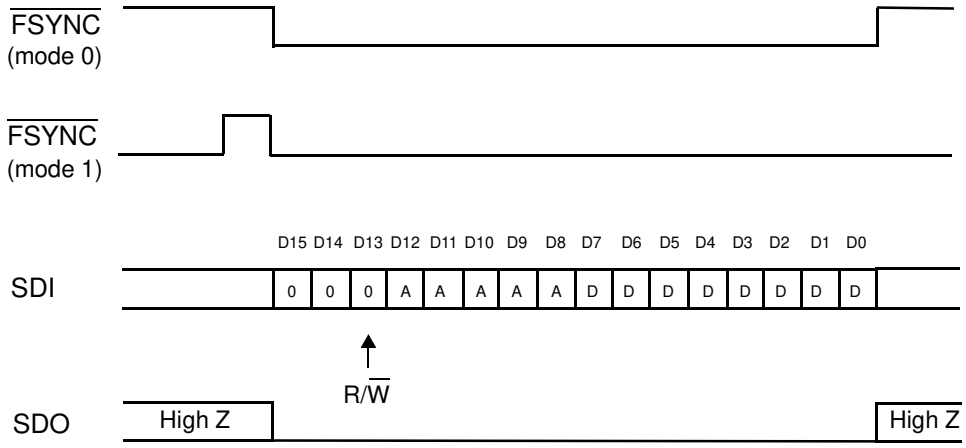


Figure 16. Secondary Communication Data Format—Write Cycle

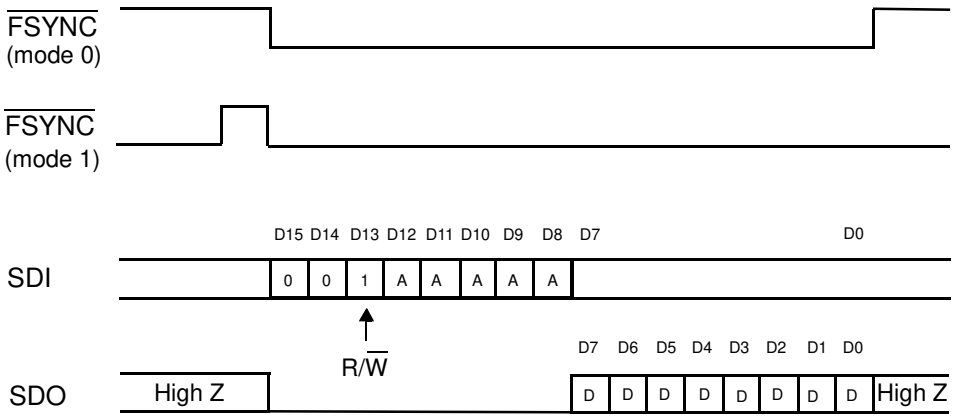


Figure 17. Secondary Frame Format—Read Cycle

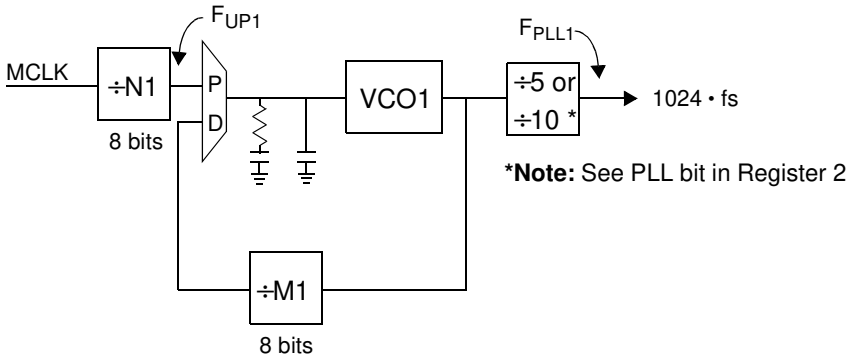


Figure 18. Clock Generation Subsystem (PLL)

Clock Generation Subsystem

The Si3000 contains an on-chip clock generator. Using a single MCLK input frequency, the Si3000 can generate all the desired standard modem sample rates, as well as the common 11.025 kHz rate for audio playback.

The clock generator consists of a phase-locked loop (PLL1) that achieves the desired sample frequency. Figure 18 illustrates the clock generator. The architecture of the PLL allows for fast lock time on initial start-up, fast lock time when changing modem sample rates and high noise immunity. A large number of MCLK frequencies between 1 MHz and 60 MHz are supported.

Programming the Clock Generator

As noted in Figure 18, the clock generator must output a clock equal to 1024*Fs, where Fs is the desired sample rate. The 1024*Fs clock is determined through programming of the following registers:

Register 3 - N1 divider, 8 bits.

Register 4 - M1 divider, 8 bits

N1 (register 3) and M1 (register 4) are 8-bit unsigned values. F_{MCLK} is the clock provided to the MCLK pin. Table 12 list several standard crystal rates that could be supplied to MCLK.

When programming the registers of the clock generator, the order of register writes is important. For PLL updates, N1 (register 3) must always be written first, immediately followed by a write to M1 (register 4).

Note: The values shown in Table 12 satisfy the equations above. However, when programming the registers for N1 and M1, the value placed in these registers must be one less than the value calculated from the equations.

Table 12. MCLK Examples for 8 kHz

MCLK (MHz)	N1	M1
1.8432	9	200
4.0000	25	256
4.0960	1	10
5.2800	33	256
5.7600	9	64
6.1440	3	20
8.1920	1	5
9.2160	9	40
10.0800	63	256
10.5600	33	128
11.0592	27	100
12.288	3	10
14.7456	9	25
16.0000	25	64
18.4320	9	20
24.5760	3	5
25.8048	63	100
33.7600	211	256
44.2368	27	25
46.0800	9	8
47.9232	117	100
48.0000	75	64
56.0000	175	128
59.200	185	128

PLL Lock Times

The Si3000 changes sample rates very quickly. However, lock time will vary based on the programming of the clock generator. The following relationship describes the boundaries on PLL locking time:

PLL lock time < 1 ms

It is recommended that the PLL be programmed during initialization.

The final design consideration for the clock generator is the update rate of PLL. The following criteria must be satisfied in order for the PLL to remain stable:

$$F_{UP1} = F_{MCLK} / (N1) \geq 144 kHz$$

Where F_{UP1} is shown in Figure 18.

Setting Generic Sample Rates

The above clock generation description focuses on common modem sample rates. The restrictions and equations above still apply; however, a more generic relationship between MCLK and Fs (the desired sample rate) is needed. The following equation describes this relationship:

$$\frac{M1}{N1} = \frac{5 \cdot 1024 \cdot Fs}{MCLK}$$

where *Fs* is the sample frequency, and all other symbols are shown in Figure 18.

Knowing the MCLK frequency and desired sample rate the values for the M1 and N1 registers can be determined. When determining these values, remember to consider the range for each register as well as the minimum update rate for the first PLL.

The values determined for M1 and N1 must be adjusted by minus one when determining the value written to the respective registers. This is due to internal logic, which adds one to the value stored in the register. This addition allows the user to write a zero value in any of the registers and the effective divide-by is one. A special case occurs when both M1 and N1 are programmed with a zero value. When M1 and N1 are both zero, the PLL is bypassed.

Sleep Mode

The Si3000 supports a low-power sleep mode. Sleep mode is activated by setting the Chip Power Down (CPD) bit in register 1. When the Si3000 is in sleep mode, the MCLK signal may be stopped or remain active, but it *must* be active before waking up the Si3000. To take the Si3000 out of sleep mode, pulse the reset pin ($\overline{\text{RESET}}$) low. In summary, the power down/up sequence is as follows:

1. Set the Power Down bit (PDN, register 6, bit 3).
2. MCLK may stay active or stop.
3. Restore MCLK before initiating the power up sequence.
4. Reset the Si3000 using the $\overline{\text{RESET}}$ pin (after MCLK is present).
5. Program the registers to desired settings.

Loopback Operation

The Si3000 advanced design provides the manufacturer with increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Two loopback modes exist for this purpose, allowing increased coverage of system components.

The digital loopback1 mode allows an external device to send audio data to the SDI input pin and receive the signal through the SDO output pin. In this mode, the group delay of the digital filters is present. This mode allows testing of the digital filters, DAC, and ADC. To enable this mode, set the DL bit of register 2.

The digital loopback2 mode allows an external device to send audio data to the SDI input pin and receive the signal through the SDO output pin. This mode allows testing of the digital filters, but not the ADC and DAC.

Reducing Power-on Pop Noise

To minimize power-on pop during initialization, a waiting period is recommended before powering up the analog output drivers. The waiting period starts when the reset signal to the Si3000 is negated. The wait time required is dependent on the external load. Typically, the load consists of an AC coupling capacitor in series with an equivalent load resistor to ground. The equivalent load resistor can either be a speaker load, or the input resistance of an external amplifier. The rule-of-thumb for the waiting period in msec is derived by C*(12+R). For example, in the case of a 10 µF AC coupling capacitor and resistive load of 1.0 kΩ the recommended waiting period is 10*(12+1) = 130 msec.

If the analog outputs drive external amplifiers, another factor to consider is the voltage division ratio determined by R/(R+12), where R represents the input resistance of the external amplifier. This ratio must be kept as small as possible. A good target value is R = 1 kΩ. If needed, add a load resistor in parallel with the amplifier input to lower the effective input resistance of the amplifier stage.

Control Registers

Note: Any register not listed here is reserved and should not be written. Any register bit labelled reserved should be written to zero during writes to the register. Register 0 can be read (always returns 0) and written safely.

Table 13. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR			SPD	LPD	HPD	MPD	CPD
2	Control 2				HPFD	PLL	DL1	DL2	
3	PLL1 Divide N1	Divider N1							
4	PLL1 Multiply M1	Multiplier M1							
5	RX Gain Control 1	LIG		LIM	MCG		MCM	HIM	IIR
6	ADC Volume Control		RXG					LOM	HOM
7	DAC Volume Control		TXG					SLM	SRM
8	Status Report	SLSC	SRSC	LOSC					
9	Analog Attenuation					LOT		SOT	

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR			SPD	LPD	HPD	MPD	CPD
Type	R/W			R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset**. 1 = Sets all registers to their reset value. 0 = Enables chip for normal operation. **Note:** Bit will automatically clear after being set.
6:5	Reserved	Read returns zero.
4	SPD	**Speaker Drive Power Down.** 1= Normal operation 0 = Power down left and right speaker drive.
3	LPD	**Line Drive Power Down.** 1 = Normal operation 0 = Power down line driver.
2	HPD	**Handset Drive Power Down.** 1 = Normal operation 0 = Power down handset driver.
1	MPD	**MIC Bias Power Down.** 1 = Power down MIC bias buffer. 0 = Normal operation
0	CPD	**Chip Power Down**. 1 = Puts Si3000 into power down mode. 0 = Normal operation

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				HPFD	PLL	DL1	DL2	
Type				R/W	R/W	R/W	R/W	

Reset Settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	HPFD	**High Pass Filter (HPF) Disable.** 1 = HPF disabled 0 = HPF enabled
3	PLL	**PLL Divide by 10.** 1 = Sets final stage of PLL to divide by 10. 0 = Sets final stage of PLL to divide by 5.
2	DL1	**Digital Loopback.** 1 = Enables digital loopback (DAC analog out → ADC analog in). 0 = Normal operation
1	DL2	**Digital Loopback.** 1 = Enables digital loopback (DAC one bit → ADC one bit). 0 = Normal operation
0	Reserved	Read returns zero.

Register 3. PLL1 Divide N1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Divider N1							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	N1	**N1.** Contains the (value – 1) for determining the output frequency on PLL.

Register 4. PLL1 Multiply M1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Multiplier M1							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	M1	**M1.** Contains the (value – 1) for determining the output frequency on PLL.

Register 5. RX Gain Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LIG		LIM	MCG		MCM	HIM	IIR
Type	R/W		R/W	R/W		R/W	R/W	R/W

Reset settings = 0100_0111

Bit	Name	Function
7:6	LIG	**Line in Gain.** 11 = 20 dB gain 10 = 10 dB gain 01 = 0 dB gain 00 = Reserved
5	LIM	**Line in Mute.** 1 = Line input muted 0 = Line input goes to mixer
4:3	MCG	**MIC Input Gain.** 11 = 30 dB gain 10 = 20 dB gain 01 = 10 dB gain 00 = 0 dB gain
2	MCM	**MIC Input Mute.** 1 = Mute MIC input 0 = MIC input goes into mixer.
1	HIM	**Handset Input Mute.** 1 = Mute handset input 0 = Handset input goes into mixer.
0	IIR	**IIR Enable.** 1 = Enables IIR filter 0 = Enables FIR filter

Register 6. ADC Volume Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RXG					LOM	HOM
Type	R/W						R/W	R/W

Reset settings = 0101_1100

Bit	Name	Function
7	Reserved	Read returns zero.
6:2	RXG	**RX PGA Gain Control.** 11111 = 12 dB 10111 = 0 dB 00000 = –34.5 dB LSB = 1.5 dB
1	LOM	**Line Out Mute.** 0 = Mute 1 = Active
0	HOM	**Handset Out Mute.** 0 = Mute 1 = Active