Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Si3056
Si3018/19/10

GLOBAL SERIAL INTERFACE DIRECT ACCESS ARRANGEMENT

Features

Complete DAA includes the following:

- Programmable line interface
  - AC termination
  - DC termination
  - Ring detect threshold
  - Ringer impedance
- 80 dB dynamic range TX/RX paths
- Integrated codec and 2- to 4-wire hybrid
- Integrated ring detector
- Type I and II caller ID support
- Line voltage monitor
- Loop current monitor
- Polarity reversal detection
- Programmable digital gain
- Clock generation
- Pulse dialing support
- Overload detection
- 3.3 V power supply
- Direct interface to DSPs
- Serial interface control for up to eight devices
- >5000 V isolation
- Proprietary isolation technology
- Parallel handset detection
- +3.2 dBm TX/RX level mode
- Programmable digital hybrid for near-end echo reduction
- Low-profile SOIC packages
- Lead-free/RoHS-compliant packages available

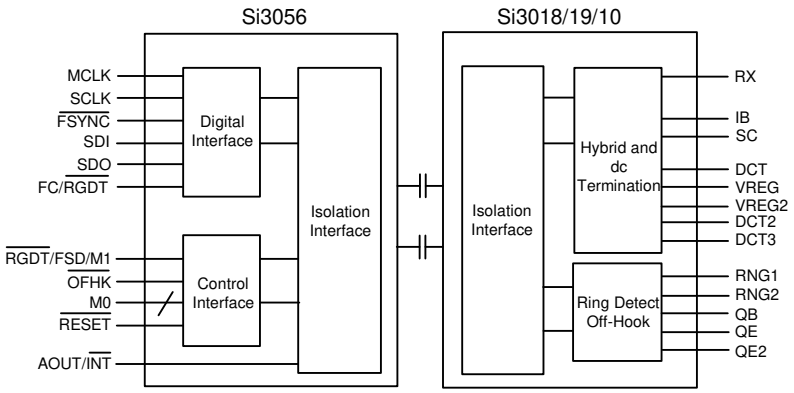
Applications

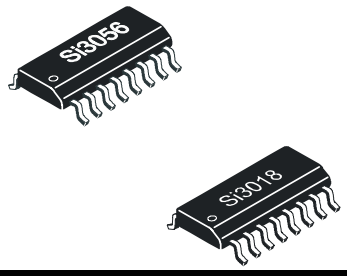
- V.92 modems
- Voice mail systems
- Multi-function printers
- Set-top boxes
- Fax machines
- Internet appliances
- Personal digital assistants

Description

The Si3056 is an integrated direct access arrangement (DAA) with a programmable line interface to meet global telephone line requirements. Available in two 16-pin small outline packages, it eliminates the need for an analog front end (AFE), isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3056 dramatically reduces the number of discrete components and cost required to achieve compliance with global regulatory requirements. The Si3056 interfaces directly to standard modem DSPs.

Functional Block Diagram



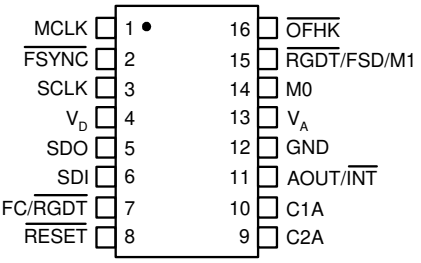


Ordering Information

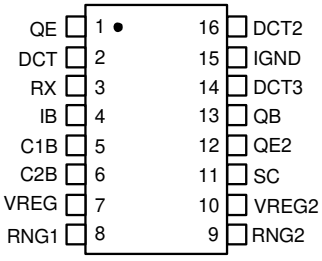
See page 87.

Pin Assignments

Si3056



Si3018/19/10



US Patent # 5,870,046
US Patent # 6,061,009
Other Patents Pending

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	F and K-Grade	0	25	70	°C
Si3056 Supply Voltage, Digital[3]	V_D		3.0	3.3	3.6	V

Notes:
1. The Si3056 specifications are guaranteed when the typical application circuit (including component tolerance) and the Si3056 and any Si3018 or Si3019 are used. See Figure 17 on page 18 for typical application schematic.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. 3.3 V applies to both the digital and serial interface and the digital signals RGDT/FSD, OFHK, RESET, M0, and M.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, see Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 11, ILIM = 0, DCV = 00, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, MINI = 11, ILIM = 0, DCV = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 00, ILIM = 0, DCV = 11, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, MINI = 00, ILIM = 0, DCV = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	—	—	40	V
On Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current		DC current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT = 0	13.5	15	16.5	V_{rms}
Ring Detect Voltage*	V_{RD}	RT = 1	19.35	21.5	23.65	V_{rms}
Ring Frequency	F_R		13	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

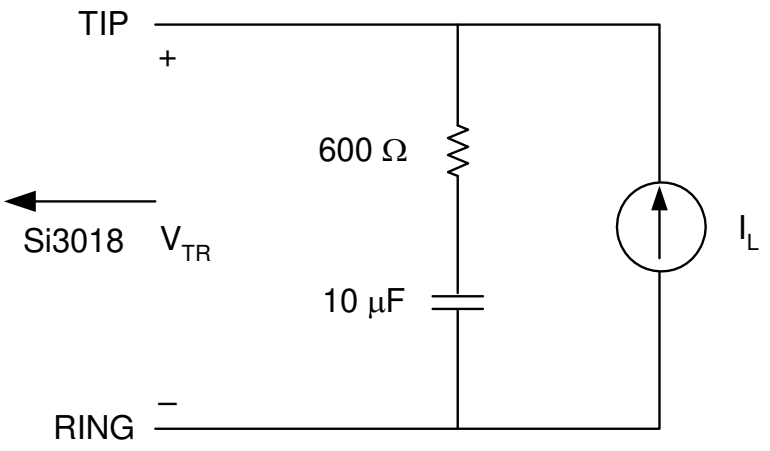


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.4	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Digital[1]	I_D	V_D pin	—	15	—	mA
Total Supply Current, Sleep Mode[1]	I_D	PDN = 1, PDL = 0	—	9	—	mA
Total Supply Current, Deep Sleep[1,2]	I_D	PDN = 1, PDL = 1	—	1	—	mA

Notes:

1. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs are held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
2. RGDT is not functional in this state.

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C; see Figure 17 on page 18)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate[1]	Fs	Fs = F_{PLL2}/5120	7.2	—	16	kHz
PLL Output Clock Frequency[1]	F_{PLL1}	F_{PLL1} = (F_{MCLK} x M)/N	—	98.304	—	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	0	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1[11]	—	200	—	Hz
Transmit Full Scale Level[2,3]	V_{FS}	FULL = 0 (0 dBm)	—	1.1	—	V_{PEAK}
		FULL = 1[11](3.2 dBm)	—	1.58	—	V_{PEAK}
		FULL2 = 1 (6.0 dBm)	—	2.16	—	V_{PEAK}
Receive Full Scale Level[2,4]	V_{FS}	FULL = 0 (0 dBm)		1.1		V_{PEAK}
		FULL = 1[11](3.2 dBm)	—	1.58	—	V_{PEAK}
		FULL2 = 1 (6.0 dBm)	—	2.16	—	V_{PEAK}
Dynamic Range[5,6,7]	DR	ILIM = 0, DCV = 11, DCR = 0, I_L = 100 mA, MINI = 00	—	80	—	dB
Dynamic Range[5,6,7]	DR	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	80	—	dB
Dynamic Range[5,6,7]	DR	ILIM = 1, DCV = 11, DCR = 0, I_L = 50 mA, MINI = 00	—	80	—	dB
Transmit Total Harmonic Distortion[8,9]	THD	ILIM = 0, DCV = 11, DCR = 0, I_L = 100 mA, MINI = 00	—	–72	—	dB
Transmit Total Harmonic Distortion[8,9]	THD	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	–78	—	dB

Notes:

1. See Figure 26 on page 37.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. With FULL = 1, the transmit and receive full scale level of +3.2 dBm can be achieved with a 600 Ω ac termination, while the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances in “FULL” mode. With FULL2 = 1, the transmit and receive full scale level of +6.0 dBm can be achieved with a 600 Ω ac termination. In “FULL2” mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
4. Receive full scale level produces –0.9 dBFS at SDO.
5. DR = 20 x log (RMS V_{FS}/RMS V_{IN}).+ 20 x log (RMS V_{IN}/RMS noise). The RMS noise measurement excludes harmonics. V_{FS} is the 0 dBm full-scale level.
6. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths. V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
7. When using the Si3010 line-side, the typical DR values will be approximately 10 dB lower.
8. THD = 20 x log (RMS distortion/RMS signal). V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
9. When using the Si3010 line-side, the typical THD values will be approximately 10 dB higher.
10. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log(RMS V_{IN}/RMS noise). V_{CID} is the 6 V full-scale level for the typical application circuit in Figure 17. With the enhanced CID circuit, the V_{CID} full-scale level is 1.5 V peak, and DR_{CID} increases to 62 dB.
11. Available on the Si3019 line-side device only.

Table 4. AC Characteristics (Continued)
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C; see Figure 17 on page 18)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Total Harmonic Distortion[8,9]	THD	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	–78	—	dB
Receive Total Harmonic Distortion[8,9]	THD	ILIM = 1, DCV = 11, DCR = 0, I_L = 50 mA, MINI = 00	—	–78	—	dB
Dynamic Range (caller ID mode)[10,7]	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	50	—	dB
Caller ID Full Scale Level[10]	V_{CID}		—	6	—	V_{PEAK}
AOUT Low Level Current			—	—	10	mA
AOUT High Level Current			—	—	10	mA

Notes:
1. See Figure 26 on page 37.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. With FULL = 1, the transmit and receive full scale level of +3.2 dBm can be achieved with a 600 Ω ac termination, while the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances in “FULL” mode. With FULL2 = 1, the transmit and receive full scale level of +6.0 dBm can be achieved with a 600 Ω ac termination. In “FULL2” mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
4. Receive full scale level produces –0.9 dBFS at SDO.
5. DR = 20 x log (RMS V_{FS}/RMS V_{IN}).+ 20 x log (RMS V_{IN}/RMS noise). The RMS noise measurement excludes harmonics. V_{FS} is the 0 dBm full-scale level.
6. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths. V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
7. When using the Si3010 line-side, the typical DR values will be approximately 10 dB lower.
8. THD = 20 x log (RMS distortion/RMS signal). V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
9. When using the Si3010 line-side, the typical THD values will be approximately 10 dB higher.
10. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log(RMS V_{IN}/RMS noise). V_{CID} is the 6 V full-scale level for the typical application circuit in Figure 17. With the enhanced CID circuit, the V_{CID} full-scale level is 1.5 V peak, and DR_{CID} increases to 62 dB.
11. Available on the Si3019 line-side device only.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 3.6	V
Input Current, Si3056 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage can occur if the above absolute maximum ratings are exceeded. Restrict functional operation to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

Table 6. Switching Characteristics—General Inputs

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_{mc}	16.67	—	1000	ns
MCLK Duty Cycle	t_{dty}	40	50	60	%
MCLK Jitter Tolerance	t_{jitter}	—	—	±2	ns
Rise Time, MCLK	t_r	—	—	5	ns
Fall Time, MCLK	t_f	—	—	5	ns
MCLK Before $\overline{\text{RESET}}$ ↑	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}	250	—	—	ns
M0, M Before $\overline{\text{RESET}}$↑[3]	t_{mxr}	20	—	—	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V. Rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 MCLK cycle times.
3. M0 and M are typically connected to V_D or GND and should not be changed during normal operation.

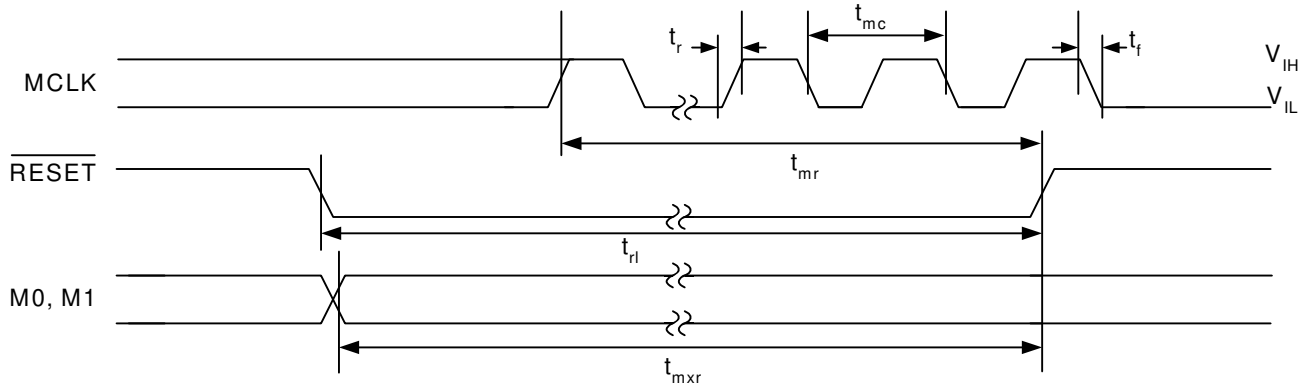


Figure 2. General Inputs Timing Diagram

Table 7. Switching Characteristics—Serial Interface (Master Mode, DCE = 0)
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	244	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↓	t_{d1}	—	—	20	ns
Delay Time, SCLK↑ to SDO Valid	t_{d2}	—	—	20	ns
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↑	t_{d3}	—	—	20	ns
Setup Time, SDI Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDI After SCLK ↓	t_h	20	—	—	ns
Setup Time, FC↑ Before SCLK↑	t_{sfc}	40	—	—	ns
Hold time, FC↑ After SCLK↑	t_{hfc}	40	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V.					

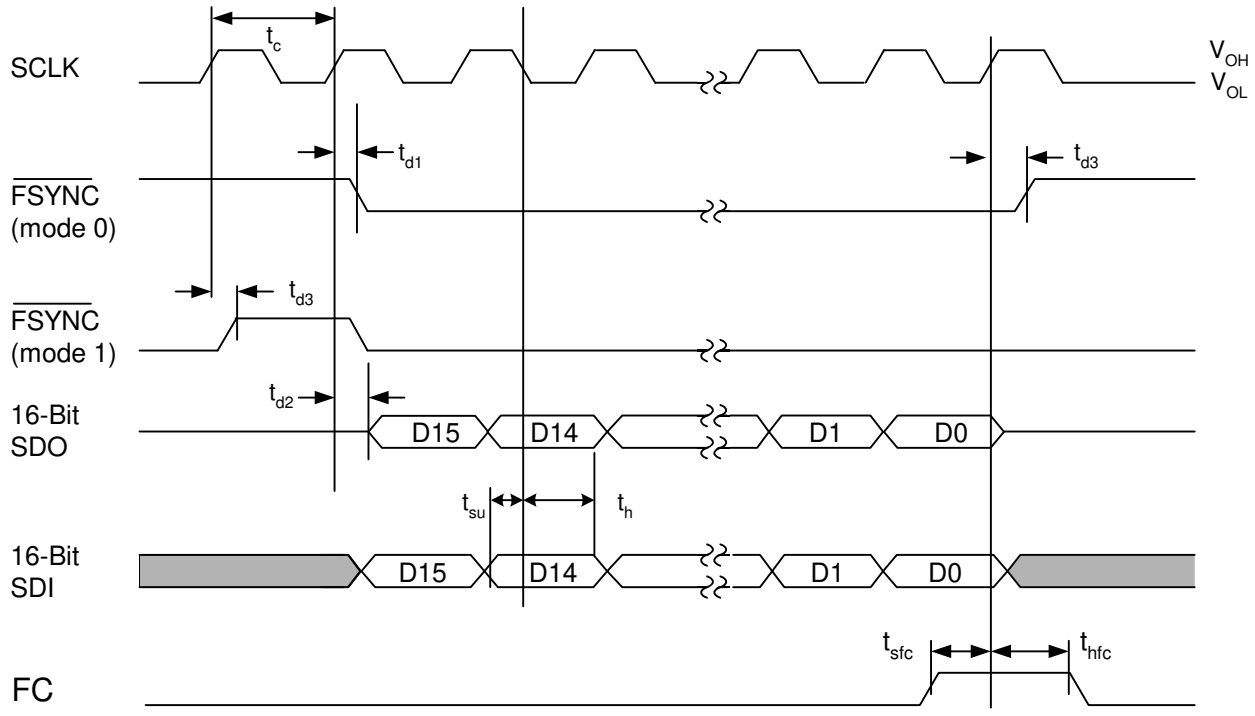


Figure 3. Serial Interface Timing Diagram (DCE = 0)

Table 8. Switching Characteristics—Serial Interface (Master Mode, DCE = 1, FSD = 0)
(V_A = Charge Pump, V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter[1,2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	244	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↑	t_{d1}	—	—	20	ns
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↓	t_{d2}	—	—	20	ns
Delay Time, SCLK↑ to SDO valid	t_{d3}	—	—	20	ns
Delay Time, SCLK↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK↑ to FSD↓	t_{d5}	—	—	20	ns
Delay Time, SCLK↑ to FSD↑	t_{d6}	—	—	20	ns
Setup Time, SDO Before SCLK↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK↓	t_h	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V.
2. See "5.27.Multiple Device Support" on page 38 for functional details.

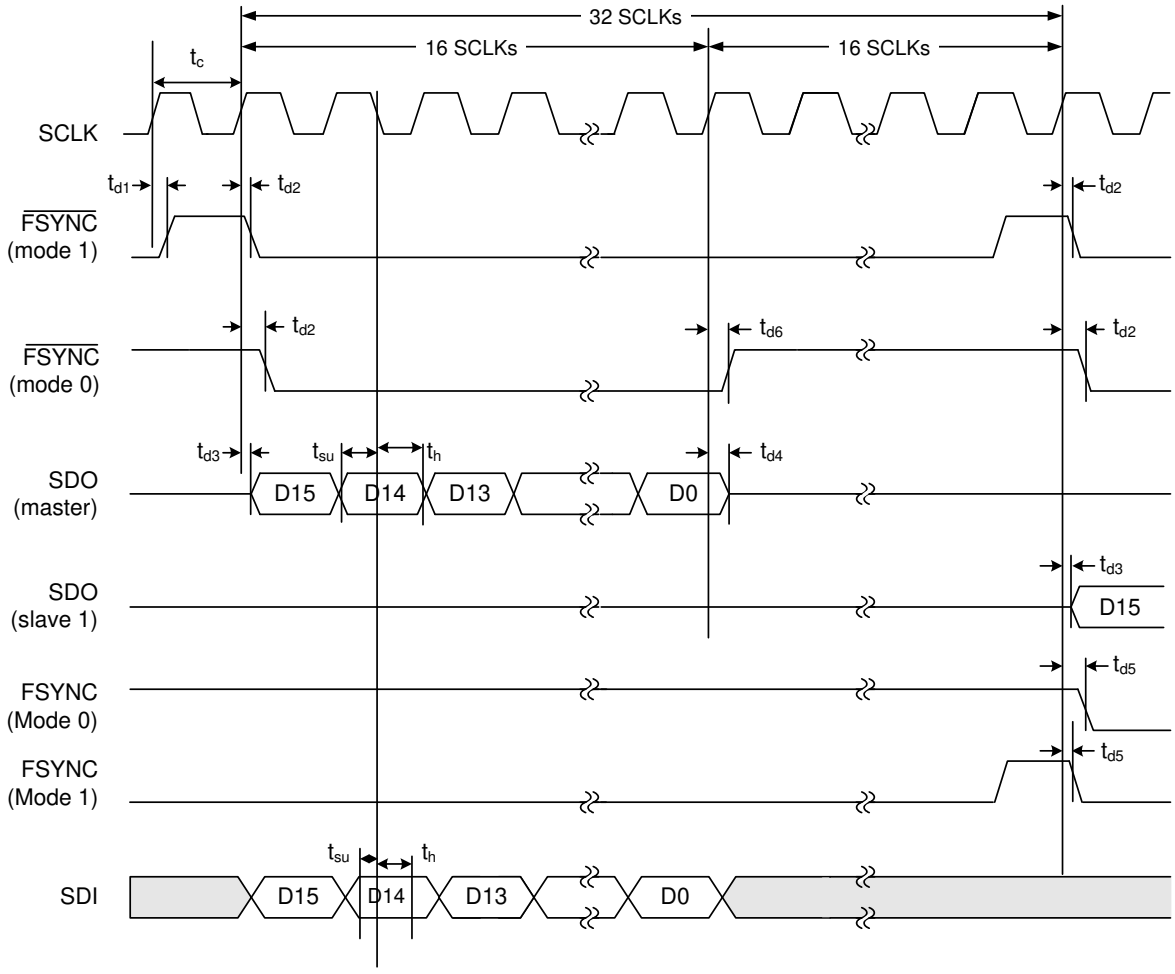


Figure 4. Serial Interface Timing Diagram (DCE = 1, FSD = 0)

Table 9. Switching Characteristics—Serial Interface (Master Mode, DCE = 1, FSD = 1)
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter[1, 2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	244	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↑	t_{d1}	—	—	20	ns
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↓	t_{d2}	—	—	20	ns
Delay Time, SCLK↑ to SDO Valid	t_{d3}	—	—	20	ns
Delay Time, SCLK↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK↑ to FSD↓	t_{d5}	—	—	20	ns
Setup Time, SDO Before SCLK↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK↓	t_h	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V.
2. See "5.27.Multiple Device Support" on page 38 for functional details.

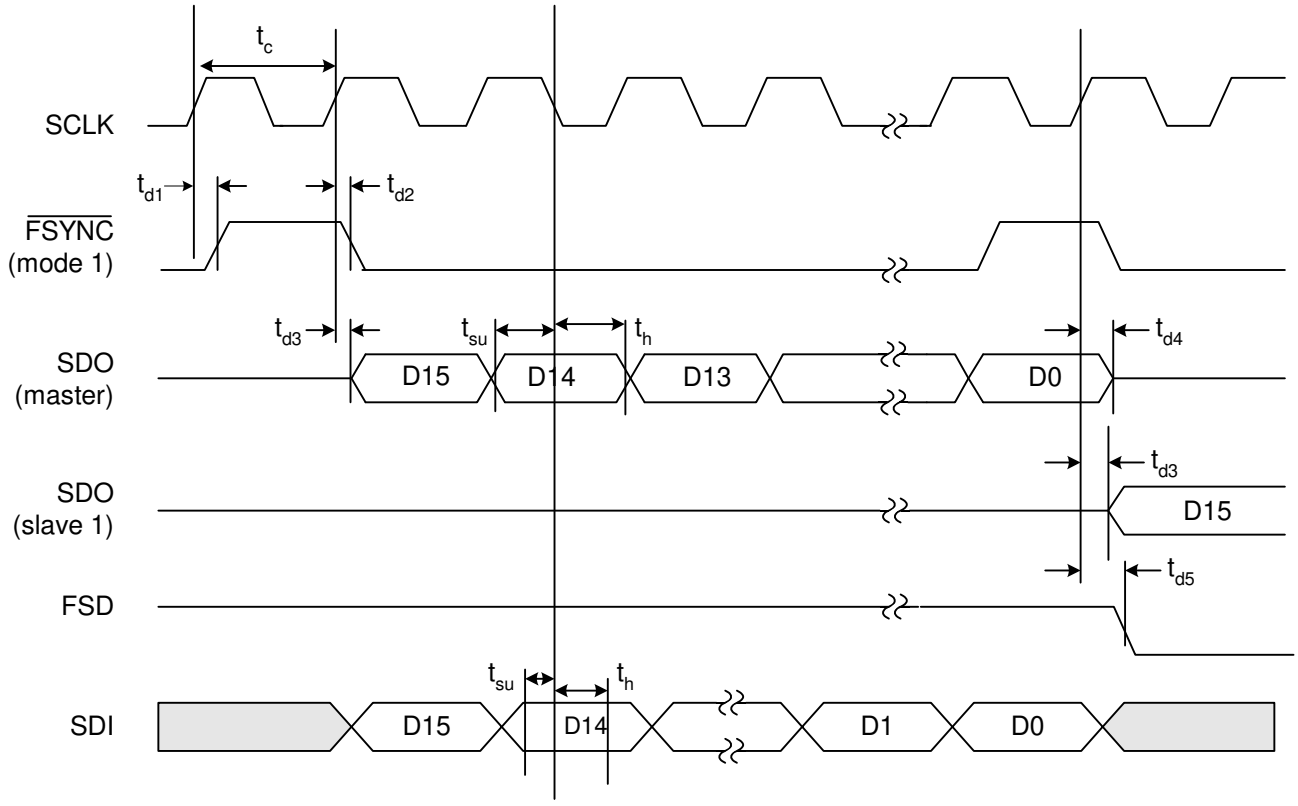


Figure 5. Serial Interface Timing Diagram (DCE = 1, FSD = 1)

Table 10. Switching Characteristics—Serial Interface (Slave Mode, DCE = 1, FSD = 1)
(V_A = Charge Pump, V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_c	244	1/256 Fs	—	ns
Setup Time, FSYNC↑ before MCLK↓*	t_{su1}	—	—	20	ns
Delay Time, FSYNC↑ after MCLK↓*	t_{d1}	—	—	20	ns
Setup Time, SDI before MCLK↓	t_{su3}	—	—	20	ns
Hold Time, SDI After MCLK↓	t_{h2}	—	—	20	ns
Delay Time, MCLK↑ to SDO	t_{d3}	—	—	20	ns
Delay Time, MCLK↑ to FSYNC↑	t_{d1}	—	—	20	ns
Delay Time, MCLK↑ to FSYNC↓	t_{d2}	—	—	20	ns
***Note:** T_{su1} and T_{h1} are listed for applications where the controller drives the MCLK and FSYNC instead of a master DAA.					

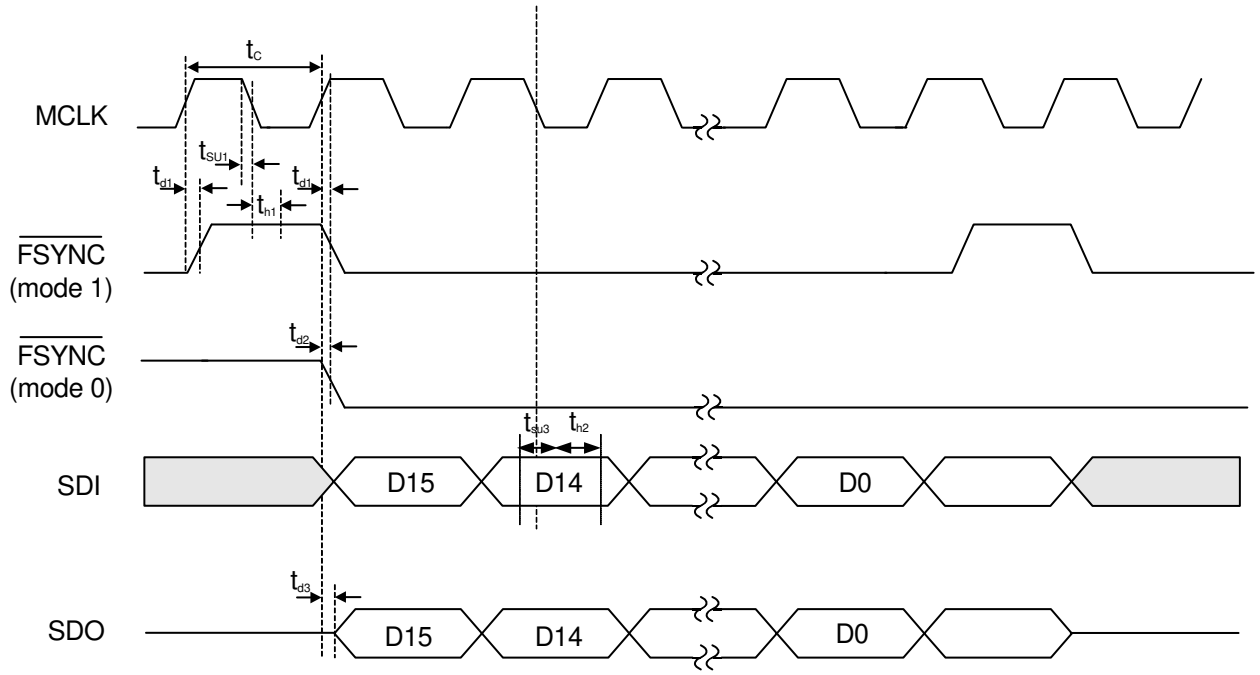


Figure 6. Serial Interface Timing Diagram (Slave Mode, DCE = 1, FSD = 1)

Table 11. Digital FIR Filter Characteristics—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 7, 8, 9, and 10.					

Table 12. Digital IIR Filter Characteristics—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	s
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 11, 12, 13, and 14. Figures 15 and 16 show group delay versus input frequency.					

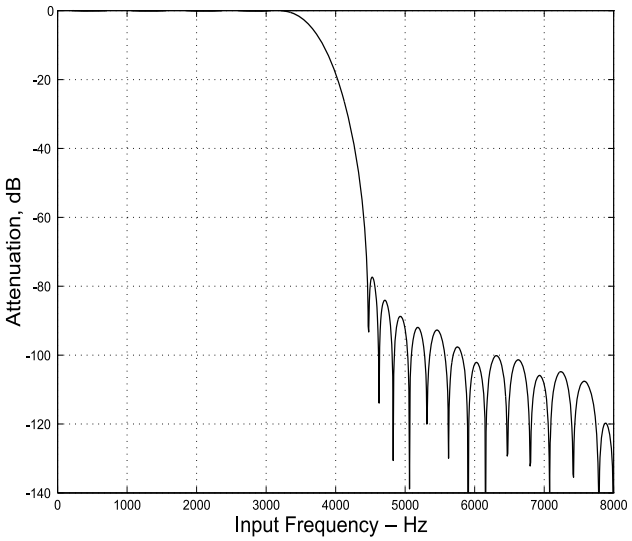


Figure 7. FIR Receive Filter Response

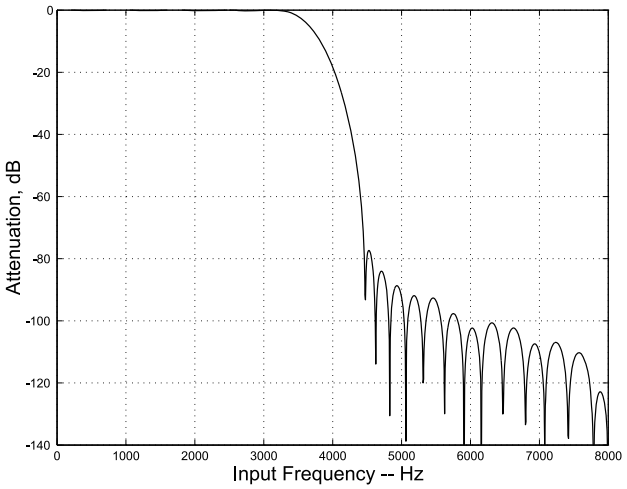


Figure 9. FIR Transmit Filter Response

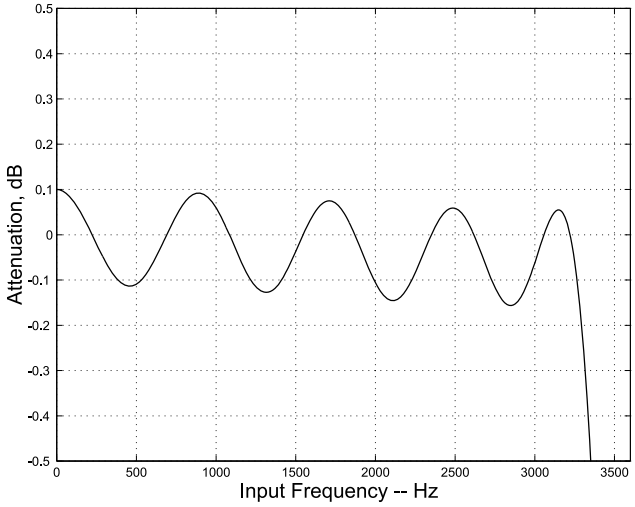


Figure 8. FIR Receive Filter Passband Ripple

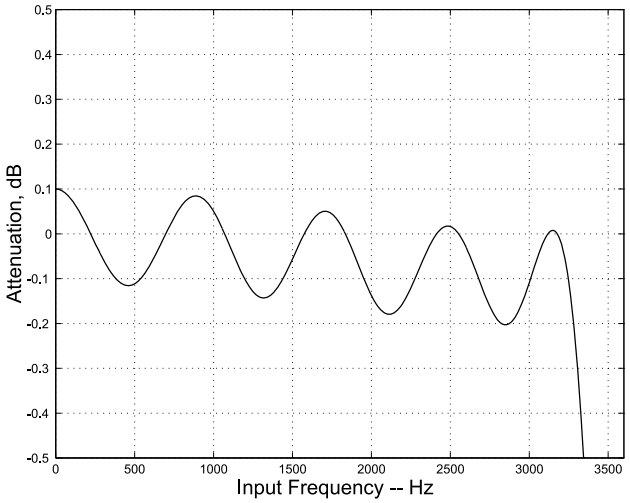


Figure 10. FIR Transmit Filter Passband Ripple

For Figures 7–10, all filter plots apply to a sample rate of Fs = 8 kHz.

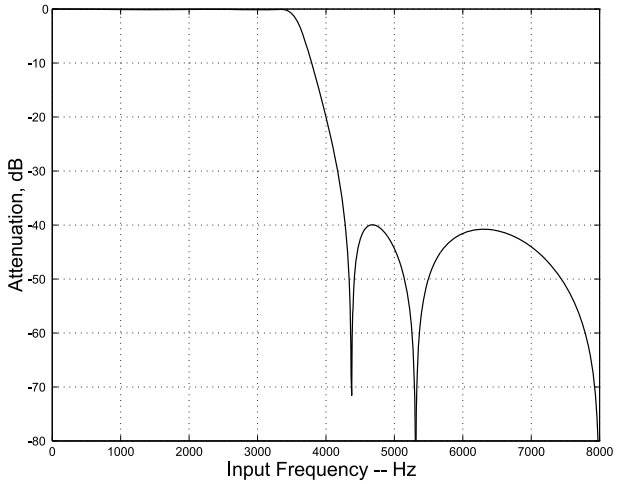


Figure 11. IIR Receive Filter Response

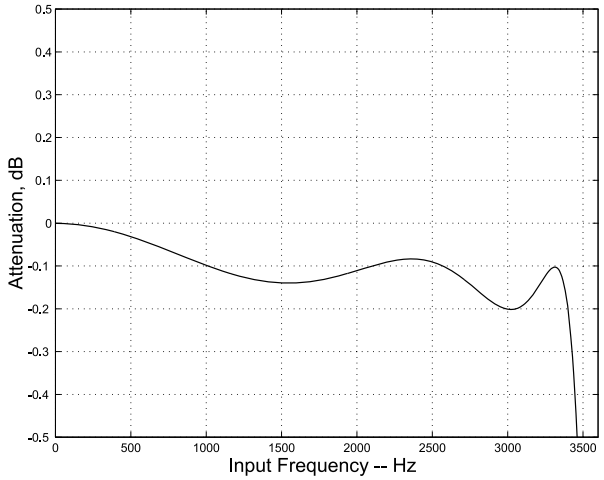


Figure 14. IIR Transmit Filter Passband Ripple

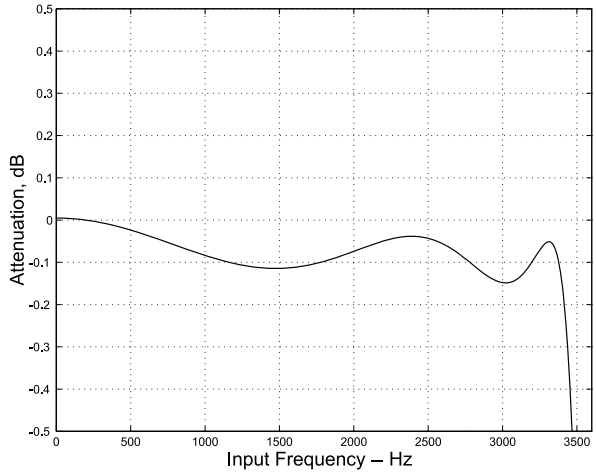


Figure 12. IIR Receive Filter Passband Ripple

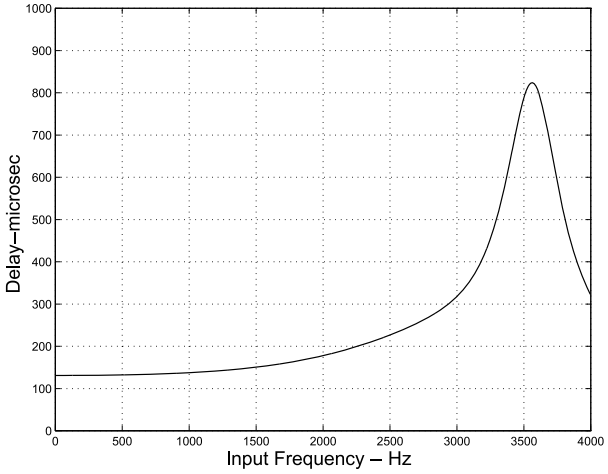


Figure 15. IIR Receive Group Delay

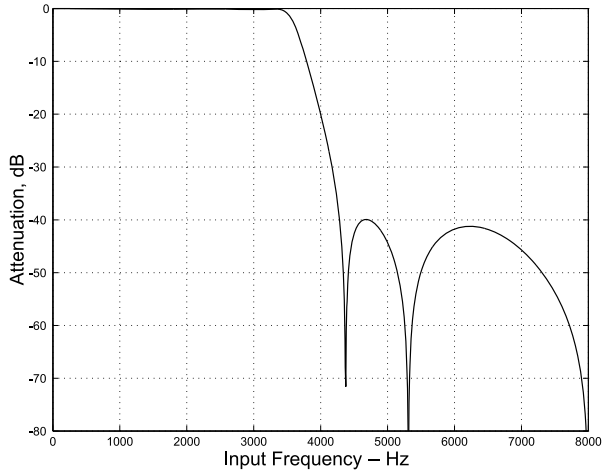


Figure 13. IIR Transmit Filter Response

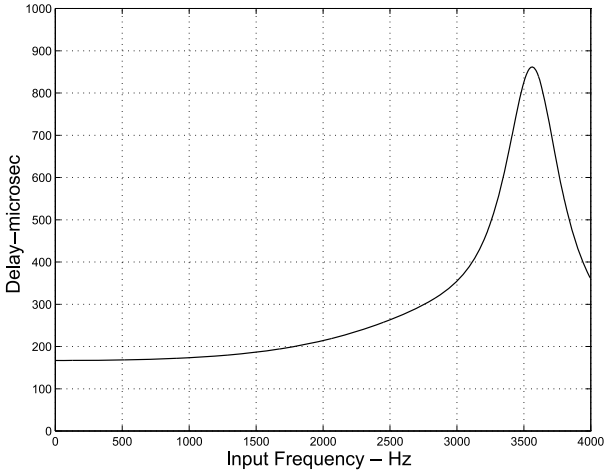


Figure 16. IIR Transmit Group Delay

2. Typical Application Schematic

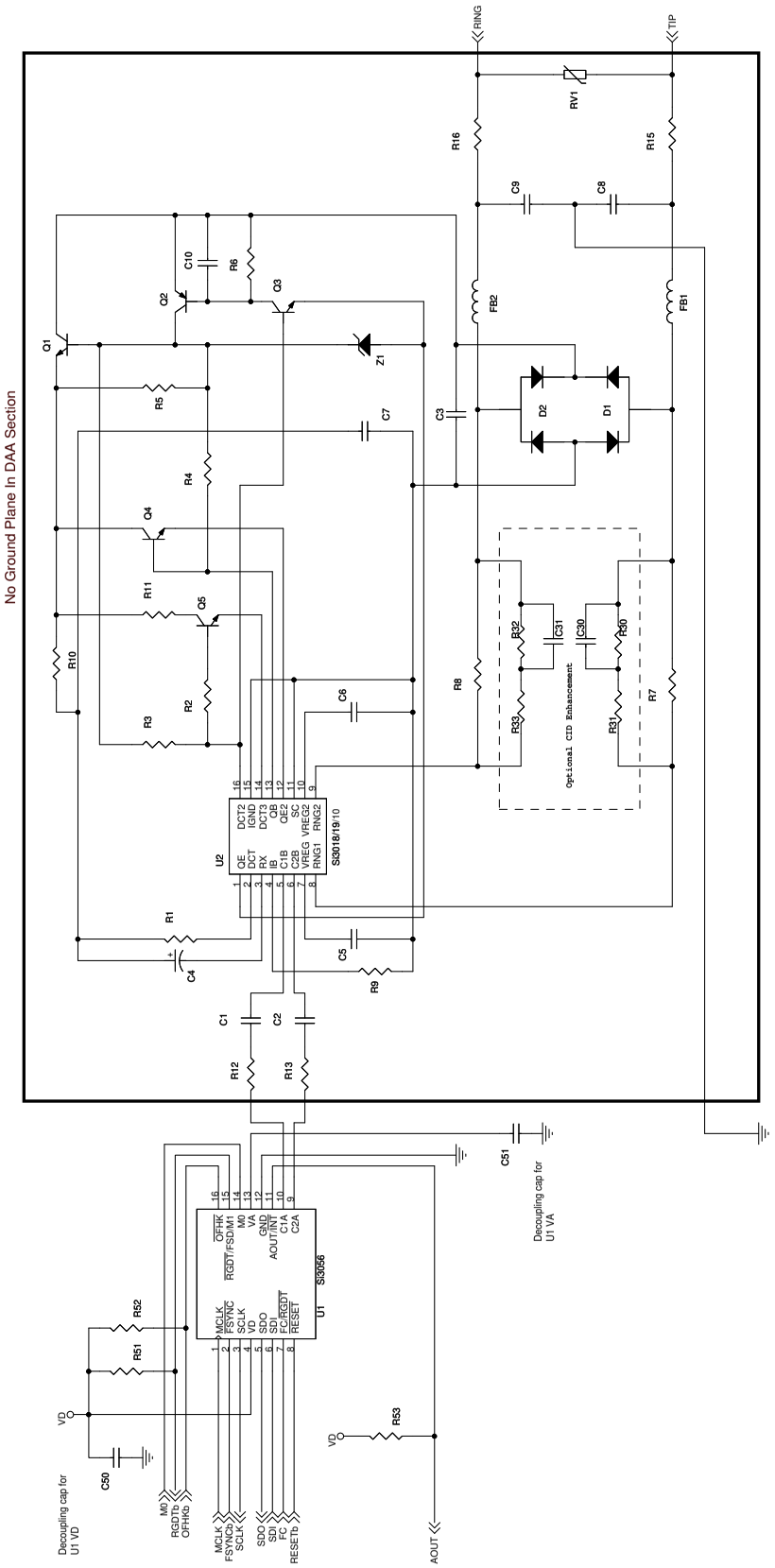


Figure 17. Typical Application Circuit for the Si3056 and Si3018/19/10 (Refer to AN67 for recommended layout guidelines)

3. Bill of Materials

Component(s)	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3[1]	10 nF, 250 V, X7R, ±10%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C51	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, 20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 µF, 16 V, X7R, ±20%	Venkel, SMEC
C30, C31[2]	Not installed, 120 pF, 250V, X7R, ±10%	Venkel, SMEC
D1, D2[3]	MMBD3004S-7-T (V_{RRM} = 350 V and I_F = 0.225 mA)	Diodes, Inc.
FB1, FB2	Ferrite Bead, BLM18AG601SN1B	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
Q4, Q5	NPN, 60 V, 330 mW, MMBTA06	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8[3]	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13	56.2 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonic
R15, R16[4]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R30, R32[2]	Not installed, 15 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R31, R33[2]	Not installed, 5.1 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R51, R52	4.7 kΩ, 1/10 W, 5%	Venkel, SMEC, Panasonic
U1	Si3056	Silicon Labs
U2	Si3018/19/10	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W, ZMM43	General Semiconductor

Notes:

1. Value for C3 above is recommended for use with the Si3018. In voice appliations, a C3 value of 3.9 nF (250 V, X7R, 20%) is recommended to improve return loss performance.
2. C30-31 and R30-33 can be substitued for R7-8 to implent the enhanced caller ID circuit.
3. Several diode configurations are acceptable, with the main requirement being $V_{RRM} \geq 350$ and $I_F \geq 225$ mA, e.g., part number HD04-T in a MiniDIP package by Diodes, Inc., two MMBD3004S-7-F diode pairs by Diodes, Inc. in an SOT-23 package, or four 1N4004 diodes.
4. Murata BLM18AG601SN1B may be substituted for R15-R16 (0 Ω) to decrease emissions.

4. AOUT PWM Output

Figure 18 illustrates an optional circuit to support the pulse width modulation (PWM) output capability of the Si3056 for call progress monitoring purposes. Set the PWME bit (Register 1, bit 3) to enable this mode.

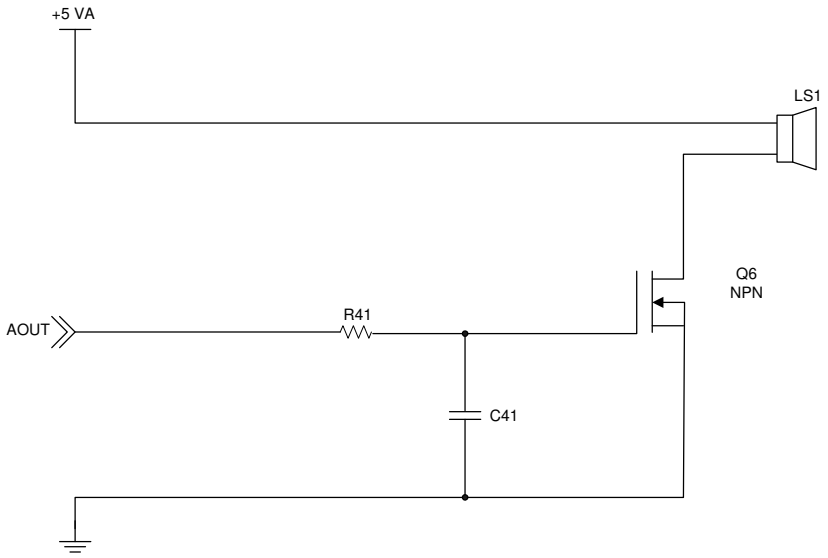


Figure 18. AOUT PWM Circuit for Call Progress

Table 13. Component Values—AOUT PWM

Component	Value	Supplier
LS1	Speaker BRT1209PF-06	Intervox
Q6	NPN KSP13	Fairchild
C41	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
R41	150 Ω, 1/16 W, ±5%	Venkel, SMEC, Panasonic

Registers 20 and 21 allow the receive and transmit paths to be attenuated linearly. When these registers are set to all 0s, the receive and transmit paths are muted. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

The PWMM[1:0] bits (Register 1, bits 5:4) select one of the three different PWM output modes for the AOUT signal, including a delta-sigma data stream, a conventional 32 kHz return to zero PWM output, and balanced 32 kHz PWM output.

5. Functional Description

The Si3056 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The Si3056 implements Silicon Laboratories® patented isolation technology and offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two 16-pin packages.

The Si3056 DAA is software programmable to meet global requirements and is compliant with FCC, TBR21, JATE, and other country-specific PTT specifications as shown in Table 16 on page 26. In addition, the Si3056 meets the most stringent worldwide requirements for out-of-band energy, emissions, immunity, high-voltage surges, and safety, including FCC Part 15 and 68, EN55022, EN55024, and many other standards.

5.1. Upgrading from the Si3034/35/44 to Si3056

The Si3056 offers Silicon Laboratories® customers currently using Si3034/35/44 standard serial interface DAA chipsets with an upgrade path for use in new designs. The Si3056 digital interface is similar to the Si3034/35/44 DAAs, thus the Si3056 retains the ability to connect to many widely available DSPs. This also allows customers to leverage software developed for existing Si3034/35/44 designs. More importantly, the Si3056 also offers a number of new features not provided in the Si3034/35/44 DAAs. An overview of the feature differences between the Si3044 and the Si3056 is presented in Table 14. Finally, the globally-compliant Si3056 can be implemented with roughly half the external components required in the already highly integrated Si3034/35/44 DAA application circuits. The following items have changed in the Si3056 as compared to the Si3034/35/44 DAAs:

- The pinout, the application circuit, and the bill of materials. The Si3056 is not pin compatible with Si3034/35/44 DAA chipsets.
- New features have been added to the Si3056 including more ac terminations, a programmable hybrid, finer gain/attenuation step resolution, finer resolution loop current monitoring capability, ring validation, more HW interrupts, a 200 Hz low frequency filter pole. (See the appropriate functional descriptions.)
- The secondary communication data format (see "5.26.Digital Interface" on page 37).
- The low-power sleep mode, and system requirements to support wake-on-ring. (See "5.28.Power Management" on page 39.)

5.2. Line-Side Device Support

Three different line-side devices can be used with the Si3056 system-side device:

- Globally-compliant line-side device—Targets global DAA requirements. Use the Si3018 global line-side device for this configuration. This line-side device supports both FCC-compliant countries and non-FCC-compliant countries.
- Globally-compliant, enhanced features line-side device—Targets embedded and voice applications with global DAA requirements. Use the Si3019 line-side device for this configuration. The Si3019 contains all the features available on the Si3018, plus the following additional features/enhancements:
  - Sixteen selectable ac terminations to increase return loss and trans-hybrid loss performance.
  - Higher transmit and receive level mode.
  - Selectable 200 Hz low frequency pole.
  - –16 to 13.5 dB digital gain/attenuation adjustment in 0.1 dB increments for the transmit and receive paths.
  - Programmable line current/voltage threshold interrupt.
- Globally-compliant, low-speed only line-side device—Targets embedded 2400 bps soft modem applications. Use the Si3010 line-side device for this configuration. The Si3010 contains all the features available on the Si3018, except the transmit and receive paths are optimized and tested only for modem connect rates up to 2400 bps.

Table 14. New Si3056 Features

Chipset	**Si3044**	**Si3056**		
System-Side Part #	**Si3021**			
Line-Side Part #	**Si3015**	**Si3010**	**Si3018**	**Si3019**
Global DAA	Yes	Yes	Yes	Yes
Digital Interface	SSI	SSI	SSI	SSI
Power Supply	3.3 V or 5 V	3.3 V	3.3 V	3.3 V
Max Modem Connect Rate	56 kbps	2400 bps	56 kbps	56 kbps
Data Bus Width	16-bit	16-bit	16-bit	16-bit
Control Register Addressing	6-bit	8-bit	8-bit	8-bit
Max Sampling Frequency	11.025 kHz	16 kHz	16 kHz	16 kHz
AC Terminations	2	4	4	16
Programmable Gain	3 dB steps	3 dB steps	3 dB steps	0.1 dB steps
Loop Current Monitoring	3 mA/bit	1.1 mA/bit	1.1 mA/bit	1.1 mA/bit
Line Voltage Monitoring	2.75 V per bit	1 V per bit	1 V per bit	1 V per bit
Polarity Reversal Detection	Yes (SW polling)	Yes (HW interrupt)	Yes (HW interrupt)	Yes (HW interrupt)
Line I/V Threshold Detection	No	No	No	Yes
Ring Qualification	No	Yes	Yes	Yes
Wake-on-Ring Support	Yes	Yes (MCLK active)	Yes (MCLK active)	Yes (MCLK active)
HW Interrupts	Ring detect only	7 HW interrupts	7 HW interrupts	8 HW interrupts
Integrated Fixed Analog Hybrid	Yes	Yes	Yes	Yes
Programmable Digital Hybrid	No	Yes	Yes	Yes
Full Scale Transmit/Receive Level	+3.2 dBm	0 dBm	0 dBm	+3.2 dBm

Table 15. Country Specific Register Settings

Register	16	31	16	16	26	26	26	30[2]	16[3]	
Country	OHS	OHS2	RZ	RT	ILIM	DCV[1:0]	MINI[1:0]	ACIM[3:0]	ACT	ACT2
Argentina	0	0	0	0	0	11	00	0000	0	0
Australia[4]	1	0	0	0	0	01	01	0011	0	1
Austria	0	1	0	0	1	11	00	0010	0	1
Bahrain	0	1	0	0	1	11	00	0010	0	1
Belgium	0	1	0	0	1	11	00	0010	0	1
Brazil	0	0	0	0	0	11	00	0000	0	0
Bulgaria	0	1	0	0	1	11	00	0011	0	1
Canada	0	0	0	0	0	11	00	0000	0	0
Chile	0	0	0	0	0	11	00	0000	0	0
China[5]	0	0	0	0	0	11	00	0000/1010	0	0
Colombia	0	0	0	0	0	11	00	0000	0	0
Croatia	0	1	0	0	1	11	00	0010	0	1
Cyprus	0	1	0	0	1	11	00	0010	0	1
Czech Republic	0	1	0	0	1	11	00	0010	0	1
Denmark	0	1	0	0	1	11	00	0010	0	1
Ecuador	0	0	0	0	0	11	00	0000	0	0
Egypt	0	1	0	0	1	11	00	0010	0	1
El Salvador	0	0	0	0	0	11	00	0000	0	0
Finland	0	1	0	0	1	11	00	0010	0	1
France	0	1	0	0	1	11	00	0010	0	1
Germany	0	1	0	0	1	11	00	0010	0	1
Greece	0	1	0	0	1	11	00	0010	0	1
Guam	0	0	0	0	0	11	00	0000	0	0
Hong Kong	0	0	0	0	0	11	00	0000	0	0
Hungary	0	1	0	0	1	11	00	0010	0	1
Iceland	0	1	0	0	1	11	00	0010	0	1
India	0	0	0	0	0	11	00	0000	0	0
Indonesia	0	0	0	0	0	11	00	0000	0	0
Ireland	0	1	0	0	1	11	00	0010	0	1
Israel	0	1	0	0	1	11	00	0010	0	1
Italy	0	1	0	0	1	11	00	0010	0	1
Japan	0	0	0	0	0	01	01	0000	0	0
Jordan	0	0	0	0	0	01	01	0000	0	0
Kazakhstan	0	0	0	0	0	11	00	0000	0	0
Kuwait	0	0	0	0	0	11	00	0000	0	0
Latvia	0	1	0	0	1	11	00	0010	0	1

Note:

1. Supported for loop current ≥ 20 mA.
2. Available with Si3019 line-side only.
3. Available with Si3018 and Si3010 line-sides only.
4. See "5.11.DC Termination" on page 27 for DCV and MINI settings.
5. ACIM is 0000 for data applications and 1010 for voice applications.
6. For South Korea, set the TB3 bit in conjunction with the RZ bit. (See Register 59 description.)

Table 15. Country Specific Register Settings (Continued)

Register	16	31	16	16	26	26	26	30[2]	16[3]	
Country	OHS	OHS2	RZ	RT	ILIM	DCV[1:0]	MINI[1:0]	ACIM[3:0]	ACT	ACT2
Lebanon	0	1	0	0	1	11	00	0010	0	1
Luxembourg	0	1	0	0	1	11	00	0010	0	1
Macao	0	0	0	0	0	11	00	0000	0	0
Malaysia[1]	0	0	0	0	0	01	01	0000	0	0
Malta	0	1	0	0	1	11	00	0010	0	1
Mexico	0	0	0	0	0	11	00	0000	0	0
Morocco	0	1	0	0	1	11	00	0010	0	1
Netherlands	0	1	0	0	1	11	00	0010	0	1
New Zealand	0	0	0	0	0	11	00	0100	1	1
Nigeria	0	1	0	0	1	11	00	0010	0	1
Norway	0	1	0	0	1	11	00	0010	0	1
Oman	0	0	0	0	0	01	01	0000	0	0
Pakistan	0	0	0	0	0	01	01	0000	0	0
Peru	0	0	0	0	0	11	00	0000	0	0
Philippines	0	0	0	0	0	01	01	0000	0	0
Poland	0	1	0	0	1	11	00	0010	0	1
Portugal	0	1	0	0	1	11	00	0010	0	1
Romania	0	1	0	0	1	11	00	0010	0	1
Russia	0	0	0	0	0	11	00	0000	0	0
Saudi Arabia	0	0	0	0	0	11	00	0000	0	0
Singapore	0	0	0	0	0	11	00	0000	0	0
Slovakia	0	1	0	0	1	11	00	0010	0	1
Slovenia	0	1	0	0	1	11	00	0010	0	1
South Africa	0	0	1	0	0	11	00	0011	1	0
South Korea[6]	0	0	1	0	0	11	00	0000	0	0
Spain	0	1	0	0	1	11	00	0010	0	1
Sweden	0	1	0	0	1	11	00	0010	0	1
Switzerland	0	1	0	0	1	11	00	0010	0	1
Taiwan	0	0	0	0	0	11	00	0000	0	0
TBR21	0	0	0	0	1	11	00	0010	0	1
Thailand	0	0	0	0	0	01	01	0000	0	0
UAE	0	0	0	0	0	11	00	0000	0	0
United Kingdom	0	1	0	0	1	11	00	0101	0	1
USA	0	0	0	0	0	11	00	0000	0	0
Yemen	0	0	0	0	0	11	00	0000	0	0

Note:

1. Supported for loop current ≥ 20 mA.
2. Available with Si3019 line-side only.
3. Available with Si3018 and Si3010 line-sides only.
4. See "5.11.DC Termination" on page 27 for DCV and MINI settings.
5. ACIM is 0000 for data applications and 1010 for voice applications.
6. For South Korea, set the TB3 bit in conjunction with the RZ bit. (See Register 59 description.)

5.3. Power Supplies

The Si3056 system-side device operates from a 3.0–3.6 V power supply. The Si3056 input pins are 5 V tolerant. The Si3056 output pins only drive 3.3 V. The line-side device derives its power from two sources: The Si3056 and the telephone line. The Si3056 supplies power over the patented isolation link between the two devices, allowing the line-side device to communicate with the Si3056 while on-hook and perform other on-hook functions such as line voltage monitoring. When off-hook, the line-side device also derives power from the line current supplied from the telephone line. This feature is exclusive to DAAs from Silicon Laboratories® and allows the most cost-effective implementation for a DAA while still maintaining robust performance over all line conditions.

5.4. Initialization

When the Si3056 is powered up, assert the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is deasserted, the registers have default values. This reset condition guarantees the line-side device is powered down without the possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined in the following list:

1. Program the PLL with registers 8 and 9 (N[7:0], M[7:0]) to the appropriate divider ratios for the supplied MCLK frequency and the sample rate in register 7 (SRC), as defined in "5.25.Clock Generation" on page 36.
2. Wait 1 ms until the PLL is locked.
3. Write a 00H into Register 6 to power up the line-side device.
4. Set the required line interface parameters (i.e., DCV[1:0], MINI[1:0], ILIM, DCR, ACT and ACT2 or ACIM[3:0], OHS, RT, RZ, ATX[2:0] or TGA2 and TXG2) as defined by “Country Specific Register Settings” shown in Table 15.

When this procedure is complete, the Si3056 is ready for ring detection and off-hook.

5.5. Isolation Barrier

The Si3056 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories® proprietary signal processing techniques. These techniques eliminate signal degradation from capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 17 on page 18, the C1, C2, C8, and C9 capacitors isolate the Si3056 (system-side) from the line-side device. Transmit, receive, control, ring detect, and caller ID data are passed across this barrier. Y2 class capacitors can be used to achieve surge performance of 5 kV or greater.

The capacitive communications link is disabled by default. To enable it, the PDL bit (Register 6, bit 4) must be cleared. No communication between the system-side and line-side can occur until this bit is cleared. The clock generator must be programmed to an acceptable sample rate before clearing the PDL bit.

5.6. Transmit/Receive Full Scale Level (Si3019 Line-Side Only)

The Si3056 supports programmable maximum transmit and receive levels. The default signal level supported by the Si3056 is 0 dBm into a 600 Ω load. Two additional modes of operation offer increased transmit and receive level capability to enable use of the DAA in applications that require higher signal levels. The full scale mode is enabled by setting the FULL bit in Register 31. With FULL = 1, the full scale signal level increases to +3.2 dBm into a 600 Ω load, or 1 dBV into all reference impedances. The enhanced full scale mode (or 2X full scale) is enabled by setting the FULL2 bit in Register 30. Will FULL2 = 1, the full scale signal level increases to +6.0 dBm into a 600 Ω load, or 1.5 dBV into all reference impedances. The full scale and enhanced full scale modes provide the ability to trade off TX power and TX distortion for a peak signal. By using the programmable digital gain registers in conjunction with the enhanced full scale signal level mode, a specific power level (+3.2 dBm for example) could be achieved across all ACT settings.

5.7. Parallel Handset Detection

The Si3056 can detect a parallel handset going off-hook. When the Si3056 is off-hook, the loop current can be monitored with the LCS bits. A significant drop in loop current signals that a parallel handset is going off-hook. If a parallel handset causes the LCS bits to read all 0s, the Drop-Out Detect (DOD) bit can be checked to verify a valid line exists.

The LVS bits can be read to determine the line voltage when on-hook and off-hook. Significant drops in line voltage can signal a parallel handset. For the Si3056 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two off-hook DAAs on the same line. Improved parallel handset operation can be achieved by changing the dc impedance from 50 to 800 Ω and reducing the DCT pin voltage with the DVC[1:0] bits.

5.8. Line Voltage/Loop Current Sensing

The Si3056 can measure loop current and line voltage with the Si3010, Si3018, and the Si3019 line-side devices. The 8-bit LCS2[7:0] and LCS[4:0] registers report loop current. The 8-bit LVS[7:0] register reports line voltage.