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SILICON LABORATORIES

Si2400

V.22BIS ISOMODEM® WITH INTEGRATED GLOBAL DAA

Features

- Data Modem Formats
  - 2400 bps: V.22bis
  - 1200 bps: V.22, V.23, Bell 212A
  - 300 bps: V.21, Bell 103
  - Fast Connect and V.23 Reversing
  - SIA and other security protocols
- Caller ID Detection and Decode
- DTMF Tone Gen./Detection
- 3.3 V or 5.0 V Power
- UART with Flow Control
- Integrated DAA
  - Capacitive Isolation
  - Parallel Phone Detect
  - Globally Compliant Line Interface
  - Overcurrent Detection
- AT Command Set Support
- Integrated Voice Codec
- PCM Data Pass-Through Mode
- HDLC Framing in Hardware
- Call Progress Support
- Pb-Free/RoHS-Compliant Packages Available

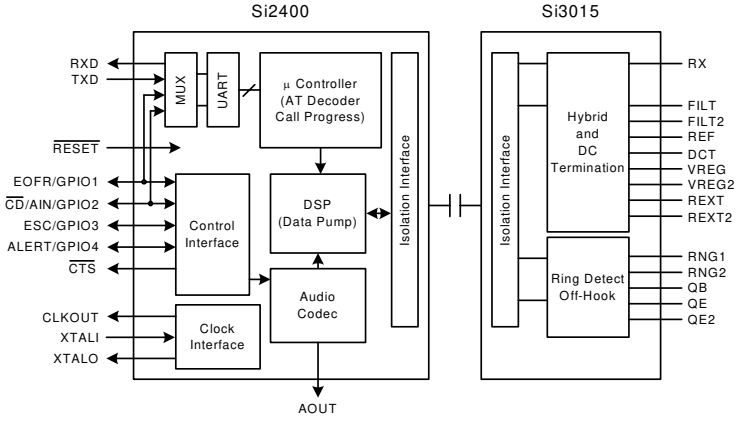
Applications

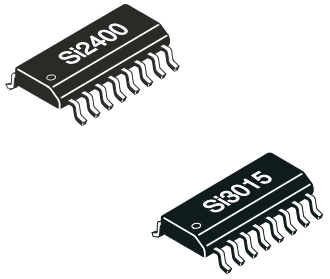
- Set Top Boxes
- Power Meters
- Security Systems
- ATM Terminals
- Medical Monitoring
- Point-of-Sale

Description

The Si2400 ISOmodem® is a complete modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two 16-pin small outline (SOIC) packages, it eliminates the need for a separate DSP data pump, modem controller, analog front end (AFE), isolation transformer, relays, opto-isolators, 2- to 4-wire hybrid, and voice codec. The Si2400 is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance.

Functional Block Diagram



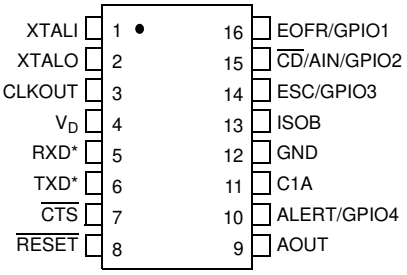


Ordering Information

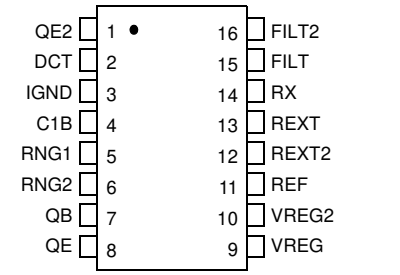
See page 90.

Pin Assignments

Si2400



Si3015



Patents pending

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Section **Page**

SILICON LABORATORIES

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Ambient Temperature	T_A	B-Grade	–40	25	85	°C
Si2400 Supply Voltage, Digital[3]	V_D		3.0	3.3/5.0	5.25	V

Notes:

1. The Si2400 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2400 and any Si3015 are used. See Figure 3 on page 10 for a typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, can operate from either 3.3 V or 5.0 V. The Si2400 interface supports 3.3 V logic when operating from 3.3 V. The 3.3 V operation applies to both the serial port and the digital signals $\overline{CTS}$, CLKOUT, GPIO1–4, and $\overline{RESET}$.

Table 2. Loop Characteristics

(V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade and –40 to 85°C for B-Grade, See Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT[1] = 1_b DCT = 11_b (CTR21)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 42 mA, ACT = 1_b DCT = 11_b (CTR21)	—	—	14.5	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ACT = 1_b DCT = 11_b (CTR21)	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ACT = 1_b DCT = 11_b (CTR21)	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0_b DCT = 01_b (Japan)	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0_b DCT = 01_b (Japan)	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0_b DCT = 10_b (FCC)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0_b DCT = 10_b (FCC)	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 15 mA, ACT = 0_b DCT = 00_b (Low Voltage)	—	—	5.2	V
On Hook Leakage Current[2]	I_{LK}	V_{TR} = –48V	—	—	7	µA
Operating Loop Current	I_{LP}	FCC/Japan Modes	13	—	120	mA
Operating Loop Current	I_{LP}	CTR21 Mode	13	—	60	mA
DC Ring Current[2]		DC current flowing through ring detection circuitry	—	—	7	µA
Ring Detect Voltage[3]	V_{RD}	RT = 0_b	11	—	22	V_{RMS}
Ring Detect Voltage[3]	V_{RD}	RT = 1_b	17	—	33	V_{RMS}
Ring Frequency[4]	F_R		15	—	68	Hz
Ringer Equivalence Number[5]	REN		—	—	0.2	

Notes:

1. SF[4] (ACT); SF5[3:2] (DCT); SF5[0] (RT).
2. R25 and R26 installed.
3. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
4. The Si2400 ring detector can be programmed to detect rings between this range.
5. C15, R14, Z2, and Z3 not installed. SF5[1] (RZ) = 0_b. See "Ringer Impedance" on page 80.

Table 3. DC Characteristics[1]

(V_D = 4.75 to 5.25 V, T_A = 0 to 70°C for K-Grade, T_A = –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.1	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.4	V
Low Level Output Voltage, GPIO1–4	V_{OL}	I_O = 20 mA	—	—	0.6	V
Input Leakage Current	I_L		–10	—	10	µA
CTS Leakage to Ground[2]	I_{CL}		—	10	—	µA
Power Supply Current, Digital[3]	I_D	V_D pin	—	28	32	mA
Power Supply Current, DSP Power Down[3]	I_D	V_D pin	—	16	19	mA
Power Supply Current, Wake-On-Ring (ATZ)	I_D	V_D pin	—	10	11	mA
Power Supply Current, Total Power Down	I_D	V_D pin	—	12	15	µA

1. Measurements are taken with inputs at rails and no loads on outputs.
2. Must be met in order to avoid putting the Si2400 into factory test mode.
3. Specifications assume SE1[7:6] (MCKR) = 00_b (default). Typical value is 4 mA lower when MCKR = 01b and 6 mA lower when MCKR = 10_b.

Table 4. DC Characteristics[1]

(V_D = 3.0 to 3.6 V, T_A = 0 to 70°C for K-Grade, T_A = –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.1	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Low Level Output Voltage, GPIO1–4	V_{OL}	I_O = 15 mA	—	—	0.6	V
Input Leakage Current	I_L		–10	—	10	µA
CTS Leakage to Ground[2]	I_{CL}		—	3	—	µA
Power Supply Current, Digital[3]	I_D	V_D pin	—	15	21	mA
Power Supply Current, DSP Power Down[3]	I_D	V_D pin	—	9	14	mA
Power Supply Current, Wake-On-Ring	I_D	V_D pin	—	5	8	mA
Power Supply Current, Total Power Down	I_D	V_D pin	—	10	12	µA

1. Measurements are taken with inputs at rails and no loads on outputs.
2. Must be met in order to avoid putting the Si2400 into factory test mode.
3. Specifications assume SE1[7:6] (MCKR) = 00_b (default). Typical value is 4 mA lower when MCKR = 01_b and 6 mA lower when MCKR = 10_b.

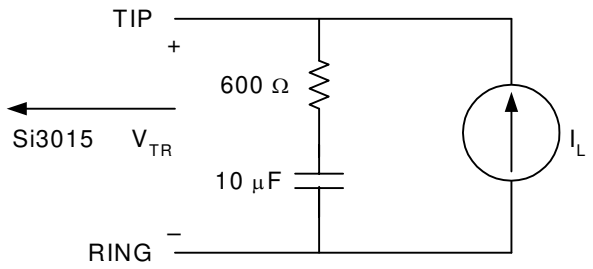


Figure 1. Test Circuit for Loop Characteristics

Table 5. AC Characteristics

(V_D = 3.0 to 3.6 V, or 4.75 to 5.25 V, T_A = 0 to 70°C for K-Grade, T_A = –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		—	9.6	—	KHz
Crystal Oscillator Frequency	F_{XTL}		—	4.9152	—	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[1]	V_{FS}	FULL = 0 (–1 dBm)	—	1	—	V_{PEAK}
		FULL = 1 (+3.2 dBm)[2]	—	1.58	—	V_{PEAK}
Receive Full Scale Level[1]	V_{FS}	FULL = 0 (–1 dBm)	—	1	—	V_{PEAK}
		FULL = 1 (+3.2 dBm)[2]	—	1.58	—	V_{PEAK}
Dynamic Range[3,4,5]	DR	ACT[6] = 0_b, DCT[6] = 10_b (FCC) I_L=100 mA	—	82	—	dB
Dynamic Range[3,4,7]	DR	ACT = 0_b, DCT = 01_b (Japan) I_L = 20 mA	—	83	—	dB
Dynamic Range[3,4,5]	DR	ACT = 1_b, DCT = 11_b (CTR21) I_L = 60 mA	—	84	—	dB
Transmit Total Harmonic Distortion[5,8]	THD	ACT = 0_b, DCT = 10_b (FCC) I_L = 100 mA	—	–85	—	dB
Transmit Total Harmonic Distortion[6,8]	THD	ACT = 0_b, DCT = 01_b (Japan) I_L = 20 mA	—	–76	—	dB
Receive Total Harmonic Distortion[7,8]	THD	ACT = 0_b, DCT = 01_b (Japan) I_L = 20 mA	—	–74	—	dB
Receive Total Harmonic Distortion[5,8]	THD	ACT = 1_b, DCT = 11_b (CTR21) I_L = 60 mA	—	–82	—	dB
Caller ID 60 Hz Common Mode Tolerance[9]	V_{CM}	> 60 dB line balance at 60 Hz	91	120	—	V_{PEAK}

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz.
2. R2 should be changed to a 243 Ω resistor when the SF5[7] (FULL) = 1_b.
3. DR = 20 x log |Vin| + 20 x log (RMS signal/RMS noise).
4. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
5. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
6. ACT = SF5[4]; DCT = SF5[3:2].
7. Vin = 1 kHz, –6 dBFS, Fs = 10300 Hz.
8. THD = 20 x log (RMS distortion/RMS signal).
9. V_{CM} can be improved to 120 V_{rms} minimum by placing a 20 MΩ resistor across the C9 capacitor.

Table 6. Voice Codec AC Characteristics

(V_D = 3.0 to 3.6 V or 4.75 to 5.25 V, T_A = 0 to 70°C for K-Grade, T_A = –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AOUT Dynamic Range, APO = 0		VIN = 1 kHz	—	40	—	dB
AOUT THD, APO = 0		VIN = 1 kHz	—	–40	—	dB
AOUT Full Scale Level, APO = 0			—	0.7 • V_{DD}	—	V_{PP}
AOUT Mute Level, APO = 0			—	60	—	dB
AOUT Dynamic Range, APO = 1, V_D = 4.75 to 5.25 V		VIN = 1 kHz, –3 dB	—	65	—	dB
AOUT Dynamic Range, APO = 1, V_D = 3 to 3.6 V		VIN = 1 kHz, –3 dB	—	65	—	dB
AOUT THD, APO = 1, V_D = 4.75 to 5.25 V		VIN = 1 kHz, –3 dB	—	–60	—	dB
AOUT THD, APO = 1, V_D = 3 to 3.6 V		VIN = 1 kHz, –3 dB	—	–60	—	dB
AOUT Full Scale Level, APO = 1			—	1.5	—	V_{PP}
AOUT Mute Level, APO = 1			—	–65	—	dB
AOUT Resistive Loading, APO = 1			10	—	—	kΩ
AOUT Capacitive Loading, APO = 1			—	—	20	pF
AIN Dynamic Range, V_D = 4.75 to 5.25 V		VIN = 1 kHz, –3 dB	—	65	—	dB
AIN Dynamic Range, V_D = 3 to 3.6 V		VIN = 1 kHz, –3 dB	—	65	—	dB
AIN THD, V_D = 4.75 to 5.25 V		VIN = 1 kHz, –3 dB	—	–60	—	dB
AIN THD, V_D = 3 to 3.6 V		VIN = 1 kHz, –3 dB	—	–60	—	dB
AIN Full Scale Level*			—	2.8	—	V_{PP}

***Note:** Receive full scale level will produce –0.9 dBFS at RXD.

Table 7. Absolute Maximum Ratings

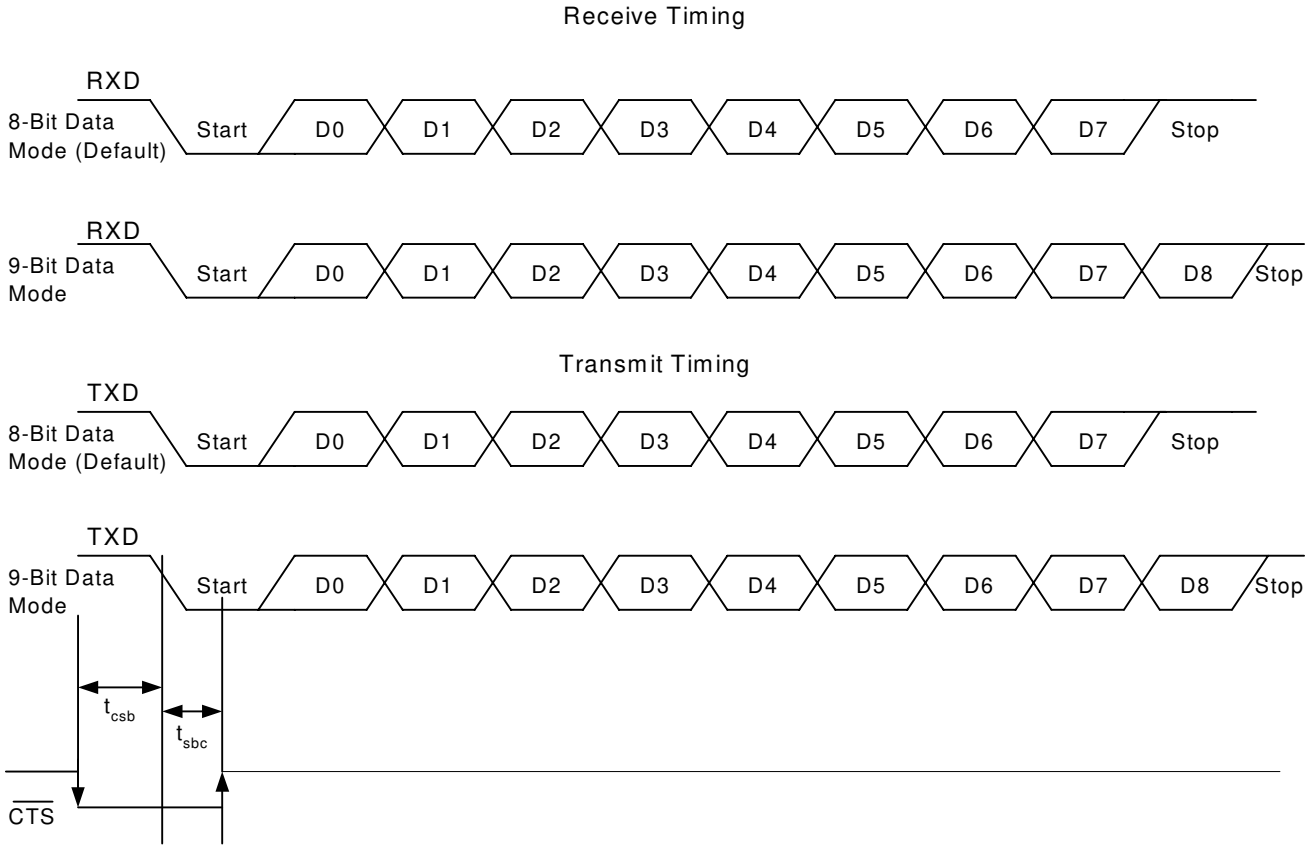
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 6.0	V
Input Current, Si2400 Digital Input Pins	I_{IN}	±10	μA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range—B-Grade	T_A	–50 to 95	°C
Operating Temperature Range—K-Grade	T_A	–10 to 80	°C
Storage Temperature Range	T_{STG}	–40 to 150	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Switching Characteristics

(V_D = 3.0 to 3.6 V or 4.75 to 5.25 V, T_A = 0 to 70°C for K-Grade, T_A = –40 to 85°C for B-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
CLKOUT Output Clock Frequency		2.4576	—	39.3216	MHz
Baud Rate Accuracy	t_{bd}	–1	—	1	%
Start Bit ↓ to $\overline{CTS}$ ↑	t_{sbc}	—	1/(2 • Baud Rate)	—	ns
$\overline{CTS}$ ↓ Active to Start Bit↓	t_{csb}	10	—	—	ns
$\overline{RESET}$ ↓ to $\overline{RESET}$ ↑	t_{rs}	5.0	—	—	ms
$\overline{RESET}$ ↑ Rise Time	t_{rs2}	—	—	100	ns
$\overline{RESET}$ ↑ to TXD ↓	t_{rs3}	3	—	—	ms
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D – 0.4$ V, V_{IL} = 0.4 V					



Note: Baud rates (programmed through register SE0) are as follows: 300,1200, 2400, 9600, 19200, 230400, 245760, and 307200 Hz.

Figure 2. Asynchronous UART Serial Interface Timing Diagram

2. Typical Application Schematic

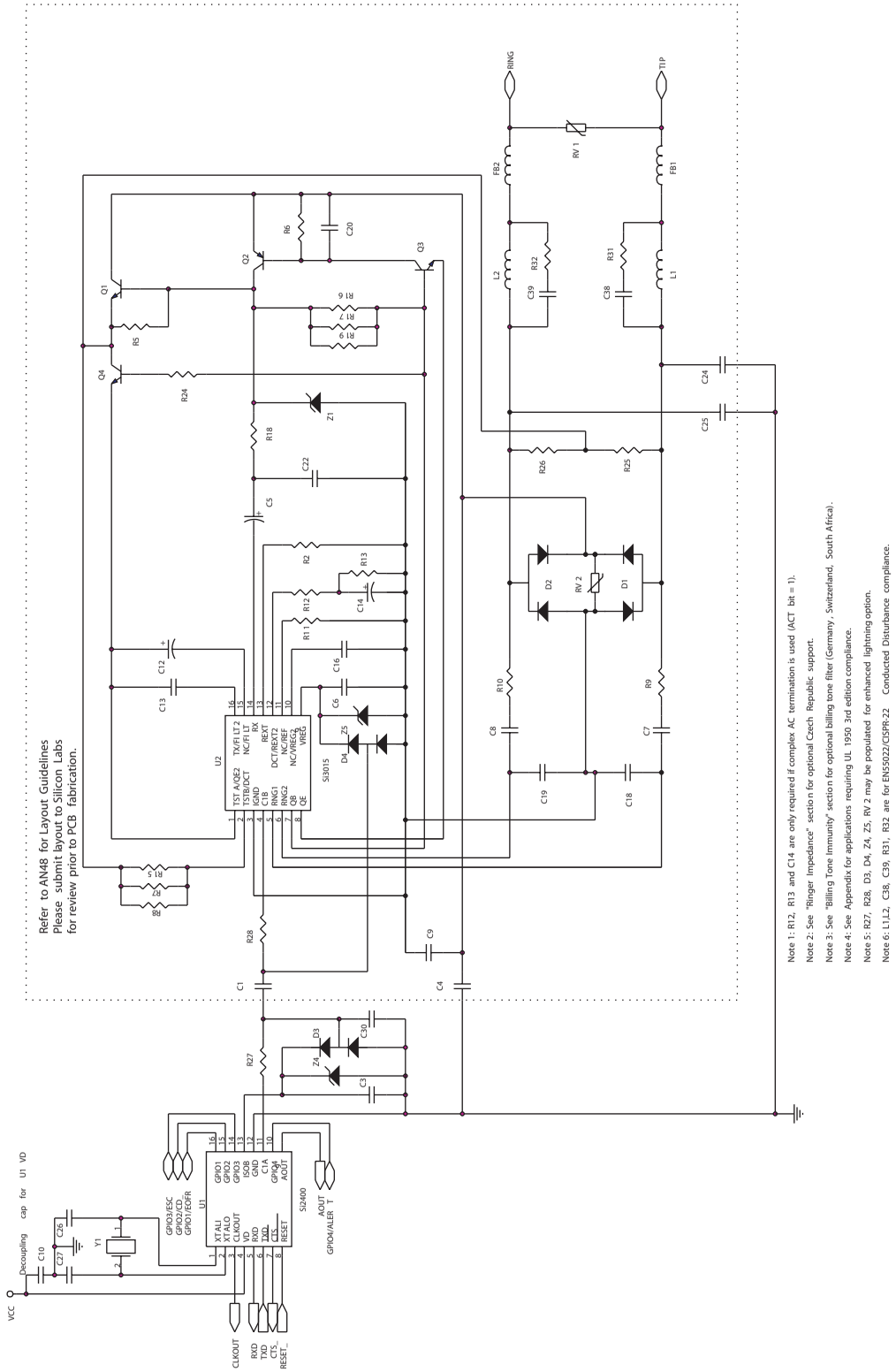


Figure 3. Typical Application Circuit Schematic

3. Bill of Materials

Component	Value	Suppliers
C1,C4[1]	150 pF, 3 kV, X7R,±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C3,C13	0.22 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C5[2]	0.1 µF, 50 V, Elec/Tant, ±20%	Venkel, Johanson, Murata, Panasonic
C6,C10,C16	0.1 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C7,C8[3]	560 pF, 250 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C9	22 nF, 250 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C12	1.0 µF, 16 V, Elec/Tant, ±20%	Venkel, Panasonic
C14[2]	0.68 µF, 16 V, X7R/Elec/Tant, ±20%	Novacap, Venkel, AUX, Murata, Panasonic
C18,C19[3]	3.9 nF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C20	0.01 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C22[4]	1800 pF, 50 V, X7R, ±20%	Not installed
C24,C25[1]	1000 pF, 3 kV, X7R, ±10%	Novacap, Venkel, Johanson, Murata, Panasonic
C26,C27	33 pF, 16 V, NPO, ±5%	Novacap, Venkel, Johanson, Murata
C30[4]	10 pF, 16 V, NPO, ±10%	Not Installed
C38,C39[2,5]	47 pF, 16 V, X7R, ±10%	Venkel
D1,D2[6]	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4[1]	BAV99 Dual Diode, 70 V	Diodes Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead, 600 Ω, ±25%, 200 mA	Murata
L1,L2[2,5]	68 µH, 120 mA, 4 Ω max, ±10%	TDK, Murata, Panasonic
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild, Zetex
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild, Zetex
Q4[7]	BCP56, NPN, 60 V, 1/2 W	OnSemiconductor, Fairchild

Notes:

1. The Si2400 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, Z5 enhanced lightning option increases longitudinal surge survival to greater than 6600 V. The isolation capacitors C1, C4, C24, and C25 must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival and are required for Norway, Sweden, Denmark, and Finland.
2. For FCC-only designs: C14, C38, C39, R12, R13, R31, and R32 are not required; L1 and L2 may be replaced with a short; R2 may be ±5%; with Z1 rated at 18 V, C5 may be rated at 16 V; also see note 9.
3. If the auto answer, ring detect, and caller ID features are not used, R9, R10, C7, C8, C18, and C19 may be removed. In this case, the RNG1 and RNG2 pins of the Si3015 should be connected to the IGND pin.
4. C22 and C30 may provide an additional improvement in emissions/immunity and/or voice performance, depending on design and layout. Population option recommended. See "Emissions/Immunity" on page 78.
5. Compliance with EN55022 and/or CISPR-22 conducted disturbance tests requires L1, L2, C38, C39, R31, R32, and RV2. See also “EN55022 and CISPR-22 Compliance” in Appendix A.
6. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.).
7. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
8. When L1 and L2 are used, RV2 must be installed, and D1 and D2 must be 400 V.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70°C, and capacitive loading.

Component	Value	Suppliers
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2[8]	270 V, MOV	Not Installed
R2[2]	402 Ω, 1/16 W, ±1%	Venkel, Panasonic
R5	100 kΩ, 1/16 W, ±1%	Venkel, Panasonic
R6	120 kΩ, 1/16 W, ±5%	Venkel, Panasonic
R7,R8,R15,R16,R17,R19[9]	5.36 kΩ, 1/4 W, ±1%	Venkel, Panasonic
R9,R10[3]	56 kΩ, 1/10 W, ±5%	Venkel, Panasonic
R11	9.31 kΩ, 1/16 W, ±1%	Venkel, Panasonic
R12[2]	78.7 Ω, 1/16 W, ±1%	Venkel, Panasonic
R13[2]	215 Ω, 1/16 W, ±1%	Venkel, Panasonic
R18	2.2 kΩ, 1/10 W, ±5%	Venkel, Panasonic
R24	150 Ω, 1/16 W, ±5%	Venkel, Panasonic
R25,R26[10]	10 MΩ, 1/16 W, ±5%	Venkel, Panasonic
R27,R28[1]	10 Ω, 1/10 W, ±5%	Venkel, Panasonic
R31,R32[2,5]	470 Ω, 1/16 W, ±5%	Venkel, Panasonic
U1	Si2400	Silicon Labs
U2	Si3015	Silicon Labs
Y1[11]	4.9152 MHz, 20 pF, 50 ppm, 150 ESR	Not Installed
Z1[2]	Zener Diode, 43 V, 1/2 W	Vishay, Motorola, Rohm
Z4,Z5[1]	Zener Diode, 5.6 V, 1/2 W	Vishay, Motorola, Rohm

Notes:

1. The Si2400 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, Z5 enhanced lightning option increases longitudinal surge survival to greater than 6600 V. The isolation capacitors C1, C4, C24, and C25 must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival and are required for Norway, Sweden, Denmark, and Finland.
2. For FCC-only designs: C14, C38, C39, R12, R13, R31, and R32 are not required; L1 and L2 may be replaced with a short; R2 may be ±5%; with Z1 rated at 18 V, C5 may be rated at 16 V; also see note 9.
3. If the auto answer, ring detect, and caller ID features are not used, R9, R10, C7, C8, C18, and C19 may be removed. In this case, the RNG1 and RNG2 pins of the Si3015 should be connected to the IGND pin.
4. C22 and C30 may provide an additional improvement in emissions/immunity and/or voice performance, depending on design and layout. Population option recommended. See "Emissions/Immunity" on page 78.
5. Compliance with EN55022 and/or CISPR-22 conducted disturbance tests requires L1, L2, C38, C39, R31, R32, and RV2. See also “EN55022 and CISPR-22 Compliance” in Appendix A.
6. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.).
7. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
8. When L1 and L2 are used, RV2 must be installed, and D1 and D2 must be 400 V.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70°C, and capacitive loading.

4. Analog Input/Output

Figure 4 illustrates an optional application circuit to support the analog output capability of the Si2400 for voice monitoring purposes.

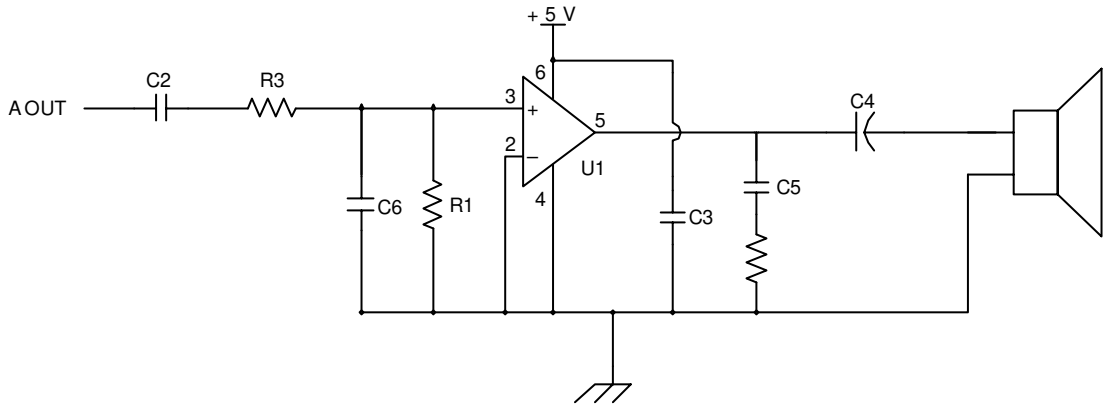


Figure 4. Optional Connection to AOUT for a Monitoring Speaker

Table 9. Component Values—Optional Connection to AOUT

Symbol	Value
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	10 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/10 W, ±5%
U1	LM386

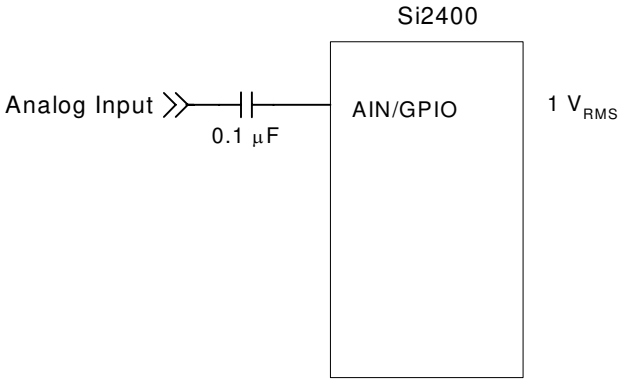


Figure 5. Analog Input Circuit

5. Functional Description

The Si2400 ISOmodem is a complete modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two 16-pin small outline packages, this solution includes a DSP data pump, a modem controller, an analog front end (AFE), a DAA, and an audio codec.

The modem, which accepts simple modem AT commands, provides connect rates of up to 2400 bps, full-duplex over the Public Switched Telephone Network (PSTN) with V.42 hardware support through HDLC framing. To minimize handshake times, the Si2400 can implement a V.25-based fast connect. The modem also supports the V.23 reversing protocol and standard alarm formats including SIA.

The Si2400 ISOmodem provides numerous features for embedded modem applications including caller ID detection and decoding for the US, UK, and Japanese caller ID formats. Both DTMF decoding and generation are provided on chip as well. Call progress is supported both at a high level through echoing result codes and at a low level through user-programmable biquad filters and parameters such as ring period, ring on/off time, and dialing interdigit time.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2400 solution integrates a silicon DAA using Silicon Laboratories' proprietary capacitive isolation technology. This highly integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. The DAA also can monitor line status for parallel handset detection and for overcurrent conditions.

The Si2400 is designed for rapid assimilation into existing modem applications. The device interfaces directly through a UART to a microcontroller. The Si2400URT-EVB connects directly to a standard RS-232 interface. This allows for PC evaluation of the modem immediately upon powerup via HyperTerminal or any standard terminal software.

The chipset can be fully programmed to meet international telephone line interface requirements with full compliance to FCC, CTR21, JATE, and other country-specific PTT specifications. In addition, the Si2400 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The Si2400 solution needs only a few low-cost discrete components to achieve global compliance. See Figure 3 on page 10 for a typical application circuit.

Table 10. Selectable Configurations

Configuration	Modulation	Carrier Frequency (Hz)	Data Rate (bps)	Standard Compliance
V.21	FSK	1080/1750	300	Full
V.22[1]	DPSK	1200/2400	1200	Full
V.22bis[1,2]	QAM	1200/2400	2400	No retrain
V.23	FSK	1300/2100	1200/75	Full; plus reversing (Europe)
V.23		1300/1700	600/75	
Bell 103	FSK	1170/2125	300	Full
Bell 212A	DPSK	1200/2400	1200	Full
Security	DTMF	—	40	Full
SIA—Pulse	Pulse	—	Low	Full
SIA Format	FSK	1170/2125	300 half-duplex	300 bps only

Notes:

1. The V.22 and V.22bis standards refer to V.14 DTE (UART) configurations. The Si2400 does not support V.14 breaks. In order to support overspeeding by the remote modem, the Si2400 DTE speed must be greater than the modem (line) data rate.
2. The Si2400 only adjusts its DCE rate from 2400 bps to 1200 bps if it is connecting to a V.22-only (1200 bps only) modem. Because the V.22bis specification does not outline a fallback procedure, the host should implement a fallback mechanism consisting of hanging up and connecting at a lower baud rate. Retraining to accommodate changes in line conditions which occur during a call must be implemented by terminating the call and redialing.

5.1. Digital Interface

The Si2400 has a universal asynchronous serial interface (UART) compatible with standard microcontroller serial interfaces. After power-up or reset, the speed of the serial (Data Terminal Equipment—DTE) interface is set by default to 2400 bps with the 8-bit, no parity, and one stop bit (8N1) format described below. The PCM codec serial interface is disabled by default and CLKOUT is set to 9.8304 MHz after power-up or reset.

The serial interface DTE rate can be modified by writing SE0[2:0] (SD) with the value corresponding to the desired DTE rate. (See Table 11.) This is accomplished with the command ATSE0=xx where xx is the hexadecimal value of the SE0 register.

Table 11. DTE Rates

DTE Rate (bps)	SE0[2:0] (SD)
300	000
1200	001
2400	010
9600	011
19200	100
228613	101
245760	110
307200	111

Immediately after the ATSE0=xx string is sent, the host UART must be reprogrammed to the new DTE rate in order to communicate with the Si2400.

The three highest DTE rates (228613, 245760, 307200) are required for transferring PCM data from the host to the Si2400 PCM interface for the transmission of voice over the phone line or through the voice codec.

Table 12. Modem Configuration Examples (S07[7] (HDEN) = 0, S07[6] (BD) = 0)

Modem Protocol	Register S07 Values
V.22bis	0x06
V.22	0x02
V.21	0x03
Bell 212A	0x00
Bell 103	0x01
V.23 (1200 tx, 75 rx)	0x16
V.23 (75 tx, 1200 rx)	0x24
V.23 (600 tx, 75 rx)	0x12
V.23 (75 tx, 600 rx)	0x20

5.2. Configurations and Data Rates

The Si2400 can be configured to any of the Bell and CCITT operation modes in Table 12. The modem, when configured for V.22bis, will connect at 1200 bps if the far end modem is configured for V.22. This device also supports SIA and other protocols for the security industry. Table 10 provides the modulation method, carrier frequencies, data rate, baud rate and notes on standard compliance for each modem configuration of the Si2400. Table 12 shows example register settings (S07) for some of the modem configurations.

As shown in Figure 6, 8-bit and 9-bit data modes refer to the DTE format over the UART. Line data formats are configured through registers S07 (MF1) and S15 (MLC). If the number of bits specified by the DTE format differs from the number of bits specified by the DCE (Data Communications Equipment or Line) format, the MSBs will either be dropped or bit-stuffed, as appropriate. For example, if the DTE format is 9 data bits (9N1), and the line data format is 8 data bits (8N1), then the MSB from the DTE will be dropped as the 9-bit word is passed from the DTE side to the DCE (line) side. In this case, the dropped ninth bit can then be used as an escape mechanism. However, if the DTE format is 8N1and the line data format is 9N1, an MSB equal to 0 will be added to the 8-bit word as it is passed from the DTE side to the DCE side.

The Si2400 UART does not continuously check for stop bits on the incoming digital data. Therefore, if the TXD pin is not high, the RXD pin may echo meaningless characters to the host UART. This requires the host UART to flush its receiver FIFO upon initialization.

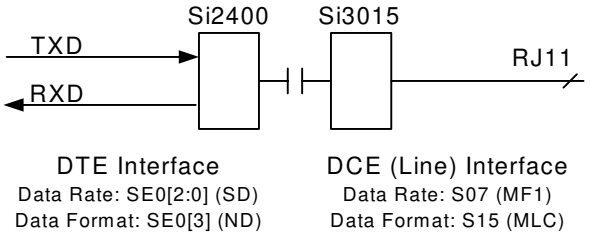


Figure 6. Link and Line Data Formats

5.2.1. Command/Data Mode

Upon reset, the modem will be in command mode and will accept AT-style commands. An outgoing modem call can be made using the “ATDT#” (tone dial) or “ATDP#” (pulse dial) command after the device is configured. If the handshake is successful, the modem will respond with the “c”, “d”, or “v” string and enter data mode. (The byte following the “c”, “d”, or “v” will be the first data byte.) At this point, AT-style commands are not accepted. There are three methods which may be used to return the Si2400 to command mode:

- Use the ESC pin—To program the GPIO3 pin to function as an ESCAPE input, set GPIO3 SE2[5:4] = 11b. In this setting, a positive edge detected on this pin will return the modem to command mode. The “ATO” string can be used to re-enter data mode.
- Use 9-bit data mode—If 9-bit data format with escape is programmed, a 1 detected on bit 9 will return the modem to command mode. (See Figure 2 on page 9.) This is enabled by setting SE0[3] (ND) = 1_b and S15[0] (NBE) = 1_b. The ATO string can be used to reenter data mode. Ninth bit escape does not work in the security modes.
- Use TIES—The time independent escape sequence is a sequence of three escape characters (“+” characters by default). Once these characters have been recognized, the modem enters the Command state without sending a confirming result code to the terminal. The modem then starts an internal prompt delay timer. From that point on if an AT<CR> (attention) command is received before the timer expires, the timer is stopped and the “O” response code is sent to the terminal. This indicates that the Si2400 is in command mode.
  If any other data is received while the timer is running, the timer is stopped, the device returns to the online state, and the data appearing on TXD is sent to the remote modem.
  If the timer expires, a confirming “O” response code is sent to the terminal indicating that the modem is in command mode.
  TIES is enabled by writing register S14[5] (TEO) = 1_b. Both the escape character “+” and the escape time-out period are programmable via registers S0F (TEC) and S10 (TDT), respectively.

Note: TIES is not the recommended escape solution for the most robust designs. Any data string containing the sequence “+++AT<CR>” will interrupt a data sequence erroneously.

Whether using an escape method or not, when the carrier is lost, the modem will automatically return to command mode and report “N”.

5.2.2. 8-Bit Data Mode (8N1)

The 8-bit data mode is the default mode after power-up or a reset and is set by SE0[3] (ND) = 0_b. It is asynchronous, full duplex, and uses a total of 10 bits including a start bit (logic 0), 8 data bits, and a stop bit (logic 1). Data received from the remote modem is transferred from the Si2400 to the host on the RXD pin. Data transfer to the host begins when the Si2400 asserts a logic 0 start bit on RXD. Data is shifted out of the Si2400 LSB first at the DTE rate determined by the SE0[2:0] (SD) setting and terminates with a stop bit. Data from the host for transmission to the remote modem is shifted to the Si2400 on TXD, beginning with a start bit, LSB first at the DTE rate determined by the SE0[2:0] setting and terminates with a stop bit. After the middle of the stop bit time the Si2400 will begin looking for a logic 1 to logic 0 transition signaling the start of the next character on TXD to be sent to the line (remote modem).

5.2.3. 9-Bit Data Mode (9N1)

The 9-bit data mode is set by SE0[3] (ND) = 1_b. It is asynchronous, full duplex, and uses a total of 11 bits including a start bit (logic 0), 9 data bits, and a stop bit (logic 1). Data received from the line (remote modem) is transferred from the Si2400 to the host on the RXD pin. Data transfer to the host begins when the Si2400 asserts a logic 0 start bit on RXD. Data is shifted out of the Si2400 LSB first at the DTE rate determined by the SE0[2:0] (SD) setting and terminates with a stop bit. Data from the host for transmission to the line (remote modem) is shifted to the Si2400 on TXD, beginning with a start bit, LSB first at the DTE rate determined by the S-Register SE0[2:0] (SD) setting and terminates with a stop bit. After the middle of the stop bit time the Si2400 will begin looking for a logic 1 to logic 0 transition signaling the start of the next character on TXD to be sent to the line (remote modem).

The ninth data bit may be used to indicate an escape by setting S15[0] (NBE) = 1_b. In this mode, the ninth data bit will normally be set to 0 when the modem is online. When the ninth data bit is set to 1, the modem will go offline into Command mode and the next frame will be interpreted as an AT command. Data mode can be reentered using the ATO command.

5.2.4. Flow Control

No flow control is needed if the DTE rate and DCE rate are the same. If the serial link (DTE) data rate is set higher than the line (DCE) rate of the modem, flow control is required to prevent loss of data to the transmitter.

To control data flow, the clear-to-send ($\overline{\text{CTS}}$) pin is used. As shown in Figure 2 on page 9, the $\overline{\text{CTS}}$ pin will normally be high, and will be low whenever the modem is able to accept new data. The $\overline{\text{CTS}}$ pin will go high again as soon as a start bit is detected on the TXD pin and will remain high until the modem is ready to accept another character.

5.3. Low Power Modes

The Si2400 has three low power modes. These are described below:

- DSP Powerdown. The DSP processor can be powered down by setting register SEB[3] (PDDE) = 1_b.
  In this mode, the serial interface still functions and the modem will detect ringing and intrusion. However, no modem modes or tone detection features will function.
- Wake-Up-On-Ring. By issuing the ATz command, the Si2400 goes into a low power mode where both the microcontroller and DSP are powered down. Only an incoming ring or a total reset will power up the chip again. Return from wake-on-ring will trigger the ALERT pin if S62[4] (WOR) = 1_b (WOR = 0_b by default).
- Total Powerdown. Setting SF1[5] = 1_b and SF1[6] = 1_b will place the Si2400 into a total powerdown mode. All logic is powered down, including the crystal oscillator and clock-out pin. Only a hardware reset can restart the Si2400.

5.4. Global DAA Operation

The Si2400 chipset contains an integrated silicon direct access arrangement (silicon DAA) that provides a programmable line interface to meet international telephone line requirements. Table 13 gives the DAA register settings required to meet various country PTT standards. A detailed description of the registers in Table 13 can be found in "Appendix A—DAA Operation" on page 78.

Table 13. Country-Specific Register Settings

Register	SF5					SF7	SF6		S62
Country	**OHS**	**ACT**	**DCT**	**RZ**	**RT**	**LIM**	**VOL**	**FLVM**	**LLC**
Australia[1]	1	1	01	0	0	0	0	0	0
Brazil[2]	0	0	01	0	0	0	0	0	0
CTR21[1, 3, 4]	0	1	10	0	0	1	0	0	1
Czech Republic	0	1	10	0	0	0	0	0	0
FCC[1, 5]	**0**	**0**	**10**	**0**	**0**	**0**	**0**	**0**	**0**
Latvia	0	1	11	0	0	1	0	0	0
Malaysia[1,6]	0	0	01	0	0	0	0	0	0
New Zealand	0	1	10	0	0	0	0	0	0
Nigeria	0	1	11	0	0	1	0	0	0
Philippines[1]	0	0	01	0	0	0	0	1	0
Poland[7], Slovenia	0	0	10	1	1	0	0	0	0
South Africa[7]	1	0	10	1	0	0	0	0	0
South Korea[7]	0	0	01	1	0	0	0	0	0

Note:

1. See "DC Termination" on page 79 for more information.
2. The following countries require the same settings as Brazil: Armenia, China, Egypt, Georgia, Japan, Jordan, Kazakhstan, Kyrgyzstan, Malaysia, Muldova, Oman, Pakistan, Qatar, Russia, Syria, Taiwan, Thailand, Ukraine.
3. The following countries require the same settings as CTR21: Austria, Bahrain, Belgium, Bulgaria, Croatia, Cyprus, Denmark, Estonia, European Union, Finland, France, Germany, Greece, Guadeloupe, Iceland, Ireland, Israel, Italy, Lebanon, Liechtenstein, Luxembourg, Malta, Martinique, Morocco, Netherlands, Norway, Polynesia (French), Portugal, Reunion, Spain, Sweden, Switzerland, Turkey, and the United Kingdom.
4. When changing into or out of CTR21 Mode, LLC should be written first. SDF must be enabled (i.e., DGSR $\neq$ 0) and SFS should be reprogrammed before each call.
5. The following countries require the same settings as FCC: Argentina, Brunei, Canada, Chile, Columbia, Dubai, Equador, El Salvador, Guam, Hong Kong, Hungary, India, Indonesia, Kuwait, Macao, Mexico, Peru, Puerto Rico, Romania, Saudi Arabia, Singapore, Slovakia, Tunisia, UAE, USA, Venezuela, Yemen.
6. Supported for loop current $\geq$ 20 mA.
7. SF5[1] (RZ) should only be set for Poland, South Africa and South Korea if the ringer impedance network (C15, R14, Z2, Z3) is not populated.

5.5. Parallel Phone Detection

The Si2400 has the ability to detect a phone or other device that is off hook on a shared line. This enables the ISOmodem to avoid interrupting a call in progress on a shared line and to intelligently handle an interruption by another device when the Si2400 is using the line. An automatic algorithm to detect parallel phone intrusion (defined as an off-hook parallel handset) is provided by default.

5.5.1. On-Hook Intrusion Detection

To implement intrusion detection, the Si2400 uses loop voltage sense register SDB (LVCS). When on hook, LVCS monitors the line voltage. (When off-hook, it measures line current.) LVCS has a full scale of 87 V with an LSB of 2.75 V. The first code (0 → 1) is skewed such that a 0 indicates that the line voltage is < 3.0 V. The voltage accuracy of LVCS is ±20%. The user can read these bits directly when on hook through register SDB (LVCS).

The automatic on-hook detector algorithm can be tripped by either an absolute level or by a voltage differential by selecting S13[3] (ONHD) = 0_b for absolute or S13[3] (ONHD) = 1_b for differential. If the absolute detector is chosen, the Si2400 algorithm will detect an intrusion if LVCS is less than the value stored in on-hook intrusion threshold, S11[4:0] (AVL). In other words, an intrusion has occurred if LVCS < AVL.

AVL defaults to 1000_b, or 25 V on powerup. The absolute detector is the correct method to use for most countries and should also be used to detect the presence (or absence) of a line connection.

Under the condition of a very short line and a current-limiting telephone off hook, the off-hook line voltage can be as high as 40 V. The minimum on-hook voltage may not be much greater. This condition can occur on phone lines with current-limiting specifications such as France. For these lines, a differential detector is more appropriate.

The differential detector method checks line status every 26.66 ms. The detector compares (LVCS (t – 0.02666) – LVCS (t)) to the differential threshold level set in register S11[7:5] (DVL). The default for DVL is 0x02 (5.5 V). If the threshold is exceeded (LVCS (t – 0.02666) – LVCS (t) > DVL), an intrusion is detected. If (LVCS (t) – LVCS (t – 0.02666) > DVL), then the intrusion is said to have terminated.

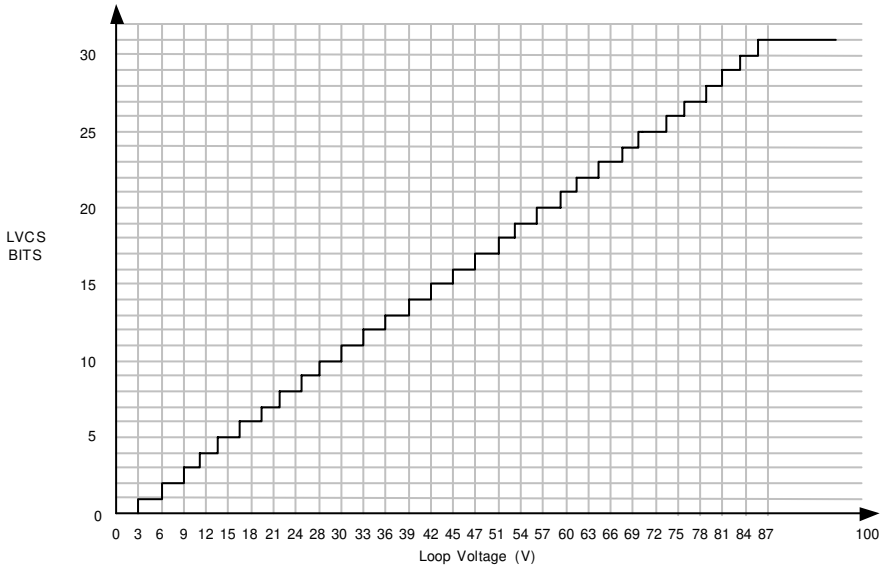


Figure 7. Loop Voltage—LVCS Transfer Function

5.5.2. Reporting of an On-Hook Intrusion

The reporting of an on-hook intrusion is the same whether or not the differential or absolute algorithm is chosen.

An “i” result code is sent when an intrusion is detected. Conversely an “I” result code is sent when an intrusion has terminated. S14[1] (IND) indicates the current intrusion status and is set for as long as an intrusion is detected.

In addition, if the LVCS returns a value of zero, an “l” result code is sent to the host. If the LVCS becomes non-zero after having gone to zero, an “L” result code is sent to the host. S14[2] (NLD) indicates the current line voltage status and is set for as long as the LVCS is zero.

It is possible to suppress the result codes by setting S14[7] MRCD = 1_b and selectively re-enabling desired result codes using the S62 register. Suppressing result codes in this fashion does not affect the setting of the NLD and IND bits of the S14 register. Suppressing the result codes is the best approach if polling the S14 register to monitor the intrusion status is preferred.

It is also possible to suppress the result codes by setting S33[6] (DON). However, this approach will stop the updating of the S14 register, rendering the on-hook intrusion algorithm completely disabled. This approach may be used if the host checks LVCS directly prior to going off-hook.

5.5.3. Off-Hook Intrusion Detection

When the Si2400 is off-hook, it can detect another phone going off-hook by monitoring the dc loop current. The loop current sense transfer function is shown in Figure 8 with the upper curve representing CTR21 (current limiting) operation and the lower curve representing all other modes. The overload points indicate excessive current draw. The user can read these bits directly through SDB (LVCS). Note that as in the line voltage sense, there is hysteresis between codes (0.375 mA for CTR21 mode and 0.75 mA for the alternate mode).

The off-hook intrusion algorithm does not begin to operate immediately after going off-hook. This is to avoid triggering an off-hook intrusion interrupt due to off-hook transients. The time between going off-hook and enabling the intrusion algorithm defaults to 1 second and may be set via S82[7:4] (IST).

Once the intrusion settling time (IST) has elapsed, the Si2400 executes one of the three off-hook intrusion algorithms, depending on the settings of SDF[6:0] (DSGR) and S13[4] (OFHD). See Table 14.

Table 14. Off-Hook Intrusion Algorithms

Algorithm	OFHD	SDF
Differential #1	1	0
Differential #2	1	≠0
Absolute	0	x

5.5.4. Differential Algorithm #1 (default)

If (LVCS (t – 800 ms) – LVCS (t)) > S12[7:5] (DCL), then an intrusion is deemed to have taken place. If (LVCS (t) – LVCS (t – 800 ms)) > DCL, then the intrusion is deemed to have completed. Default DCL is 2. This comparison occurs every 200 ms.

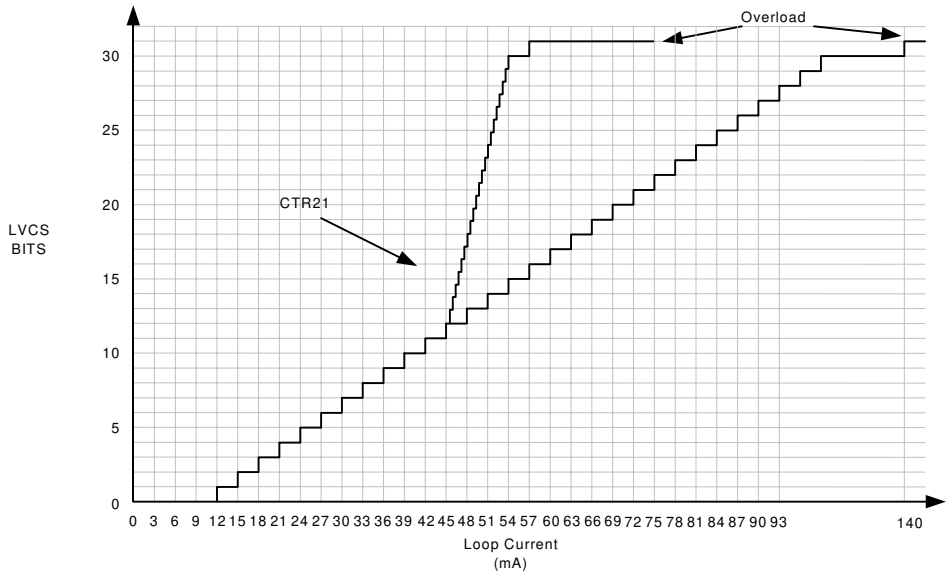


Figure 8. Loop Current—LVCS Transfer Function

5.5.5. Differential Algorithm #2

This differential algorithm has features added to Differential Algorithm #1. The additional features are as follows:

- Programmable deglitch filter to minimize false intrusions
- Ability to preset initial LVCS reference prior to going off-hook
- Optional time window where intrusions are blocked and ignored

5.5.6. Deglitch Filter

To avoid triggering an off-hook intrusion interrupt due to a transient or glitch on the telephone line, a deglitch filter is inserted before the off-hook intrusion algorithm. The sample rate of the deglitcher is set by SDF[6:0] (DGSR). (If DGSR = 0, the Differential Algorithm #1 is implemented.) Before a sample is passed to the off-hook intrusion algorithm, it must be confirmed by a subsequent sample of the same value. Otherwise, it is not submitted to the off-hook algorithm.

In order to filter out glitches of up to 1 second in duration, for example, DGSR should be set to 1 second (SDF[6:0] = 011001b). In this example, an intrusion event that lasts for more than two seconds is guaranteed to be treated as a real intrusion. Intrusion events between one second and two seconds in duration may or may not be treated as an intrusion. The recommended setting for DGSR is one second, which should work for most applications.

Once a sample has been deemed valid by the deglitch filter, the off-hook algorithm operates as follows:

If (LVCS (t – 80 ms • DGSR) – LVCS (t)) > DCL, then an intrusion is deemed to have taken place. Default DCL is 2. This comparison occurs every 40 ms • DGSR. Because the compared value is continually updated, the off-hook intrusion algorithm automatically adjusts to account for drift in line resistance.

5.5.7. LVCS Initialization

If an intrusion begins within the time window defined by S82[7:4] (IST), it is possible for an intrusion to go unreported because the initial LVCS used as the reference is sampled after the intrusion has begun.

S12[4:0] (ACL) is used to avoid this problem. Prior to going off-hook, the host can set the ACL register to a known value of LVCS with the Si2400 off-hook and all parallel phones or other devices on-hook. If this value is not known, such as on the first off-hook event using this specific phone line, ACL should be set to 0, indicating no known LVCS reference.

Once the Si2400 goes back on-hook, it automatically writes the value of the last known LVCS sample prior to an intrusion, if any, into ACL. Therefore, ACL may be used for the next off-hook event even if the current off-hook sample contains an intrusion. Except for the first initialization, no host intervention is necessary.

The Si2400 clears ACL automatically under a hardware reset. Additionally, ACL is cleared if the modem is on-hook, and the phone line is disconnected and then reconnected once again.

If the host hardware resets the Si2400 between off-hook events, the host may choose to store the ACL value prior to reset, and then restore this value to ACL prior to the next off-hook event.

5.5.8. Intrusion Blocking

Differential Algorithm #2 may be disabled for a period of time after dialing begins. This can avoid triggering an off-hook intrusion interrupt due to pulse dialing or line transients from central office switching. The method to block the intrusion algorithm is set via S82[1:0] (IB). If IB = 10b is chosen, S29 (IS) can be used to set this blocking to an absolute time.

In order to detect if an intrusion does occur during blocking and is sustained until after the blocking, the Si2400 will measure the difference in LVCS between the sample before blocking and the sample after blocking.

5.5.9. Absolute Algorithm

If the absolute detector is chosen (S13[4] [OFHD] = 0_b), the Si2400 will detect an intrusion under the condition that LVCS is less than the off-hook intrusion threshold, S12[4:0] (ACL). In other words, it is determined that an intrusion has occurred if LVCS < ACL. ACL defaults to 0 (12 mA) on powerup. Because the loop current can vary from 20 mA to 100 mA, depending on the line, a factory preset threshold is not useful.

To use this absolute mode, the host must measure the line current and set the threshold accordingly. A measurement of the loop current is accomplished by going off-hook (issuing the “ATDT;” command), reading LVCS after 800 ms, and going back on hook using the “ATH” command. This measured value of LVCS should be used to determine the threshold register ACL. If this method is used, the loop current should be measured on a periodic basis to account for drift in line resistance.

5.5.10. Reporting Off-Hook Intrusions

The primary method of reporting an off-hook intrusion event to the host is through the use of the ALERT pin. The ALERT function is assigned to GPIO4 by setting SE2[7:6] (GPIO4) = 11b.

In general, “i” and “I” result codes are sent when the modem detects an intrusion. However, it is important to note that these result codes are not always reported. When the modem is in the data mode, the “i” and “I”

result codes are suppressed, and the ALERT pin is the only method of reporting an intrusion to the host.

The "i" and "I" result codes may be sent to the host under the following conditions:

1. If the modem is in the process of establishing a connection using the "ATDT#<cr>" or "ATA<cr>" commands and prior to the "c", "v", or "d" result codes.
2. If the modem is in command mode and a call is initiated using "ATDT#;" command.
3. If the modem is used in the security modes (ATDT#!0-!7) (except !2).
4. If the modem is used in the !2 security mode while the modem is not actively receiving/sending FSK data.

Once the ALERT pin is asserted as a consequence of an intrusion, it is the responsibility of the host software to negate it by clearing SE3[3] (GPD4) directly.

S14[1] (IND) is an indication of the current intrusion status. It is updated whenever the "i" and "I" result codes are sent to the host or when the ALERT pin is asserted. If set, IND indicates that an intrusion event is in progress. In addition, the status of IND persists for 800 msec after an off hook to on-hook event. After 800 msec has elapsed, IND functions as documented for the on-hook intrusion algorithm. This delay preserves the S14 register contents at the time the ALERT is asserted.

When using the modem as a standard data modem and the ALERT pin asserts, the host software may need to force the modem back into command mode. In the command mode, the host can determine if the ALERT assertion was caused by an intrusion or a carrier loss by querying the S14 register.

If the modem is dialing (after the ATDT string but before the "c", "v", or "d" result codes), sending any character places the modem back into command mode. In the case in which the modem has already connected (in data mode after the "c", "v" or "d" result code has been sent), an escape sequence is required to place the modem in the command mode.

The best method of regaining control, without having to know the exact status of the modem, is by issuing an escape sequence (asserting the ESC pin and waiting a short period of time) and sending a carriage return character. The escape sequence takes care of the case in which the modem is in the connected state, and the carriage return character aborts the dialing if the modem is in the process of dialing to get a connection. If the modem is already on-hook and in command mode, the carriage return character and escape sequence are benign events.

5.6. Loop Current Detection

In addition to monitoring parallel phone intrusion, it is possible to monitor the loss of loop current. This feature can be enabled by setting SE82[3] (LCLD) = 1. This feature is disabled by default. If the loop current is too low for normal DAA operation, the "l" result code is sent, and S14[2] (NLD) is set. Once the loop current returns to a normal current state, the "L" result code is sent and S14[2] (NLD) is cleared. The ALERT pin is also asserted if enabled. The "L" and "l" result codes are not always sent. The principles governing the reporting of the "i" and "I" result codes apply to the "L" and "l" result codes. The status of the S14 register is unchanged for 800 msec after an off-hook to on-hook event. This delay preserves the S14 register contents at the time the ALERT is asserted.

5.7. Carrier Detect/Loss

The Si2400 can provide the functionality of a loss-of-carrier pin similar to the CD pin functionality in an RS-232 connection. If programmed as an ALERT, GPIO4 will go high in data mode when either parallel phone intrusion or a loss-of-carrier is detected. When used in this manner, the host detects a low-to-high transition on GPIO4 (ALERT), escapes into command mode, and reads S14[1] (IND). If high, IND indicates intrusion. If low, IND indicates loss-of-carrier.

A carrier detect function may also be implemented by setting SE2[3:2] (GPIO2) = 01b, SE4[0] (TRSP) = 0_b, and SOC[7] (CDE) = 1_b.

If the Si2400 does not reliably detect loss of carrier, use the following AT command string:

ATSE8=00SE6=00SE5=25SE8=01SE6=0ASE5=3DSE8=00

This moves the carrier-off level to within 0.5 dB of the carrier-on level. (The default is 2.5 dB.) This reduces the likelihood that the Si2400 will detect its own output as a remote modem carrier.

5.8. Overcurrent Detection

The Si2400 will always go off hook with the current-limiting mode enabled. This allows no possibility of damage for voltages up to about 48 V. However, at higher voltages the 43 V Zener protection device will begin to conduct and could be damaged if the power is applied for too long.

The Si2400 will detect the value of the loop current at a programmable time set by S32 (OCDT) after going off-hook (default = 20 ms). If the loop current is too high, an "x" will be echoed back to the host to indicate a fault condition. The host may then check S14[3] (OD) to confirm an overcurrent condition.

The user can optionally put the Si2400 into a lower drive

mode, which is similar to the current-limiting mode but has reduced hookswitch drive. This feature allows the Si2400 to remain off-hook on a digital line for a longer period of time without damage. If the Si2400 does not detect overcurrent after the time set by S32 (OCDT), the correct line termination is applied. Another option is setting S13[5] (OFHE) = 1_b. When this bit is set, the Si3015 is forced to CTR21 termination during the short period of time from the off-hook event until the timeout defined by OCDT. After the OCDT timeout, the desired dc termination is restored.

If it is determined that a false overcurrent condition has been detected, the host may choose to set S62[6] (OCR) = 1_b to disable the reporting of the "x" result code.

5.9. Caller ID Decoding Operation

The Si2400 supports full caller ID detection and decode for US Bellcore, UK, and Japanese standards. To use the caller ID decoding feature, the following set-up is necessary:

1. Set SE0[3] (ND) = 0_b (Set modem to 8N1 configuration)
2. Set S13[1] (CIDU) = 1_b (Set modem to Bellcore type caller ID) or S13[2] (CIDB) = 1_b (Set modem to UK type caller ID) or S13[7] (JID) = 1_b (Set modem to Japanese type caller ID)

5.9.1. Bellcore Caller ID Operation

The Si2400 will detect the first ring burst signal and echo an "R" to the host. The device will then start searching for the caller ID preamble sequence after the appropriate time-out. When 50 continuous mark bits have been detected, the "m" response will be echoed to indicate that the mark has been detected and that caller ID data will follow.

At this point the algorithm will look for the first start bit, assemble the characters and transmit them out of the serial port as they are detected.

Finally, the Si2400 will continue detecting ring bursts and echoing "R" for each burst and will automatically answer after the correct number of rings set by S00 (NR).

5.9.2. UK Caller ID Operation

When the Si2400 detects a line reversal, it will echo an "f" to the host. It will then start searching for the Idle State Tone Alert Signal. When this signal has been detected, the Si2400 will transmit an "a" to the host. After the Idle State Tone Alert Signal is completed, the Si2400 will apply the wetting pulse for the required 15 ms by quickly going off hook and on hook. From this point on, the algorithm is identical to that of Bellcore in that it will search for the channel seizure signal and the marks before echoing an "m" and will then report the decoded caller ID data. The wetting pulse may cause false intrusions to be detected. To prevent this, setting S14[7] (MRCD) = 1_b is recommended.

5.9.3. Japan Caller ID Operation

After a polarity reversal and the first ring burst are detected, the Si2400 is taken off hook. The Si2400 then looks for mark bits. If three seconds elapse without detecting a mark bit, the Si2400 hangs up and echoes an "H". Otherwise, after 40 1s (marks) have been detected, the Si2400 will search for a start bit, echo an "m" for mark, and begin assembling characters and transmitting them out through the serial port. When the carrier is lost, the Si2400 immediately hangs up and echoes "N".

5.9.4. Force Caller ID Monitor

The Si2400 may be used to continuously monitor the phone line for the caller ID mark signals. This can be useful in systems that require detection of caller ID data before the ring signal, voice mail indicator signals, and Type II caller ID monitor support. To force the Si2400 into caller ID monitor mode, set SOC[6:5] (CIDM) = 11b. In addition, the Force Caller ID Monitor feature can require that the caller ID FSK data be preceded by either a DTMF A or D or a channel seizure pattern by setting CIDM appropriately.

Note: CIDM should be disabled before going off-hook.

5.9.5. DTMF Caller ID

In order for the Si2400 to detect DTMF-based caller ID, it must be put into the data mode for DTMF detection. This mode behaves similarly to the ATA0 and ATDT!0 modes in that once a command is sent, ATO must be sent to return to the detection state. The following commands place the Si2400 into an on-hook DTMF detection mode:

ATS1D=02SF0=02SE8=02SE6=01S83=66O<CR>

The Si2400 cannot distinguish between DTMF sent from the central office or DTMF sent from a parallel phone. For this reason, the host processor will need to know the proper format of the caller ID information to interpret whether the incoming digits are caller ID information or if they are the outgoing digits of a parallel phone. DTMF-based caller ID typically uses the extended DTMF digits (A, B, C, D, *, #) to indicate the start and end of the caller ID data.

While in this mode, the Si2400 will not report detection of ringing and must rely on the caller ID string as an indication that the phone is ringing. It is necessary to end the DTMF detection mode by sending the ATH command before originating (ATDT) or answering (ATA) a call.

5.10. Tone Generation and Tone Detection

The Si2400 provides comprehensive and flexible tone generation and detection. This includes all tones needed to establish a circuit connection and to set up and control a communication session. The tone generation furnishes the DTMF tones for PSTN auto dialing and the supervisory tones for call establishment. The tone detection provides support for call progress monitoring. The detector can also be user-programmed to recognize up to four tones and two tone detection bandpass filters.

DTMF tones may be detected and generated by using the “ATA0” and “ATDT!0” commands described in the AT command section. A description of the user-programmable tones can be found in "7.1.DSP Registers" on page 40.

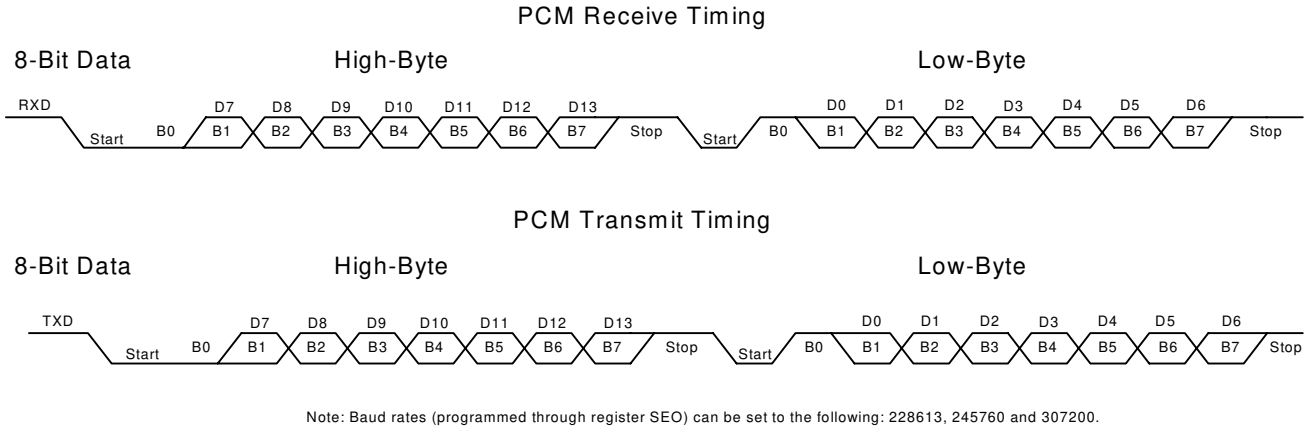
The Si2400 DTMF decoder is designed for single loop applications such as local detection of a parallel DTMF device. Applications requiring DTMF detection across two loops such as programming via a remote keypad are not supported.

5.11. PCM Data Mode

The Si2400 has the ability to bypass the modem algorithm and send 14-bit PCM data, sampled at 9600 Hz, across the DAA. To use this mode, it is necessary to set the serial link (DTE) rate to at least 228613 bps SE0[2:0] (SD) = 101b, set S13[0] (PCM) = 1_b, and set SE1[7:6] (MCKR) = 00_b. The data format (Figure 9) requires that the high byte be sent first containing bits D13–D7. The LSB (B0) must equal zero. The low byte must be sent next containing bits D6–D0; the LSB (B0) must equal one. The receive data format is the same.

In PCM data mode, the line can be answered or originated using the “ATDT#;” command. (The “;” is used to keep the modem from leaving the command mode.) When PCM data mode is enabled (set S13[0] (PCM) = 1_b and SE4[5:4] (DRT) = 001_b (default)), data will immediately begin streaming into and out of the serial port at a 9600 Hz • 2 word rate. In this mode, the controller will not detect dial tones or other call progress tones. If desired, the user can monitor these tones using manual call progress detection prior to entering the PCM data mode.

To exit the PCM data mode, an escape must be performed either by pulsing the ESC pin or by using 9-bit data mode and setting the ninth bit. (TIES cannot be used in PCM data mode.) The escape command will disable PCM streaming, and the controller will again accept AT style commands.



Note: Baud rates (programmed through register SEO) can be set to the following: 228613, 245760 and 307200.

Figure 9. PCM Timing

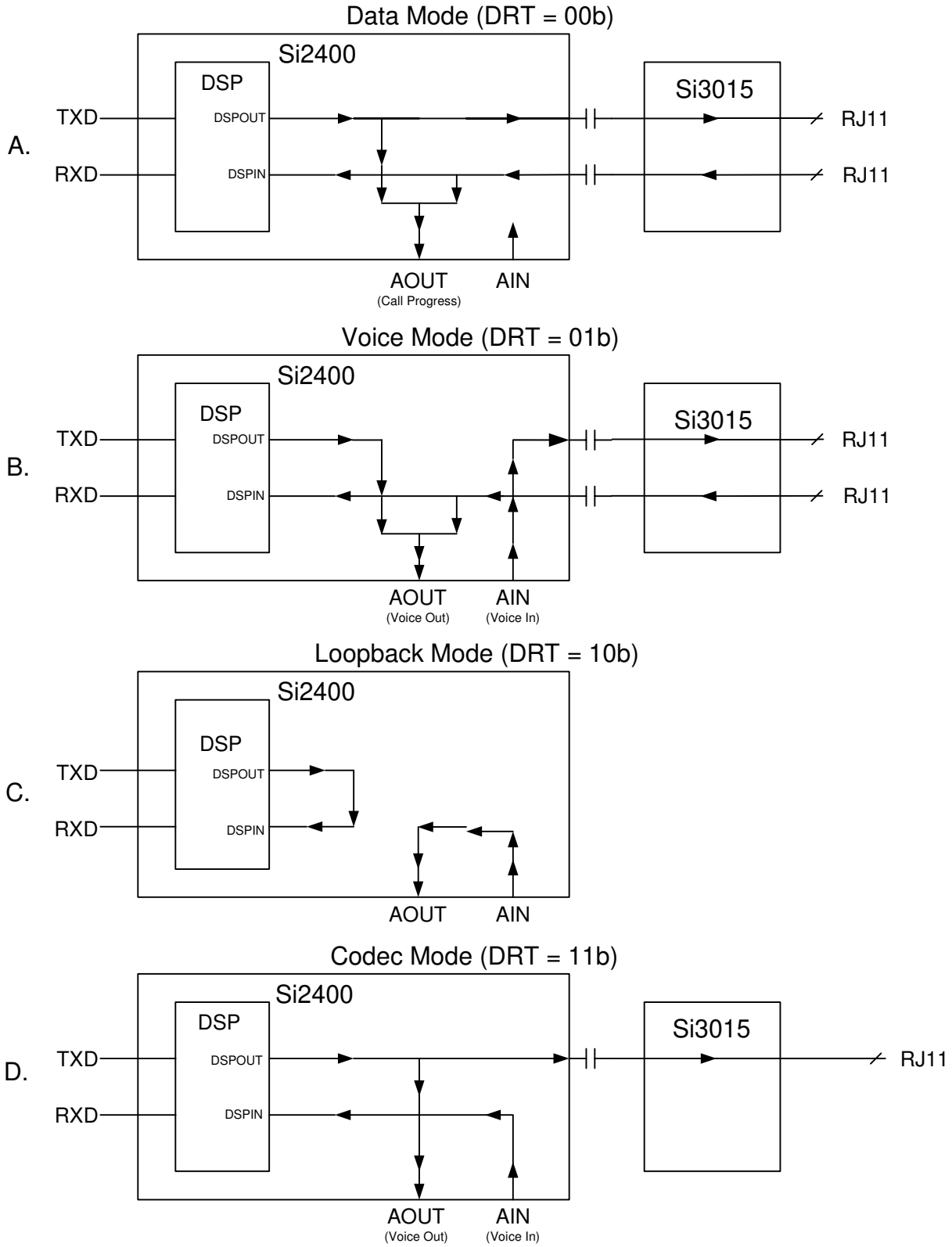


Figure 10. Signal Routing

5.12. Analog Codec

The Si2400 features an on-chip, voice quality codec. The codec consists of a digital to analog converter (DAC) and an analog to digital converter (ADC). The sample rate for the codec is set to 9.6 kHz. When the codec is powered on (SE4[1] [APO] = 1_b), the output of the DAC is always present on the Si2400 AOUT pin. When the codec is powered off (APO = 0_b), a PWM output is present on the AOUT pin instead. In order to use the ADC, one of the four GPIO pins must be selected as an analog input (AIN) by programming SE2 (GPIO).

Figure 10 shows the various signal routing modes for the Si2400 voice codec, which are programmed through register SE4[5:4] (DRT). Figure 10A shows the data routing for data mode. This is the default mode used for modem data formats. In this configuration, AOUT produces a mixed sum of the DSPOUT and DSPIN signals and is typically used for call progress monitoring through an external speaker. The relative levels of the DSPOUT and DSPIN signals that are output on the AOUT pin can be set through SF4[1:0] (ATL) and SF4[3:2] (ARL).

Figure 10B shows the format for sending analog voice across the DAA to the PSTN. AIN is routed directly across the DAA to the telephone line. In this configuration, AOUT produces a mixed sum of the DSPOUT and DSPIN signals. The relative levels of the DSPOUT and DSPIN signals that are output on the AOUT pin can be set through registers ATL and ARL. The DSP may process these signals if it is not in PCM data mode. Thus, the DSP may be used in this configuration, for example, to decode DTMF tones. This is the mode used with the “!0” and “A0” commands.

Figure 10C shows the loopback format, which can be used for in-circuit testing.

Figure 10D shows the codec mode. This format is useful, for example, in voice prompting, speaker phones, or any systems involving digital signal processing. In this mode, DSPOUT is routed to both the AOUT pin and to the telephone line, and AIN is routed directly to DSPIN.

In all the DRT formats, the DSP must be in PCM mode in order to pass DSPIN and DSPOUT directly to and from TXD and RXD.

5.13. V.23 Operation/V.23 Reversing

The Si2400 supports full V.23 operation including the V.23 reversing procedure. V.23 operation is enabled by setting S07 (MF1) = $xx10xx00_b$ or $xx01xx10_b$. If S07[5] (V23R) = 1_b, then the Si2400 will transmit data at 75 bps and receive data at either 600 or 1200 bps. If S07[4] (V23T) = 1_b, then the Si2400 will receive data at 75 bps and transmit data at either 600 or 1200 bps. S07[2] (BAUD) is the 1200 or 600 bps indicator. BAUD = 1_b will enable the 1200/600 V.23 channel to run at 1200 bps while BAUD = 0_b will enable 600 bps operation.

When a V.23 connection is successfully established, the modem will respond with a “c” character if the connection is made with the modem transmitting at 1200/600 bps and receiving at 75 bps. The modem will respond with a “v” character if a V.23 connection is established with the modem transmitting at 75 bps and receiving at 1200/600 bps.

The Si2400 supports the V.23 turnaround procedure. This allows a modem that is transmitting at 75 bps to initiate a “turnaround” procedure so that it can begin transmitting data at 1200/600 bps and receiving data at 75 bps. The modem is defined as being in V.23 master mode if it is transmitting at 75 bps and it is defined as being in slave mode if the modem is transmitting at 1200/600 bps. The following paragraphs give a detailed description of the V.23 turnaround procedure.

5.13.1. Modem in master mode

To perform a direct turnaround once a modem connection is established, the master host goes into online-command-mode by sending an escape command (Escape pin activation, TIES, or ninth bit escape) to the master modem. (Note that the host can initiate a turnaround only if the Si2400 is the master.) The host then sends the ATRO command to the Si2400 to initiate a V.23 turnaround and to go back to the online (data) mode.

The Si2400 will then change its carrier frequency (from 390 Hz to 1300 Hz), and wait to detect a 390 Hz carrier for 440 ms. If the modem detects more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it will echo the “c” response character. If the modem does not detect more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it will hang up and echo the “N” (no carrier) character as a response