



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





## 3.3 V ENHANCED GLOBAL DIRECT ACCESS ARRANGEMENT

### Features

Complete DAA includes the following:

- Line voltage monitor
- Loop current monitor
- 3.2 dBm transmit/receive levels
- Parallel handset detection
- 7  $\mu$ A on-hook line monitor current
- Overload protection
- Programmable line interface
  - AC termination
  - DC termination
  - Ring detect threshold
  - Ringer impedance
- Polarity reversal detection
- 84 dB dynamic range TX/RX
- Integrated analog front end (AFE) and 2- to 4-wire hybrid
- Integrated ring detector
- Caller ID support
- Pulse dialing support
- Billing tone detection
- 3.3 V or 5 V power supply
- Direct interface to DSPs
- Up to 5000 V isolation
- Proprietary isolation technology

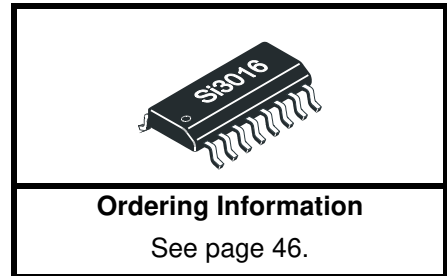
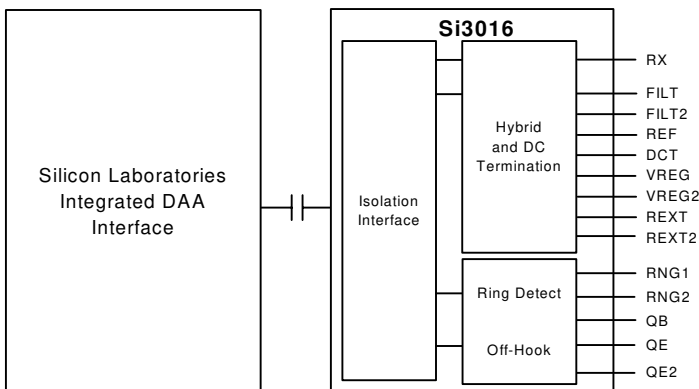
### Applications

- V.90 modems
- Set-top boxes
- Internet appliances
- Voice mail systems
- Fax machines
- VOIP systems

### Description

The Si3016 is an integrated direct access arrangement (DAA) line-side device with a programmable line interface to meet global telephone line interface requirements. Available in a 16-pin small outline package, it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3016 dramatically reduces the number of discrete components and cost required to achieve compliance with global regulatory requirements. The Si3016 interfaces directly to a Silicon Laboratories integrated DAA system-side interface.

### Functional Block Diagram



**Pin Assignments**

**Si3016**

QE2	1	16	FILT2
DCT	2	15	FILT
IGND	3	14	RX
C1B	4	13	REXT
RNG1	5	12	REXT2
RNG2	6	11	REF
QB	7	10	VREG2
QE	8	9	VREG

U.S. Patent #5,870,046  
U.S. Patent #6,061,009  
Other Patents Pending



---

**TABLE OF CONTENTS**


---

<b><u>Section</u></b>	<b><u>Page</u></b>
<b>1. Electrical Specifications</b>	<b>4</b>
<b>2. Bill of Materials</b>	<b>10</b>
<b>3. Analog Output</b>	<b>11</b>
<b>4. Functional Description</b>	<b>12</b>
4.1. Initialization	14
4.2. Power Supply	14
4.3. Isolation Barrier	14
4.4. Transmit/Receive Full Scale Level	14
4.5. Parallel Handset Detection	15
4.6. Line Voltage/Loop Current Sensing	15
4.7. Off-Hook	16
4.8. DC Termination	16
4.9. DC Termination Considerations	17
4.10. AC Termination	18
4.11. Ring Detection	18
4.12. Ringer Impedance	18
4.13. DTMF Dialing	19
4.14. Pulse Dialing	19
4.15. Billing Tone Detection	19
4.16. Billing Tone Filter (Optional)	20
4.17. On-Hook Line Monitor	20
4.18. Caller ID	20
4.19. Overload Protection	22
4.20. Analog Output	22
4.21. Gain Control	23
4.22. Clocking	23
4.23. Power Management	23
4.24. Calibration	23
4.25. In-Circuit Testing	24
4.26. Exception Handling	24
4.27. Revision Identification	25
<b>5. Control Registers</b>	<b>26</b>
<b>Appendix A—UL1950 3rd Edition</b>	<b>42</b>
<b>Appendix B—CISPR22 Compliance</b>	<b>43</b>
<b>6. Pin Descriptions: Si3016</b>	<b>44</b>
<b>7. Ordering Guide</b>	<b>46</b>
<b>8. Package Outline: SOIC</b>	<b>47</b>
<b>Document Change List</b>	<b>48</b>
<b>Contact Information</b>	<b>50</b>



## 1. Electrical Specifications

All Si3016 electrical specifications are based on the assumption that all specifications listed in the data sheet of the host processor with the integrated system-side DAA module are met.

**Table 1. Recommended Operating Conditions**

Parameter <sup>1</sup>	Symbol	Test Condition	Min <sup>2</sup>	Typ	Max <sup>2</sup>	Unit
Ambient Temperature	T <sub>A</sub>	K-Grade	0	25	70	°C
Ambient Temperature	T <sub>A</sub>	B-Grade	-40	25	85	°C

**Notes:**

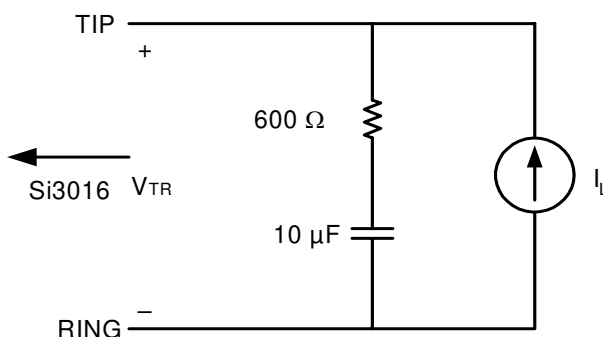
1. The Si3016 specifications are guaranteed when the typical application circuit (including component tolerance) and any system-side module and any Si3016 are used. See Figure 6, “Si3016 Typical Application Circuit,” on page 9.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

**Table 2. Loop Characteristics**(T<sub>A</sub> = 0 to 70 °C for K-Grade and -40 to 85 °C for B-Grade, See Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ACT = 1 DCT = 11 (CTR21)	—	—	7.5	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 42 mA, ACT = 1 DCT = 11 (CTR21)	—	—	14.5	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 50 mA, ACT = 1 DCT = 11 (CTR21)	—	—	40	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 60 mA, ACT = 1 DCT = 11 (CTR21)	40	—	—	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ACT = 0 DCT = 01 (Japan)	—	—	6.0	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 100 mA, ACT = 0 DCT = 01 (Japan)	9	—	—	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ACT = 0 DCT = 10 (FCC)	—	—	7.5	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 100 mA, ACT = 0 DCT = 10 (FCC)	9	—	—	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 15 mA, ACT = 0 DCT = 00 (Low Voltage)	—	—	5.2	V
On Hook Leakage Current <sup>1</sup>	I <sub>LK</sub>	V <sub>TR</sub> = -48 V	—	—	7	μA
Operating Loop Current	I <sub>LP</sub>	FCC / Japan Modes	13	—	120	mA
Operating Loop Current	I <sub>LP</sub>	CTR21 Mode	13	—	60	mA
DC Ring Current <sup>1</sup>		dc flowing through ring detection circuitry	—	—	7	μA
Ring Detect Voltage <sup>2</sup>	V <sub>RD</sub>	RT = 0	11	—	22	V <sub>RMS</sub>
Ring Detect Voltage <sup>2</sup>	V <sub>RD</sub>	RT = 1	17	—	33	V <sub>RMS</sub>
Ring Frequency	F <sub>R</sub>		15	—	68	Hz
Ringer Equivalence Number <sup>3</sup>	REN		—	—	0.2	

**Notes:**

1. R25 and R26 installed.
2. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
3. RZ = 0. See "4.12. Ringer Impedance" on page 18.

**Figure 1. Test Circuit for Loop Characteristics**



# Si3016

**Table 3. DC Characteristics**

( $T_A = 0$  to  $70$  °C for K-Grade and  $-40$  to  $85$  °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	$I_L$		-10	—	10	$\mu$ A
Power Supply Current, Analog*	$I_A$		—	0.3	—	mA

\*Note: This current is required from the integrated system-side interface to communicate with the Si3016 through the isolation interface.

**Table 4. AC Characteristics**

( $T_A = 0$  to  $70$  °C for K-Grade and  $-40$  to  $85$  °C for B-Grade; see Figure 6 on page 9)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	$F_s$	$F_s = F_{PLL2}/5120$	7.2	—	11.025	KHz
Transmit Frequency Response		Low -3 dBFS Corner	—	0	—	Hz
Receive Frequency Response		Low -3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level <sup>1</sup>	$V_{FS}$	FULL = 0 (-1 dBm)	—	1	—	$V_{PEAK}$
		FULL = 1 (+3.2 dBm) <sup>2</sup>	—	1.58	—	$V_{PEAK}$
Receive Full Scale Level <sup>1,3</sup>	$V_{FS}$	FULL = 0 (-1 dBm)	—	1	—	$V_{PEAK}$
		FULL = 1 (+3.2 dBm) <sup>3</sup>	—	1.58	—	$V_{PEAK}$
Dynamic Range <sup>4,5,6</sup>	DR	ACT=0, DCT=10 (FCC) $I_L=100$ mA	—	82	—	dB
Dynamic Range <sup>4,5,7</sup>	DR	ACT=0, DCT=01 (Japan) $I_L=20$ mA	—	83	—	dB
Dynamic Range <sup>4,5,6</sup>	DR	ACT=1, DCT=11(CTR21) $I_L=60$ mA	—	84	—	dB
Transmit Total Harmonic Distortion <sup>6,8</sup>	THD	ACT=0, DCT=10 (FCC) $I_L=100$ mA	—	-85	—	dB
Transmit Total Harmonic Distortion <sup>7,8</sup>	THD	ACT=0, DCT=01 (Japan) $I_L=20$ mA	—	-76	—	dB
Receive Total Harmonic Distortion <sup>7,8</sup>	THD	ACT=0, DCT=01 (Japan) $I_L=20$ mA	—	-74	—	dB
Receive Total Harmonic Distortion <sup>6,8</sup>	THD	ACT=1, DCT=11 (CTR21) $I_L=60$ mA	—	-82	—	dB
Dynamic Range (Caller ID mode)	$DR_{CID}$	$V_{IN} = 1$ kHz, -13 dBm	—	60	—	dB

**Notes:**

1. Measured at TIP and RING with  $600 \Omega$  termination at 1 kHz, as shown in Figure 1.
2. R2 should be changed to a  $243 \Omega$  resistor when the FULLSCALE bit (FULL) is set to 1 (Register 18, bit 7).
3. Receive full scale level will produce -0.9 dBFS at SDO.
4.  $DR = 20 \times \log |V_{in}| + 20 \times \log (\text{RMS signal/RMS noise})$ .
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6.  $V_{in} = 1$  kHz, -3 dBFS,  $F_s = 10300$  Hz.
7.  $V_{in} = 1$  kHz, -6 dBFS,  $F_s = 10300$  Hz.
8.  $THD = 20 \times \log (\text{RMS distortion/RMS signal})$ .
9. The AOUT pin is an optional pin located on the integrated system-side module.  $V_D$  refers to the digital power supply of the integrated system-side module.

**Table 4. AC Characteristics (Continued)**(T<sub>A</sub> = 0 to 70 °C for K-Grade and –40 to 85 °C for B-Grade; see Figure 6 on page 9)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Caller ID Full Scale Level (0 dB gain)	V <sub>CID</sub>	MODE = 0	—	0.8	—	V <sub>PP</sub>
Caller ID Full Scale Level (ARX = 00)	V <sub>CID</sub>	MODE = 1	—	1.4	—	V <sub>PP</sub>
Gain Accuracy <sup>5,6</sup>		2-W to SDO, ATX and ARX = 000, 001, or 010	–0.5	0	0.5	dB
Gain Accuracy <sup>5,6</sup>		2-W to SDO, ATX and ARX = 011, 1xx	–1	0	1	dB

**Notes:**

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
2. R2 should be changed to a 243 Ω resistor when the FULLSCALE bit (FULL) is set to 1 (Register 18, bit 7).
3. Receive full scale level will produce –0.9 dBFS at SDO.
4. DR = 20 x log |Vin| + 20 x log (RMS signal/RMS noise).
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
7. Vin = 1 KHz, –6 dBFS, Fs = 10300 Hz.
8. THD = 20 x log (RMS distortion/RMS signal).
9. The AOUT pin is an optional pin located on the integrated system-side module. V<sub>D</sub> refers to the digital power supply of the integrated system-side module.

**Table 5. Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Operating Temperature Range	T <sub>A</sub>	–40 to 100	°C
Storage Temperature Range	T <sub>STG</sub>	–65 to 150	°C

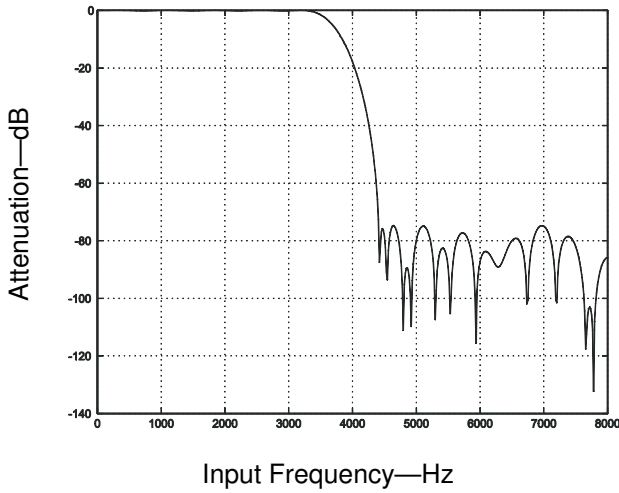
**Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6. Digital FIR Filter Characteristics—Transmit and Receive**(Sample Rate = 8 kHz, T<sub>A</sub> = 70 °C for K-Grade and –40 to 85 °C for B-Grade)

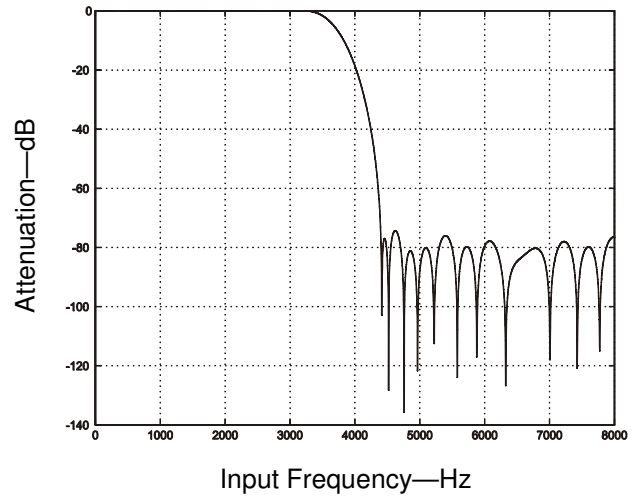
Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	F <sub>(0.1 dB)</sub>	0	—	3.3	kHz
Passband (3 dB)	F <sub>(3 dB)</sub>	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t <sub>gd</sub>	—	12/Fs	—	sec

**Note:** Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 2, 3, 4, and 5.

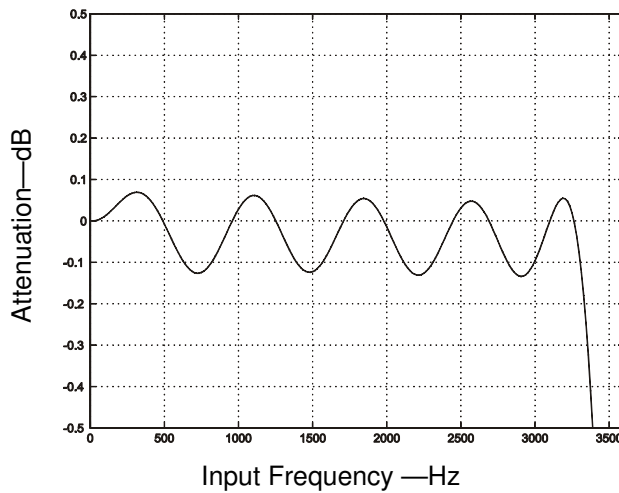




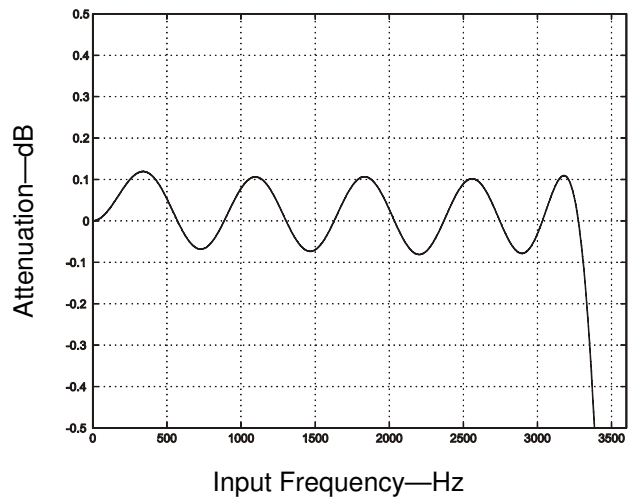
**Figure 2. FIR Receive Filter Response**



**Figure 4. FIR Transmit Filter Response**



**Figure 3. FIR Receive Filter Passband Ripple**



**Figure 5. FIR Transmit Filter Passband Ripple**

For Figures 2–5, all filter plots apply to a sample rate of  $F_s = 8 \text{ kHz}$ . The filters scale with the sample rate as follows:

$$F_{(0.1 \text{ dB})} = 0.4125 F_s$$

$$F_{(-3 \text{ dB})} = 0.45 F_s$$

where  $F_s$  is the sample frequency.

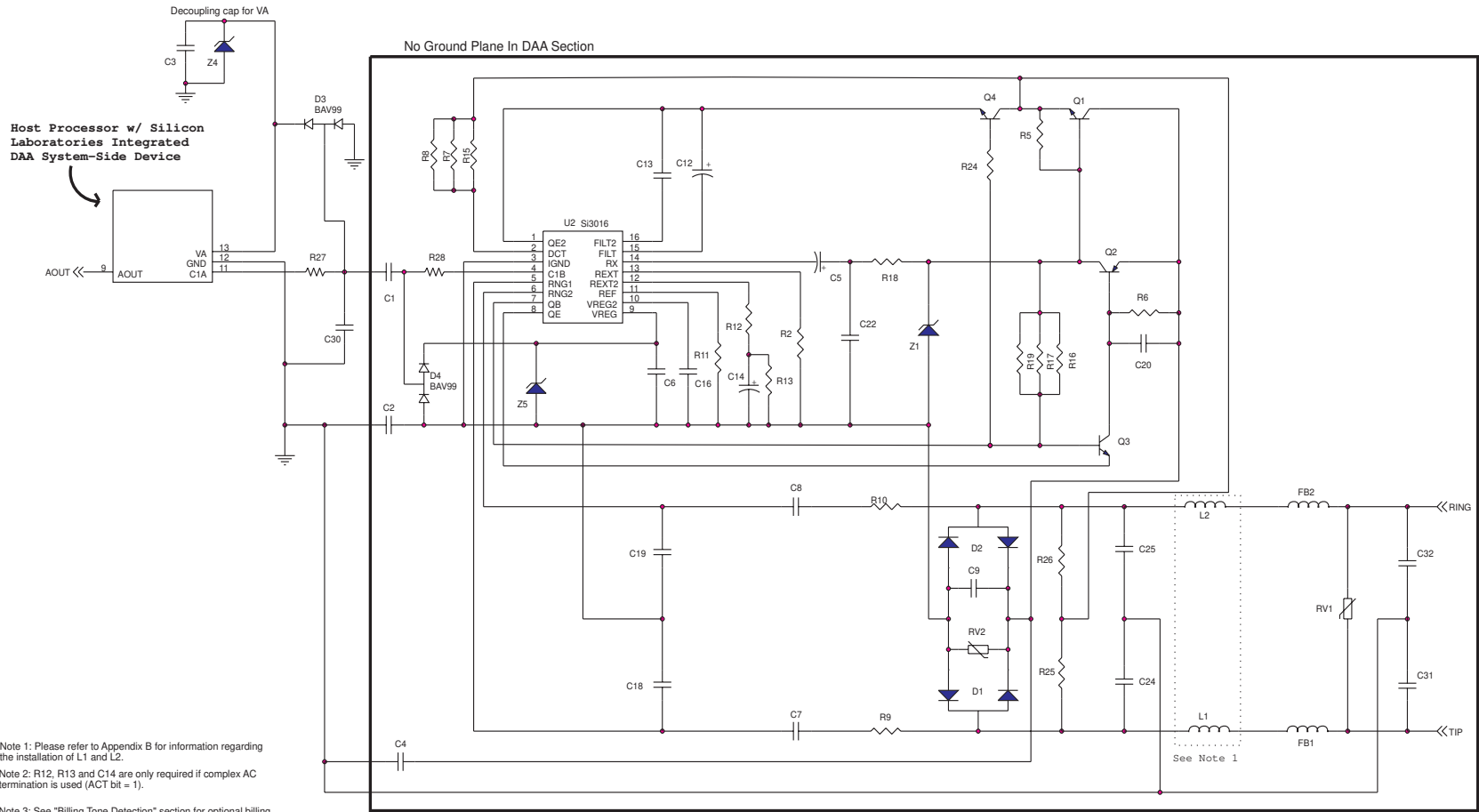


Figure 6. Si3016 Typical Application Circuit

## 2. Bill of Materials

**Table 7. Si3016 Global Component Values**

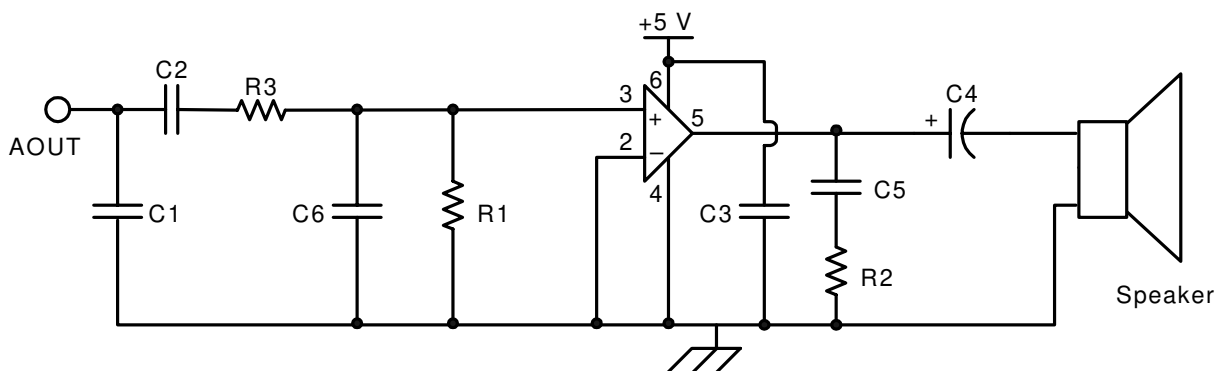
Component	Value	Supplier(s)
C1,C4 <sup>1</sup>	150 pF, 3 kV, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C2, C31, C32	Not Installed	
C3, C13 <sup>2</sup>	0.22 μF, 16 V, X7R, ±20%	
C5	0.1 μF, 50 V, Elec/Tant, ±20%	
C6,C16	0.1 μF, 16 V, X7R, ±20%	
C7,C8	560 pF, 250 V, X7R, ±20%	Novacap, Johanson, Murata, Panasonic
C9	10 nF, 250 V, X7R, ±20%	
C12	1.0 μF, 16 V, Tant, ±20%	Panasonic
C14	0.68 μF, 16 V, X7R/Elec/Tant, ±20%	
C18,C19	3.9 nF, 16 V, X7R, ±20%	
C20	0.01 μF, 16 V, X7R, ±20%	
C22	1800 pF, 50 V, X7R, ±20%	
C24,C25 <sup>1</sup>	1000 pF, 3 kV, X7R, ±10%	
C30 <sup>3</sup>	Not Installed	
D1,D2 <sup>4</sup>	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4	BAV99 Dual Diode, 70 V, 350 mW	Diodes Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead	Murata
L1, L2 <sup>5</sup>	330 μH, DCR < 3 Ω, 120 mA, ±10%	Taiyo-Yuden, ACT, Transtek Magnetics, Cooper Electronics
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild
Q4 <sup>6</sup>	BCP56T1, NPN, 80 V, 1/2 W	OnSemiconductor, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2 <sup>7</sup>	Not Installed	
R2 <sup>8</sup>	402 Ω, 1/16 W, ±1%	
R5	100 kΩ, 1/16 W, ±1%	
R6	120 kΩ, 1/16 W, ±5%	
R7,R8,R15,R16,R17,R19 <sup>9</sup>	5.36 kΩ, 1/4 W, ±1%	
R9,R10	56 kΩ, 1/10 W, ±5%	
R11	9.31 kΩ, 1/16 W, ±1%	
R12	78.7 Ω, 1/16 W, ±1%	
R13	215 Ω, 1/16 W, ±1%	
R18	2.2 kΩ, 1/10 W, ±5%	
R24	150 Ω, 1/16 W, ±5%	
R25,R26	10 MΩ, 1/16 W, ±5%	
R27,R28	10 Ω, 1/10 W, ±5%	
U1	Si3021	Silicon Labs
U2	Silicon Labs System-Side Device	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	Vishay, Motorola, Rohm
Z4,Z5	Zener Diode, 5.6 V, 1/2 W	Vishay, Motorola, Rohm

**Notes:**

- Y2 class capacitors are needed for the Nordic requirements of EN60950 and may also be used to achieve surge performance of 5 kV or better.
- C13 is used to ensure compliance with on-hook pulse dialing and spark quenching requirements in countries, such as Australia and South Africa. If this is not a concern, a 0.1 μF cap may be used.
- Install only if needed for improved radiated emissions performance (10 pF, 16 V, NPO, ±10%).
- Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.).
- See Appendix B for additional requirements.
- Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
- RV2 can be installed to improve performance from 2500 V to 3500 V for multiple longitudinal surges (270 V, MOV).
- If supporting +3.2 dBFS voice applications, R2 should be 243 Ω and set the FULLSCALE bit (Reg 18[7]).
- The R7, R8, R15, and R16, R17, and R19 resistors may each be replaced with a single resistor of 1.62 kΩ, 3/4 W, ±1%.

### 3. Analog Output

Figure 7 illustrates an optional application circuit to support the analog output capability of the DAA system-side module for call progress monitoring purposes. The ARM bits in Register 6 allow the receive path to be attenuated by 0, -6, or -12 dB. The ATM bits, which are also in Register 6, allow the transmit path to be attenuated by -20, -26, or -32 dB. Both the transmit and receive paths can also be independently muted.



**Figure 7. Optional Connection to AOUT for a Call Progress Speaker**

**Table 8. Component Values—Optional Connection to AOUT**

Symbol	Value
C1	2200 pF, 16 V, $\pm 20\%$
C2, C3, C5	0.1 $\mu$ F, 16 V, $\pm 20\%$
C4	100 $\mu$ F, 16 V, Elec. $\pm 20\%$
C6	820 pF, 16 V, $\pm 20\%$
R1	10 k $\Omega$ , 1/10 W, $\pm 5\%$
R2	10 $\Omega$ , 1/10 W, $\pm 5\%$
R3	47 k $\Omega$ , 1/10 W, $\pm 5\%$
U1	LM386

## 4. Functional Description

The Si3016 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The device implements Silicon Laboratories' proprietary capacitive isolation technology which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with a 16-pin small outline integrated circuit (SOIC) package in conjunction with a system-side module that is integrated into another device.

The Si3016 chip can be fully programmed to meet international requirements and is compliant with FCC, CTR21, JATE, and various other country-specific PTT specifications as shown in Table 9. In addition, the Si3016 has been designed to meet the most stringent global requirements for out-of-band energy, emissions, immunity, lightning surges, and safety.

The Si3016 is intended for single-channel applications. For multi-channel applications, up to eight Si3044 DAAs can be daisy-chained together on one serial port.

**Table 9. Country Specific Register Settings**

Register Country	16					17	18
	OHS	ACT	DCT[1:0]	RZ	RT	LIM	VOL
Argentina	0	0	10	0	0	0	0
Australia <sup>1</sup>	1	1	01	0	0	0	0
Austria	0	0 or 1	11	0	0	1	0
Bahrain	0	0	10	0	0	0	0
Belgium	0	0 or 1	11	0	0	1	0
Brazil <sup>1</sup>	0	0	01	0	0	0	0
Bulgaria	0	1	11	0	0	1	0
Canada	0	0	10	0	0	0	0
Chile	0	0	10	0	0	0	0
China <sup>1</sup>	0	0	01	0	0	0	0
Colombia	0	0	10	0	0	0	0
Croatia	0	1	11	0	0	1	0
CTR21 <sup>1,2</sup>	0	0 or 1	11	0	0	1	0
Cyprus	0	1	11	0	0	1	0
Czech Republic	0	1	11	0	0	1	0
Denmark	0	0 or 1	11	0	0	1	0
Ecuador	0	0	10	0	0	0	0
Egypt <sup>1</sup>	0	0	01	0	0	0	0
El Salvador	0	0	10	0	0	0	0
Finland	0	0 or 1	11	0	0	1	0
France	0	0 or 1	11	0	0	1	0
Germany	0	0 or 1	11	0	0	1	0
Greece	0	0 or 1	11	0	0	1	0
Guam	0	0	10	0	0	0	0
Hong Kong	0	0	10	0	0	0	0

**Notes:**

1. See "4.9. DC Termination Considerations" on page 17 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. Supported for loop current  $\geq 20$  mA.

Table 9. Country Specific Register Settings

Register Country	16					17	18
	OHS	ACT	DCT[1:0]	RZ	RT	LIM	VOL
Hungary	0	0	10	0	0	0	0
Iceland	0	0 or 1	11	0	0	1	0
India	0	0	10	0	0	0	0
Indonesia	0	0	10	0	0	0	0
Ireland	0	0 or 1	11	0	0	1	0
Israel	0	0 or 1	11	0	0	1	0
Italy	0	0 or 1	11	0	0	1	0
Japan <sup>1</sup>	0	0	01	0	0	0	0
Jordan <sup>1</sup>	0	0	01	0	0	0	0
Kazakhstan <sup>1</sup>	0	0	01	0	0	0	0
Kuwait	0	0	10	0	0	0	0
Latvia	0	0 or 1	11	0	0	1	0
Lebanon	0	0 or 1	11	0	0	1	0
Luxembourg	0	0 or 1	11	0	0	1	0
Macao	0	0	10	0	0	0	0
Malaysia <sup>1,3</sup>	0	0	01	0	0	0	0
Malta	0	0 or 1	11	0	0	1	0
Mexico	0	0	10	0	0	0	0
Morocco	0	0 or 1	11	0	0	1	0
Netherlands	0	0 or 1	11	0	0	1	0
New Zealand	0	1	10	0	0	0	0
Nigeria	0	0 or 1	11	0	0	1	0
Norway	0	0 or 1	11	0	0	1	0
Oman <sup>1</sup>	0	0	01	0	0	0	0
Pakistan <sup>1</sup>	0	0	01	0	0	0	0
Peru	0	0	10	0	0	0	0
Philippines <sup>1</sup>	0	0	01	0	0	0	0
Poland	0	0	10	1	1	0	0
Portugal	0	0 or 1	11	0	0	1	0
Romania	0	0	10	0	0	0	0
Russia <sup>1</sup>	0	0	01	0	0	0	0
Saudi Arabia	0	0	10	0	0	0	0
Singapore	0	0	10	0	0	0	0
Slovakia	0	0	10	0	0	0	0
Slovenia	0	0	10	1	1	0	0
South Africa	1	0	10	1	0	0	0
South Korea	0	0	10	0	0	0	0

**Notes:**

1. See "4.9. DC Termination Considerations" on page 17 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. Supported for loop current  $\geq 20$  mA.



Table 9. Country Specific Register Settings

Register	16					17	18
Country	OHS	ACT	DCT[1:0]	RZ	RT	LIM	VOL
Spain	0	0 or 1	11	0	0	1	0
Sweden	0	0 or 1	11	0	0	1	0
Switzerland	0	0 or 1	11	0	0	1	0
Syria <sup>1</sup>	0	0	01	0	0	0	0
Taiwan <sup>1</sup>	0	0	01	0	0	0	0
Thailand <sup>1</sup>	0	0	01	0	0	0	0
UAE	0	0	10	0	0	0	0
United Kingdom	0	0 or 1	11	0	0	1	0
USA	0	0	10	0	0	0	0
Yemen	0	0	10	0	0	0	0

**Notes:**

1. See "4.9. DC Termination Considerations" on page 17 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. Supported for loop current  $\geq 20$  mA.

#### 4.1. Initialization

When the integrated system-side module and the Si3016 are initially powered up, the DAA registers will have default values that guarantee the line-side chip (Si3016) is powered down with no possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined below:

1. Program the desired sample rate with the Sample Rate Control Register.
2. Wait until the Si3016 PLL is locked. This time is between 100  $\mu$ s and 1 ms.
3. Write a 00H into the DAA Control 2 Register. This powers up the line-side chip (Si3016) and enables the AOUT for call progress monitoring.
4. Set the desired line interface parameters (i.e., DCT[1:0], ACT, OHS, RT, LIM[1:0], and VOL) as defined by "Country Specific Register Settings" shown in Table 9, "Country Specific Register Settings," on page 12.

After this procedure is complete, the Si3016 is ready for ring detection and off-hook.

#### 4.2. Power Supply

When on-hook, the Si3016 draws power across the isolation link from the system-side module. When off-hook, power is drawn from the 2-wire line. Thus, no power supply connections are needed for the Si3016.

#### 4.3. Isolation Barrier

The Si3016 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' proprietary signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 6 on page 9, the C1, C4, C24, and C25 capacitors isolate the system side from the Si3016 (line side). All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier.

The isolated communications link is disabled by default. To enable it, the PDL bit must be cleared. No communication between the system-side module and the Si3016 can occur until this bit is cleared. When the PDL bit is cleared, a check is performed to ensure that the line-side device is an Si3016 device. If it is not, the system-side module will not function.

#### 4.4. Transmit/Receive Full Scale Level

The Si3016 supports programmable maximum transmit and receive levels. The full-scale TX/RX level is established by writing the FULL bit in Register 18. With FULL = 1, the full scale TX/RX level is increased to 3.2 dBm to support certain FCC voice applications that require higher TX/RX levels. When FULL = 1, R2 must be changed from 402  $\Omega$  to 243  $\Omega$ . The default full scale value is -1 dBm (FULL = 0). Note that this higher TX/RX full-scale mode must be used in FCC/600  $\Omega$  termination mode.



## 4.5. Parallel Handset Detection

The Si3016 is capable of detecting a parallel handset going off-hook. When the Si3016 is off-hook, the loop current can be monitored via the LVCS bits. A significant drop in loop current can signal a parallel handset going off-hook. If a parallel handset causes the LVCS bits to read all 0s, the Drop-Out Detect (DOD) bit may be checked to verify that a valid line still exists.

When on-hook, the LVCS bits may also be read to determine the line voltage. Significant drops in line voltage may also be used to detect a parallel handset. For the Si3016 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two off-hook DAAs on the same line. The OFF bit in Register 16 is designed to improve parallel handset operation by changing the dc impedance from 50  $\Omega$  to 800  $\Omega$  and reducing the DCT pin voltage.

## 4.6. Line Voltage/Loop Current Sensing

The Si3016 has the ability to measure both line voltage and loop current. The five bit LVCS register reports line voltage measurements when on-hook, loop current measurements when off-hook, or on-hook line monitor data depending on the state of the MODE, OH, and ONHM bits. Using the LVCS bits, the user can

determine the following:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- Detect if there is an overload condition which could damage the DAA (see overload protection feature).

### 4.6.1. Line Voltage Measurement

The Si3016 reports the line voltage with the LVCS bits in Register 19. LVCS has a full scale of 87 V with an LSB of 2.75 V. The first code (0  $\rightarrow$  1) is skewed such that a 0 indicates that the line voltage is < 3 V. The accuracy of the LVCS bits is  $\pm 20\%$ . The user can read these bits directly through the LVCS register when it is on-hook and the MODE bit is set to 1. A typical transfer function is shown in Figure 8.

### 4.6.2. Loop Current Measurement

When the Si3016 is off-hook, the LVCS bits measure loop current in 3 mA/bit resolution. These bits enable the user to detect another phone going off-hook by monitoring the dc loop current. The line voltage current sense transfer function is shown in Figure 9 and is detailed in Table 10.

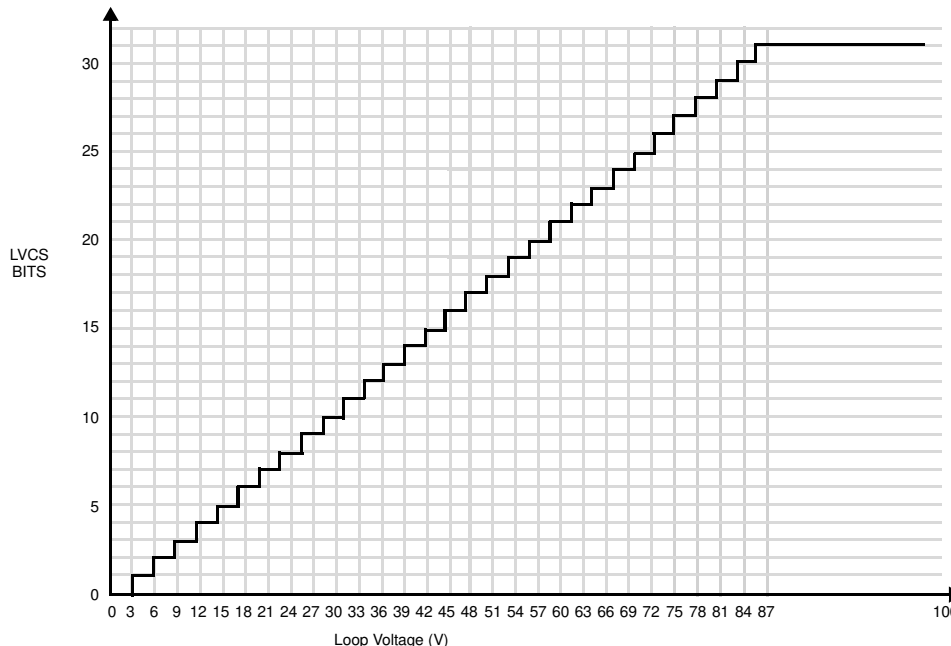
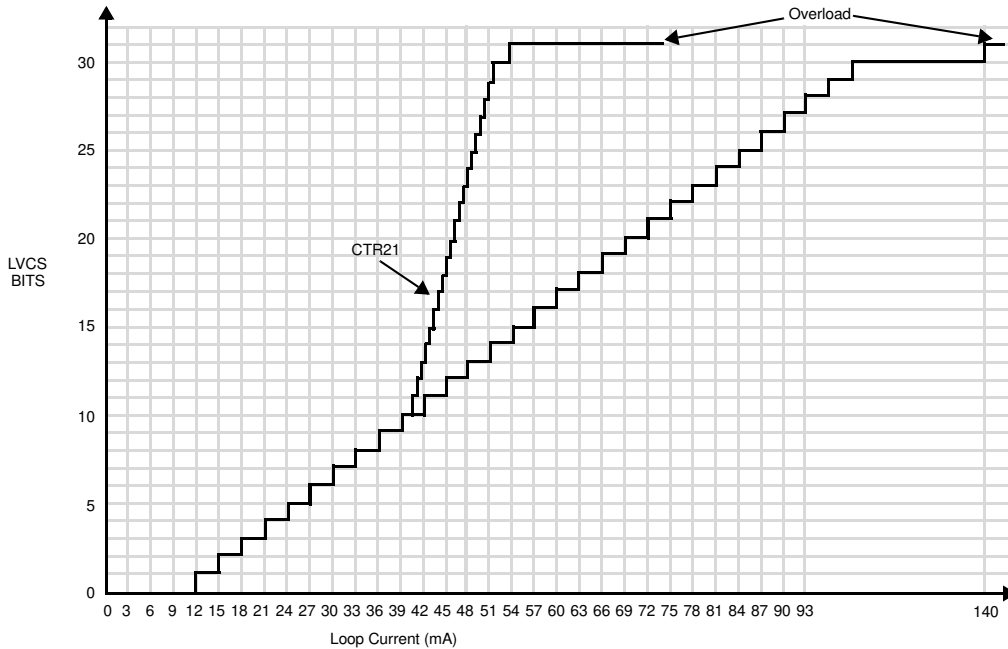


Figure 8. Typical Loop Voltage LVCS Transfer Function



**Figure 9. Typical Loop Current LVCS Transfer Function**

**Table 10. Loop Current Transfer Function**

LVCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DOD bit to determine if a line is still connected.
00001	Minimum line current for normal operation.
11111	Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21. Overload > 54 mA in CTR21 mode.

### 4.7. Off-Hook

The communication system generates an off-hook command by setting the OH bit. With the OH bit set, the system is in an off-hook state.

The off-hook state is used to seize the line for incoming/outgoing calls and can also be used for pulse dialing. When the DAA is on-hook, negligible dc current flows through the hookswitch. When the DAA is placed in the off-hook state, the hookswitch transistor pair, Q1 and Q2, turn on. This applies a termination impedance across TIP and RING and causes dc loop current to flow. The termination impedance has both an ac and dc component.

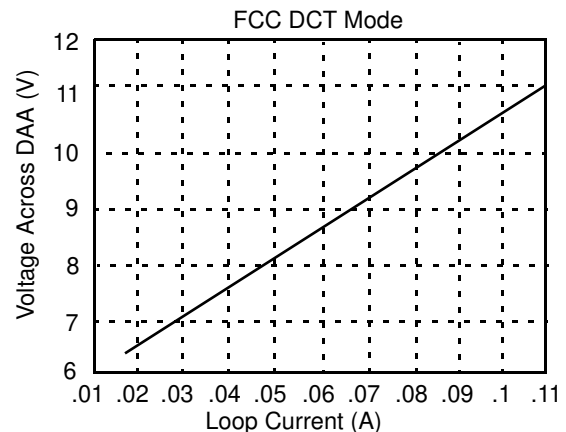
When executing an off-hook sequence, the Si3016 requires  $1548/F_s$  seconds to complete the off-hook and provide phone-line data on the serial link. This includes

the  $12/F_s$  filter group delay. If necessary, for the shortest delay, a higher  $F_s$  may be established prior to executing the off-hook, such as an  $F_s$  of 10.286 kHz. The delay allows for line transients to settle prior to normal use.

### 4.8. DC Termination

The Si3016 has four programmable dc termination modes that are selected with the DCT[1:0] bits in Register 16.

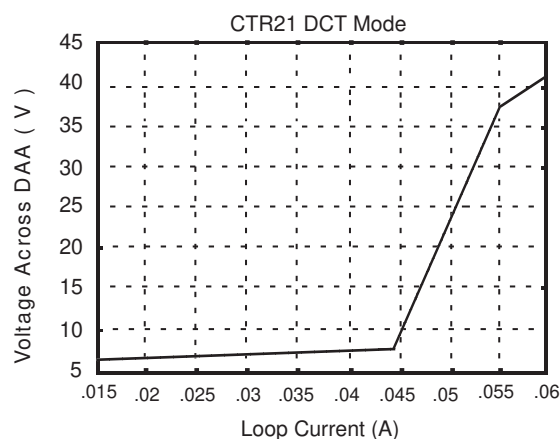
FCC mode (DCT[1:0] = 10 b), shown in Figure 10, is the default dc termination mode and supports a transmit full scale level of  $-1$  dBm at TIP and RING. This mode meets FCC requirements in addition to the requirements of many other countries.



**Figure 10. FCC Mode I/V Characteristics**

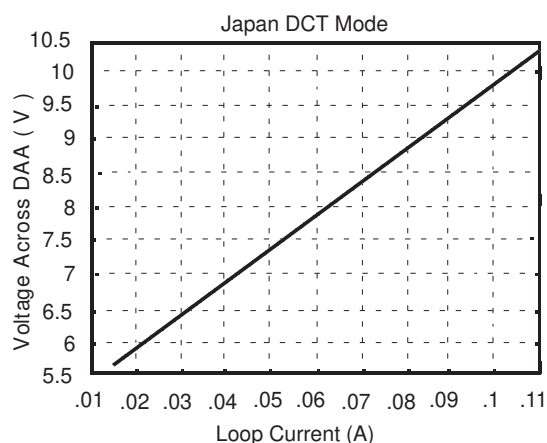
CTR21 mode (DCT[1:0] = 11 b), shown in Figure 11,

provides current limiting while maintaining a transmit full scale level of  $-1$  dBm at TIP and RING. In this mode, the dc termination will current limit before reaching 60 mA if the LIM bit is set.



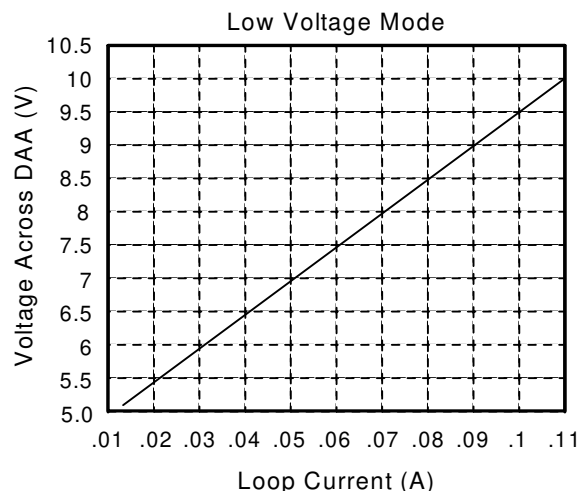
**Figure 11. CTR21 Mode I/V Characteristics**

Japan mode (DCT[1:0] = 01 b), shown in Figure 12, is a lower voltage mode and supports a transmit full scale level of  $-2.71$  dBm. Higher transmit levels for DTMF dialing are also supported. See "4.13. DTMF Dialing" on page 19. The low-voltage requirement is dictated by countries, such as Japan and Malaysia.



**Figure 12. Japan Mode I/V Characteristics**

Low Voltage mode (DCT[1:0] = 00b), shown in Figure 13, is the lowest line voltage mode supported on the Si3016, with a transmit full scale level of  $-5$  dBm. Higher transmit levels for DTMF dialing are also supported. See "4.13. DTMF Dialing" on page 19. This low-voltage mode is offered for situations that require very low line voltage operation. It is important to note that this mode should only be used when necessary, as the dynamic range will be significantly reduced, and thus the Si3016 will not be able to transmit or receive large signals without clipping them.



**Figure 13. Low Voltage Mode I/V Characteristics**

#### 4.9. DC Termination Considerations

Under certain line conditions, it may be beneficial to use other dc termination modes not intended for a particular world region. For instance, in countries that comply with the CTR21 standard, improved distortion characteristics can be seen for very low loop current lines by switching to FCC mode. Thus, after going off-hook in CTR21 mode, the loop current monitor bits (LVCS[4:0]) may be used to measure the loop current, and if  $LVCS[4:0] < 6$ , it is recommended that FCC mode be used.

Additionally, for very low-voltage countries, such as Japan and Malaysia, the following procedure should be used to optimize distortion characteristics and maximize transmit levels:

1. When first going off-hook, use the Low Voltage mode with the VOL bit set to 1.
2. Measure the loop current using the LVCS[4:0] bits.
3. If  $LVCS[4:0] \leq 2$ , maintain the current settings, and proceed with normal operation.
4. If  $LVCS[4:0] > 2$  or  $< 6$ , switch to Japan mode, leave the VOL bit set, and proceed with normal operation.
5. If  $LVCS[4:0] \geq 6$ , switch to FCC mode, set the VOL bit to 0, and proceed with normal operation.

**Note:** A single decision of dc termination mode following off-hook is appropriate for most applications. However, during PTT testing, a false dc termination I/V curve may be generated if the dc I/V curve is determined following a single off-hook event.

Finally, Australia has separate dc termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial



off-hook. This will satisfy the Australian dc termination requirements.

## 4.10. AC Termination

The Si3016 has two ac Termination impedances, which are selected with the ACT bit.

ACT = 0 is a real, nominal 600  $\Omega$  termination, which satisfies the impedance requirements of FCC part 68, JATE, and other countries. This real impedance is set by circuitry internal to the Si3016 as well as the resistor R2 connected to the REXT pin.

ACT = 1 is a complex impedance, which satisfies the impedance requirements of Australia, New Zealand, South Africa, CTR21, and some European NET4 countries, such as the UK and Germany. This complex impedance is set by circuitry internal to the Si3016 as well as the complex network formed by R12, R13, and C14 connected to the REXT2 pin.

## 4.11. Ring Detection

The ring signal is capacitively coupled from TIP and RING to the RNG1 and RNG2 pins. The Si3016 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal as well as the ring signal. See "4.18. Caller ID" on page 20. The ring detection threshold is programmable with the RT bit.

The ring detector output can be monitored in one of two ways. The first method uses the register bits, RDTP, RDTN, and RDT. The second method uses the SDO output internal to the integrated system-side module.

The DSP must detect the frequency of the ring signal in order to distinguish a ring from pulse dialing by telephone equipment connected in parallel.

A positive ringing signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. RNG1 and RNG2 are pins 5 and 6 of the Si3016. Conversely, a negative ringing signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2.

The first ring detect method uses the ring detect bits, RDTP, RDTN, and RDT. RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. Whenever the signal on RNG1-RNG2 is above the positive ring threshold, the RDTP bit is set. Whenever the signal on RNG1-RNG2 is below the negative ring threshold, the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFW bit is a 0 or a 1, a positive ringing signal will set the RDT bit for a period of time. The RDT bit will not be set for a negative ringing signal.

The RDT bit acts as a one shot. Whenever a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter counting down to zero, the RDT bit will return to zero. The length of this count (in seconds) is 65536 divided by the sample rate. The RDT will also be reset to zero by an off-hook event.

The second ring detect method uses the internal serial output of the integrated system-side module (SDO) to transmit ring data. If the link is active (PDL = 0) and the device is not off-hook or not in on-hook line monitor mode, the ring data will be sent by the system-side module to the host processor. The waveform on SDO depends on the state of the RFW bit.

When the RFW bit is 0, SDO will be -32768 (0x8000) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, SDO will transition to +32767 while the ring signal is positive, then go back to -32768 while the ring is near zero and negative. Thus, a near square wave is presented on SDO that swings from -32768 to +32767 in cadence with the ring signal.

When the RFW bit is 1, SDO will sit at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring goes positive, SDO will transition to +32767. When the ring signal goes near zero, SDO will remain near 1228. Then, as the ring goes negative, the SDO will transition to -32768. This will repeat in cadence with the ring signal.

The best way to observe the ring signal on SDO is simply to observe the MSB of the data. The MSB will toggle in cadence with the ring signal independent of the ring detector mode. This is adequate information for determining the ring frequency. The MSB of SDO will toggle at the same frequency as the ring signal.

## 4.12. Ringer Impedance

The ring detector in many DAAs is ac-coupled to the line with a large, 1  $\mu$ F, 250 V decoupling capacitor. The ring detector on the Si3016 is also capacitively coupled to the line, but it is designed to use smaller, less expensive 1.8 nF capacitors. Inherently, this network produces a high ringer impedance to the line of approximately 800 to 900 k $\Omega$ . This value is acceptable for the majority of countries, including FCC and CTR21.

Several countries including Poland, South Africa, and Slovenia, require a maximum ringer impedance that can be met with an internally-synthesized impedance by setting the RZ bit in Register 16.

### 4.13. DTMF Dialing

In CTR21 dc termination mode, the DIAL bit should be set during DTMF dialing if the LVCS[4:0] bits are less than 12. Setting this bit increases headroom for large signals. This bit should not be used during normal operation or if the LVCS[4:0] bits are greater than 11.

In Japan dc termination mode, the system-side module attenuates the transmit output by 1.7 dB to meet headroom requirements. Similarly, in Low Voltage termination mode, the system-side module attenuates the transmit output by 4 dB. However, when DTMF dialing is desired in these modes, this attenuation must be removed. This is achieved by entering the FCC dc termination mode and setting either the FJM or the FLVM bits. When in the FCC dc termination modes, these bits will enable the respective lower loop current termination modes without the associated transmit attenuation. Increased distortion may be observed, which is acceptable during DTMF dialing. After DTMF dialing is complete, the attenuation should be enabled by returning to either the Japan dc termination mode (DCT[1:0] = 01b) or the Low Voltage termination mode (DCT[1:0] = 00b). The FJM and the FLVM bits have no effect in any other termination mode other than the FCC dc termination mode.

Higher DTMF levels may also be achieved if the amplitude is increased and the peaks of the DTMF signal are clipped at digital full scale (as opposed to wrapping). Clipping the signal will produce some distortion and intermodulation of the signal. Generally, somewhat increased distortion (between 10–20%) is acceptable during DTMF signaling. Several dB higher DTMF levels can be achieved with this technique, compared with a digital full-scale peak signal.

### 4.14. Pulse Dialing

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have very tight specifications for pulse fidelity, including make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are a number of issues in meeting these requirements.

The Si3016 dc holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries, such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive dc feed, resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional way of

dealing with this problem is to put a parallel RC shunt across the hookswitch relay. The capacitor is large (~1  $\mu$ F, 250 V) and relatively expensive. In the Si3016, the OHS bit can be used to slowly ramp down the loop current to pass these tests without requiring additional components.

### 4.15. Billing Tone Detection

“Billing tones” or “metering pulses” generated by the central office can cause modem connection difficulties. The billing tone is typically either a 12 kHz or 16 kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major errors related to the modem data. The Si3016 has a feature that allows the device to provide feedback as to whether a billing tone has occurred and when it ends.

Billing tone detection is enabled by setting the BTE bit. Billing tones less than 1.1  $V_{PK}$  on the line will be filtered out by the low-pass digital filter on the Si3016. The ROV bit is set when a line signal is greater than 1.1  $V_{PK}$ , indicating a receive overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the line-side device (Si3016). When the BTD bit is set, the dc termination is changed to an 800  $\Omega$  dc impedance. This ensures minimum line voltage levels even in the presence of billing tones.

The OVL bit should be polled following a billing tone detection. When the OVL bit returns to zero, indicating that the billing tone has passed, the BTE bit should be written to zero to return the dc termination to its original state. It will take approximately one second to return to normal dc operating conditions. The BTD and ROV bits are sticky, and they must be written to zero to be reset. After the BTE, ROV, and BTD bits are all cleared, the BTE bit can be set to re-enable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. The user should look for multiple events before qualifying whether billing tones are actually present.

Although the DAA will remain off-hook during a billing tone event, the received data from the line will be corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries/customers.

Alternatively, when a billing tone is detected, the system software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

## 4.16. Billing Tone Filter (Optional)

In order to operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. (The Si3016 can remain off-hook during a billing tone event, but modem data will be lost in the presence of large billing tone signals.) The notch filter design requires two notches, one at 12 KHz and one at 16 KHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 14 shows an example billing tone filter.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 KHz and 16 KHz.

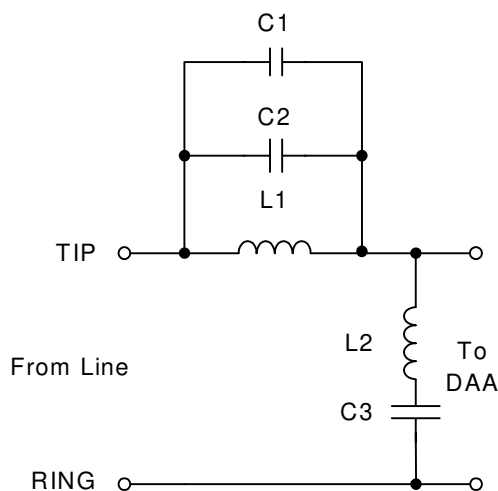


Figure 14. Billing Tone Filter

Table 11. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 $\mu$ F, 50 V, $\pm$ 10%
C3	0.01 $\mu$ F, 250 V, $\pm$ 10%
L1	3.3 mH, >120 mA, <10 $\Omega$ , $\pm$ 10%
L2	10 mH, >40 mA, <10 $\Omega$ , $\pm$ 10%

The billing tone filter affects the ac termination and return loss. The current complex ac termination will pass worldwide return loss specifications both with and without the billing tone filter by at least 3 dB. The ac termination is optimized for frequency response and hybrid cancellation, while having greater than 4 dB of margin with or without the dongle for South Africa, Australia, CTR21, German, and Swiss country-specific specifications.

## 4.17. On-Hook Line Monitor

The Si3016 allows the user to receive line activity when in an on-hook state. This is accomplished through a low-power ADC located on-chip that digitizes the signal passed across the RNG1/2 pins and then sends this signal digitally across the isolation link to the system-side module. This mode is typically used to detect caller ID data (see the “Caller ID” section). There are two low-power ADCs on the Si3016. One is enabled by setting the ONHM bit in Register 5. This ADC draws approximately 450  $\mu$ A of current from the line when activated. A lower-power ADC also exists on the Si3016, which enables a reduced current draw from the line of approximately 7  $\mu$ A. This lower power ADC is enabled by setting the MODE bit (in conjunction with the ONHM bit) to 1. (See the MODE bit description in the “Control Registers” section.) Regardless of which ADC is being used, the on-hook line monitor function must be disabled before the device is taken off-hook. Thus, ensure that the ONHM bit is cleared before setting the OH bit.

The signal to the lower power ADC can be attenuated to accommodate larger signals. This is accomplished through the use of the ARX[2:0] bits. It is important to note that while these ARX bits provide gain to the normal receive path of the DAA, they also function as attenuation bits for the on-hook line monitor low-power ADC. Attenuation settings include 0, 1, 2.2, 3.5, and 5 dB. It is recommended that the new lower-power ADC be used for on-hook line monitoring.

## 4.18. Caller ID

The Si3016 provides the designer with the ability to pass caller ID data from the phone line to a caller ID decoder connected to the serial port.

### 4.18.1. Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook.

In systems where the caller ID data is passed on the phone line between the first and second rings, the following method should be utilized to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in "4.11. Ring Detection" on page 18, determine when the first ring has completed.
2. Set the OFF/SQL2 bit. This bit resets the ac coupling network on the ring input in preparation for the caller ID data. This bit should not be cleared until after the caller ID data has been received.
3. Assert the MODE bit and then the ONHM bit. This enables the lower current caller ID ADC.
4. The low-power ADC (which is powered from the system chip, allowing for approximately 7  $\mu$ A current draw from the line) then digitizes the caller ID data passed across the RNG 1/2 pins and presents the data to the DSP via the SDO signal internal to the integrated system-side module.
5. Clear the ONHM, MODE, and OFF/SQL2 bits after the caller ID data has been received but prior to the start of the second ring.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, the following method should be used to capture the caller ID data:

1. Enable full wave rectified ring detection with the RFW bit.
2. Monitor the RDTP and RDTN register bits to identify whether a polarity reversal or a ring signal has occurred. A polarity reversal will trip either the RDTP or RDTN ring detection bits, and thus the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Once the signal has been identified as a battery reversal, the ac coupling network on the ring input must be reset in preparation for the caller ID data. Set the OFF/SQL2 bit. This bit should not be cleared until after the caller ID data has been received.
4. Assert the MODE bit and then the ONHM bit. This enables the lower current caller ID ADC.
5. The low-power ADC (which is powered from the system chip, allowing for approximately 7  $\mu$ A current draw from the line) then digitizes the caller ID data

passed across the RNG 1/2 pins and presents the data to the DSP via the SDO signal internal to the system-side module.

6. Clear the ONHM, MODE, and OFF/SQL2 bits after the caller ID data has been received but prior to the start of the second ring.

#### 4.18.2. Type II Caller ID

Type II Caller ID sends the CID data while the DAA is off-hook. This mode is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, the following procedure should be used (also see Figure 15):

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The host processor must detect the presence of this tone.
2. The DAA must then check to see if there is another parallel device on the same line. This is accomplished by briefly going on-hook, measuring the line voltage, and then returning to an off-hook state.
  - a. Set the CALD bit to 1. This disables the calibration that automatically occurs when going off-hook.
  - b. With the OH bit set to 1 and the ONHM bit set to 0, set the MODE bit to 1. This forces the DAA to go on-hook and disables the off-hook counter that is normally enabled when going back off-hook.
  - c. Read the LVCS bits to determine the state of the line.
  - d. If the LVCS bits read the typical on-hook line voltage, there are no parallel devices active on the line, and CID data reception can be continued.
  - e. If the LVCS bits read well below the typical on-hook line voltage, then there are one or more devices present and active on the same line that are not compliant with Type II CID. CID data reception should not be continued.
  - f. Set the MODE bit to 0 to return to an off-hook state.
3. Immediately after returning to an off-hook state, the ONHM bit must be set and left enabled for at least 30 ms. This allows the line voltage to settle before transmitting or receiving any data. After 30 ms, the ONHM bit should be disabled to allow normal data transmission and reception.

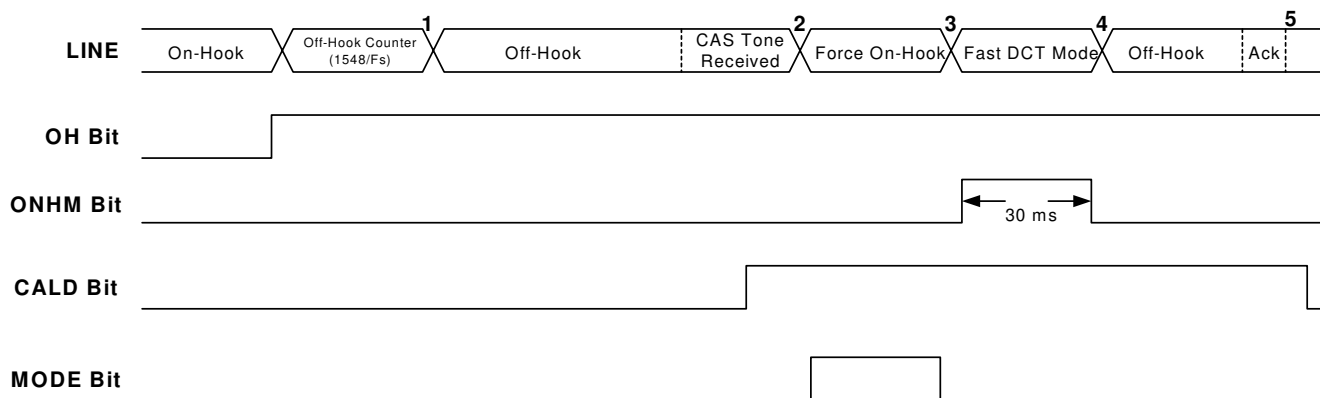




4. If a non-compliant parallel device is present, a reply tone is not sent by the host tone generator, and the CO does not proceed with sending the CID data.
5. If all devices on the line are Type II CID compliant, the host must mute its upstream data output to avoid the propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the host processor must then send an acknowledgement (ACK) tone back to the CO to request the transmission of the CID data.
6. The CO then responds with the CID data. After receiving this, the host processor unmutes the upstream data output and continues with normal

- operation.
7. The muting of the upstream data path by the host processor has the effect of muting the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.
8. The CALD bit can be set to 0 to reenables the automatic calibration when going off-hook.

Due to the nature of the low-power ADC, the data presented on SDO could have up to a 10% dc offset. The caller ID decoder must use either a high-pass or a band-pass filter to accurately retrieve the caller ID data.



#### Notes:

1. The off-hook counter is used to prevent transmission or reception of data for 1548/Fs to allow time for the line voltage to settle. If the CALD bit is 0, an automatic calibration will also be performed during this time.
2. The caller alert signal (CAS) tone is transmitted from the CO, which signals an incoming call.
3. When the MODE bit is set while the device is off-hook, the device is forced on-hook. This is done to read the line voltage in the LVCS bits to detect parallel handsets. In this mode, no data is transmitted on the SDO pin.
4. When the device returns off-hook after being forced on-hook using the MODE bit, the normal off-hook counter is disabled. Additionally, if the CALD bit is set, the automatic calibration will not be performed. The fast DCT mode must be manually enabled for at least 30 ms in order to properly settle the line voltage. This is done by setting the ONHM bit after disabling the MODE bit.
5. After allowing the line voltage to settle in fast DCT mode, normal off-hook mode should be entered by disabling the ONHM bit. If CID data reception is desired, the appropriate signal should be sent to the CO at this time.

**Figure 15. Implementing Type II Caller ID on the Si3016**

## 4.19. Overload Protection

The Si3016 can detect if an overload condition capable of damaging the DAA circuit is present. The DAA may be damaged if excessive line voltage or loop current is sustained.

The overload protection circuit utilizes the LVCS bits to determine an excessive line current or voltage per the LVCS bit transfer functions outlined in Figures 8 and 9.

When off-hook, if OPE is set and LVCS = 11111, the dc termination is disabled (800 Ω presented to the line), the hookswitch current is reduced, and the OPD bit is set.

**Note:** If the OPE bit is enabled before going off-hook, the overload protection circuit can be activated by the line transients produced by going off-hook. To avoid this, the OPE bit should be 0 prior to going off-hook. This bit can then be set ~25 ms after going off-hook to enable the overload protection feature.

## 4.20. Analog Output

The integrated system-side module that the Si3016 is connected to supports an analog output (AOUT) for driving the call progress speaker found with most of today's modems. AOUT is an analog signal that is comprised of a mix of the transmit and receive signals.

The receive portion of this mixed signal has a 0 dB gain, while the transmit signal has a gain of  $-20$  dB.

The transmit and receive signals of the AOUT signal have independent controls found in Register 6. The ATM[1:0] bits control the transmit portion, while the ARM[1:0] bits control the receive portion. The bits only affect the AOUT signal and do not affect the modem data. Figure 7 on page 11 illustrates a recommended application circuit. In the configuration shown, the LM386 provides a gain of 26 dB. Additional gain adjustments may be made by varying the voltage divider created by R1 and R3.

#### 4.21. Gain Control

The Si3016 supports multiple receive gain and transmit attenuation settings. The receive path can support gains of 0, 3, 6, 9, and 12 dB, as selected with the ARX[2:0] bits. The receive path can also be muted with the RXM bit. The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB, as selected with the ATX[2:0] bits. The transmit path can also be muted with the TXM bit.

The gain control bits, ARXB and ATXB, should be set to 0 at all times.

#### 4.22. Clocking

The system-side module that the Si3016 connects to is integrated onto a host processor and is thus clocked from the processor. The Si3016 receives all clocking from this system-side module and does not need any other clock inputs. The sample rate for the Si3016 is controlled by the Sample Rate Control register.

#### 4.23. Power Management

The Si3016 supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full powerdown mode. The power management modes are controlled by the PDN and PDL bits in Register 6.

On powerup or following a reset, the DAA is in reset operation. In this mode, the PDL bit is set while the PDN bit is cleared. The system-side module is fully operational except for the link. No communication between the system-side module and Si3016 can occur during reset operation. Note that any register bits associated with the Si3016 are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The DAA is fully operational, and the link is passing information between the system-side module and the Si3016. The desired sample rate should be programmed prior to entering this mode.

The Si3016 supports a low-power sleep mode. This

mode supports the popular wake-up-on-ring feature of many modems. To enable it, the PDN bit must be set and the PDL bit then cleared. When the Si3016 is in sleep mode, the host processor clock signal may be stopped or remain active to the system-side module, but it *must* be active before waking up the DAA. The system-side module is non-functional except for the link. To take the Si3016 out of sleep mode, the system-side module should be reset.

In summary, the powerdown/up sequence for sleep mode is as follows:

1. Set the PDN bit and clear the PDL bit.
2. The system-side module clock may stay active or stop.
3. Restore the system-side module clock before initiating the powerup sequence.
4. Reset the system-side module (after system-side module clock is present).
5. Program registers to desired settings.

The Si3016 also supports an additional power-down mode. When both the PDN and PDL bits are set, the chipset enters a complete power-down mode and draws negligible current (deep sleep mode). In this mode, the ring detect function does not operate. Normal operation may be restored using the same process for taking the DAA out of sleep mode.

#### 4.24. Calibration

The Si3016 initiates an auto-calibration by default whenever the device goes off-hook or experiences a loss in line power. Calibration is used to remove any offsets in the on-chip A/D converter that could affect the A/D dynamic range. Auto-calibration is typically initiated after the DAA dc termination stabilizes and takes  $512/F_s$  seconds to complete. Due to the large variation in line conditions and line card behavior that can be presented to the DAA, it may be beneficial to use manual calibration in lieu of auto-calibration.

Manual calibration should be executed as close to  $512/F_s$  seconds as possible before valid transmit/receive data is expected.

The following steps should be taken to implement manual calibration:

1. The CALD (auto-calibration disable) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to one and then zero to begin and complete the calibration.
3. The calibration will be completed in  $512/F_s$  seconds.

## 4.25. In-Circuit Testing

The Si3016's advanced design provides the designer with an increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Four loopback modes exist allowing increased coverage of system components. For three of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 1 on page 5 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side chip.

For the startup test mode, no line-side power is necessary and no off-hook sequence is required. The startup test mode is enabled by default. When the PDL bit is set (the default case), the line side is in a power-down mode and the system-side module is in a digital loop-back mode. In this mode, data received on SDI is passed through the internal filters and transmitted on SDO. This path will introduce approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters will exist between SDI and SDO. Clearing the PDL bit disables this mode, and the SDO data is switched to the receive data from the line-side. When the PDL bit is cleared, the FDT bit becomes active, indicating successful communication between the line-side and DSP-side. This can be used to verify that the isolation link is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirements:

1. Powerup or reset.
2. Program the desired sample rate.
3. Enable the line side by clearing the PDL bit.
4. Issue off-hook
5. Delay 1548/Fs sec to allow calibration to occur.
6. Set the desired test mode.

The isolation link digital loopback mode allows the data pump to provide a digital input test pattern on the system-side module and receive that digital test pattern back on the system-side module. To enable this mode, set the DL bit. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitor, C1, of Figure 6 on page 9 to the line side device and returned across the same barrier. Note that in this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive a signal on the telephone line into the Si3016 line-side device and have it driven back out onto the line. This mode allows testing of external components

connecting the RJ-11 jack (TIP and RING) to the Si3016. To enable this mode, set the AL bit.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit and receive paths on the line-side chip and the external components in Figure 6 on page 9. In this test mode, the data pump provides a digital test waveform on the system-side module. This data is passed across the isolation barrier, transmitted to and received from the line, passed back across the isolation barrier, and presented back to the data pump from the system-side module. To enable this mode, clear the HBE bit.

When the HBE bit is cleared, this will cause a dc offset which affects the signal swing of the transmit signal. In this test mode, it is recommended that the transmit signal be 12 dB lower than normal transmit levels. This lower level will eliminate clipping caused by the dc offset which results from disabling the hybrid. It is assumed in this test that the line ac impedance is nominally 600  $\Omega$ .

**Note:** All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

## 4.26. Exception Handling

The Si3016 provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit FDT. This bit indicates that the system-side module and line-side (Si3016) device are communicating. During normal operation, the FDT bit can be checked before reading any bits that indicate information about the line side. If FDT is not set, the following bits related to the line side are invalid: RDT, RDTN, RDTP, LCS[3:0], CBID, REVB[3:0], LVCS[4:0], ROV, BTD, DOD, OPD, and OVL.

Following powerup and reset, the FDT bit is not set because the PDL bit defaults to 1. In this state, the link is not operating, and no information about the line side can be determined. The user must program the desired sample rate and clear the PDL bit to activate the link. While the system and line side are establishing communication, the system-side does not generate  $\overline{\text{FSYNC}}$  signals. Establishing communication will take less than 10 ms.

The FDT bit can also indicate if the line side executes an off-hook request successfully. If the line side is not connected to a phone line (i.e., the user fails to connect a phone line to the modem), the FDT bit remains cleared. The controlling processor must allow sufficient time for the line side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT bit is high, the

LVCS[4:0] bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit in Register 6 must be set high for at least 1 ms to reset the line side.

Another useful bit is the communication link error (CLE) bit. The CLE bit indicates a timeout error for the isolation link. This condition indicates a severe error in programming or possibly a defective line-side chip.

#### 4.27. Revision Identification

The Si3016 provides the system designer the ability to determine the revision of the system-side module and/or the Si3016. The REVA[3:0] bits identify the revision of the system-side module. The REVB[3:0] and CBID bits identify the revision of the Si3016. Table 12 lists revision values for both chips.

**Table 12. Revision Values**

Revision	System-Side Module	Si3016
C	1010	—
D	—	1100
E	—	1101
F	—	1110