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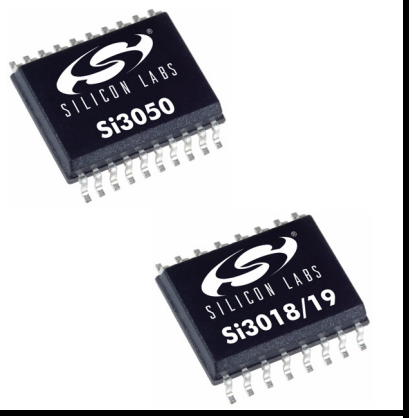
Si3050 + Si3018/19

GLOBAL VOICE DAA

Features

- PCM highway data interface
- μ-law/A-law companding
- SPI control interface
- GCI interface
- 80 dB dynamic range TX/RX
- Line voltage monitor
- Loop current monitor
- +6 dBm or +3.2 dBm TX/RX level mode
- Parallel handset detection
- 3 μA on-hook line monitor current
- Overload detection
- Programmable line interface
  - AC termination
  - DC termination
  - Ring detect threshold
  - Ringer impedance
- TIP/RING polarity detection
- Integrated codec and 2- to 4-wire analog hybrid
- Programmable digital hybrid for near-end echo reduction
- Polarity reversal detection
- Programmable digital gain in 0.1 dB increments
- Integrated ring detector
- Type I and II caller ID support
- Pulse dialing support
- 3.3 V power supply
- Daisy-chaining for up to 16 devices
- Greater than 5000 V isolation
- Patented isolation technology
- Ground start and loop start support
- Available in Pb-free RoHS-compliant packages



Ordering Information

See page 102.

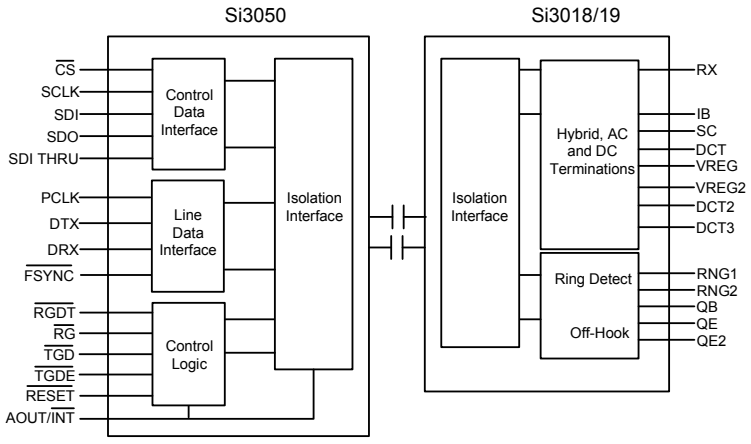
Applications

- DSL IADs
- VoIP gateways
- PBX and IP-PBX systems
- Voice mail systems

Description

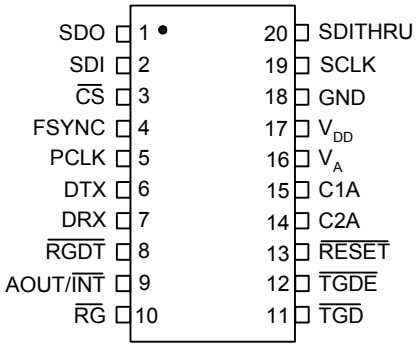
The Si3050+Si3018/19 Voice DAA chipset provides a highly-programmable and globally-compliant foreign exchange office (FXO) analog interface that is ideal for DSL IADs, PBXs, IP-PBXs, and VoIP gateway products. The solution implements Silicon Laboratories' patented isolation capacitor technology, which eliminates the need for costly isolation transformers, relays, or opto-isolators, while providing superior surge immunity for robust field performance. The Voice DAA is available in one 20-pin TSSOP (Si3050) and one 16-pin TSSOP/SOIC (Si3018/19) and requires minimal external components. The Si3050 interfaces directly to standard telephony PCM interfaces.

Functional Block Diagram

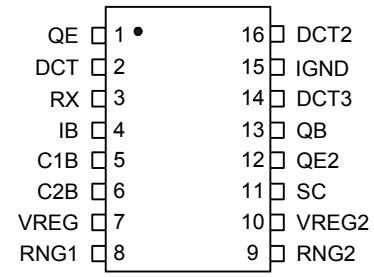


Pin Assignments

Si3050



Si3018/19



US Patent# 5,870,046
US Patent# 6,061,009
Other Patents Pending

TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions and Thermal Information

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	F/K-Grade	0	25	70	°C
		B/G-Grade	–40	25	85	
Si3050 Supply Voltage, Digital	V_D		3.0	3.3	3.6	V
Thermal Resistance (Si3018/19)[3]	θ_{JA}	SOIC-16	—	77	—	°C/W
		TSSOP-16	—	89	—	°C/W
Thermal Resistance (Si3050)[3]	θ_{JA}	TSSOP-20	—	84	—	°C/W

Notes:
1. The Si3050 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si3050 and any Si3018/19 are used. See "2. Typical Application Schematic" on page 17 for the typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. Operation above 125 °C junction temperature may degrade device reliability.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, see Figure 1 on page 6)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	40	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT2 = 0, RT = 0	13.5	15	16.5	V_{rms}
Ring Detect Voltage*	V_{RD}	RT2 = 0, RT = 1	19.35	21.5	23.65	V_{rms}
Ring Detect Voltage*	V_{RD}	RT2 = 1, RT = 1	40.5	45	49.5	V_{rms}
Ring Frequency	F_R		13	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

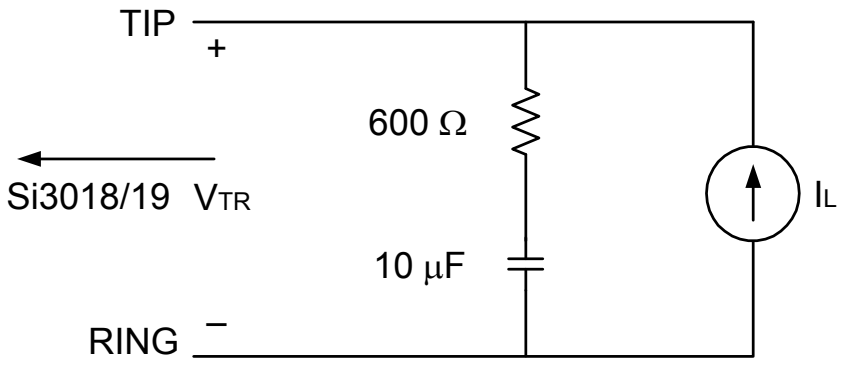


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage[1]	V_{IH}		2.0	—	—	V
Low Level Input Voltage[1]	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
AOUT High Level Voltage	V_{AH}	I_O = 10 mA	2.4	—	—	V
AOUT Low Level Voltage	V_{AL}	I_O = 10 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Digital[2]	I_D	V_D pin	—	8.5	10	mA
Total Supply Current, Sleep Mode[2]	I_D	PDN = 1, PDL = 0	—	5.0	6.0	mA
Total Supply Current, Deep Sleep[2,3]	I_D	PDN = 1, PDL = 1	—	1.3	1.5	mA

Notes:

1. V_{IH}/V_{IL} do not apply to C1A/C2A.
2. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs are held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
3. $\overline{\text{RGDT}}$ is not functional in this state.

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade, Fs = 8000 Hz, see "2. Typical Application Schematic" on page 17)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		8	—	16	kHz
PCLK Input Frequency	PCLK		256	—	8192	kHz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	—	200	—	Hz
Transmit Full-Scale Level[1]	V_{FS}	FULL = 0 (0 dBm)	—	1.1	—	V_{PEAK}
		FULL = 1 (+3.2 dBm)[2]	—	1.58	—	V_{PEAK}
		FULL2 = 1 (+6.0 dBm)[2]	—	2.16	—	V_{PEAK}
Receive Full-Scale Level[1,3]	V_{FS}	FULL = 0 (0 dBm)	—	1.1	—	V_{PEAK}
		FULL = 1 (+3.2 dBm)[2]	—	1.58	—	V_{PEAK}
		FULL2 = 1 (+6.0 dBm)[2]	—	2.16	—	V_{PEAK}
Dynamic Range[4,5,6]	DR	ILIM = 0, DCV = 11, MINI=00 DCR = 0, I_L = 100 mA	—	80	—	dB
Dynamic Range[4,5,6]	DR	ILIM = 0, DCV = 00, MINI=11 DCR = 0, I_L = 20 mA	—	80	—	dB
Dynamic Range[4,5,6]	DR	ILIM = 1, DCV = 11, MINI=00 DCR = 0, I_L = 50 mA	—	80	—	dB
Transmit Total Harmonic Distortion[6,7]	THD	ILIM = 0, DCV = 11, MINI=00 DCR = 0, I_L = 100 mA	—	–72	—	dB
Transmit Total Harmonic Distortion[6,7]	THD	ILIM = 0, DCV = 00, MINI=11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ILIM = 0, DCV = 00, MINI=11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ILIM = 1,DCV = 11, MINI=00 DCR = 0, I_L = 50 mA	—	–78	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 6.
2. With FULL = 1, the transmit and receive full-scale level of +3.2 dBm can be achieved with a 600 Ω ac termination. While the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances. With FULL2 = 1, the transmit and receive full-scale level of +6.0 dBm can be achieved with a 600 Ω termination. In this mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
3. Receive full-scale level produces –0.9 dBFS at DTX.
4. DR = 20 x log (RMS V_{FS}/RMS Vin) + 20 x log (RMS V_{in}/RMS noise). The RMS noise measurement excludes harmonics. Here, V_{FS} is the 0 dBm full-scale level per Note 1 above.
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6. Vin = 1 kHz, –3 dBFS.
7. THD = 20 x log (RMS distortion/RMS signal).
8. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{CID} is the 1.5 V full-scale level with the enhanced caller ID circuit. With the typical CID circuit, the V_{CID} full-scale level is 6 V peak, and the DR_{CID} decreases to 50 dB.
9. Refer to Tables 10–11 for relative gain accuracy characteristics (passband ripple).
10. Analog hybrid only. Z_{ACIM} controlled by ACIM in Register 30.

Table 4. AC Characteristics (Continued)

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade, Fs = 8000 Hz, see "2. Typical Application Schematic" on page 17)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Range (Caller ID mode)[8]	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	62	—	dB
Caller ID Full-Scale Level[8]	V_{CID}		—	1.5	—	V_{PEAK}
Gain Accuracy[6,9]		2-W to DTX, TXG2, RXG2, TXG3, and RXG3 = 0000	–0.5	0	0.5	dB
Transhybrid Balance[10]		300–3.4 kHz, $Z_{ACIM} = Z_{LINE}$	20	—	—	dB
Transhybrid Balance[10]		1 kHz, $Z_{ACIM} = Z_{LINE}$	—	30	—	dB
Two-Wire Return Loss		300–3.4 kHz, all ac terminations	25	—	—	dB
Two-Wire Return Loss		1 kHz, all ac terminations	—	32	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 6.
2. With FULL = 1, the transmit and receive full-scale level of +3.2 dBm can be achieved with a 600 Ω ac termination. While the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances. With FULL2 = 1, the transmit and receive full-scale level of +6.0 dBm can be achieved with a 600 Ω termination. In this mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
3. Receive full-scale level produces –0.9 dBFS at DTX.
4. DR = 20 x log (RMS V_{FS}/RMS Vin) + 20 x log (RMS V_{in}/RMS noise). The RMS noise measurement excludes harmonics. Here, V_{FS} is the 0 dBm full-scale level per Note 1 above.
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6. Vin = 1 kHz, –3 dBFS.
7. THD = 20 x log (RMS distortion/RMS signal).
8. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{CID} is the 1.5 V full-scale level with the enhanced caller ID circuit. With the typical CID circuit, the V_{CID} full-scale level is 6 V peak, and the DR_{CID} decreases to 50 dB.
9. Refer to Tables 10–11 for relative gain accuracy characteristics (passband ripple).
10. Analog hybrid only. Z_{ACIM} controlled by ACIM in Register 30.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 3.6	V
Input Current, Si3050 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Ambient Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage can occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

Table 6. Switching Characteristics—General Inputs

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, PCLK	t_p	0.12207	—	3.90625	µs
PCLK Duty Cycle	t_{dty}	40	50	60	%
PCLK Jitter Tolerance	t_{jitter}	—	—	2	ns
Rise Time, PCLK	t_r	—	—	25	ns
Fall Time, PCLK	t_f	—	—	25	ns
PCLK Before $\overline{\text{RESET}}$ ↑[2]	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[3]	t_{rl}	250	—	—	ns
$\overline{\text{CS}}$, SCLK Before $\overline{\text{RESET}}$↑	t_{mxr}	20	—	—	ns
Rise Time, Reset	t_r	—	—	25	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC/PCLK relationship must be fixed after $\overline{\text{RESET}}$↑.
3. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 PCLK cycle times.

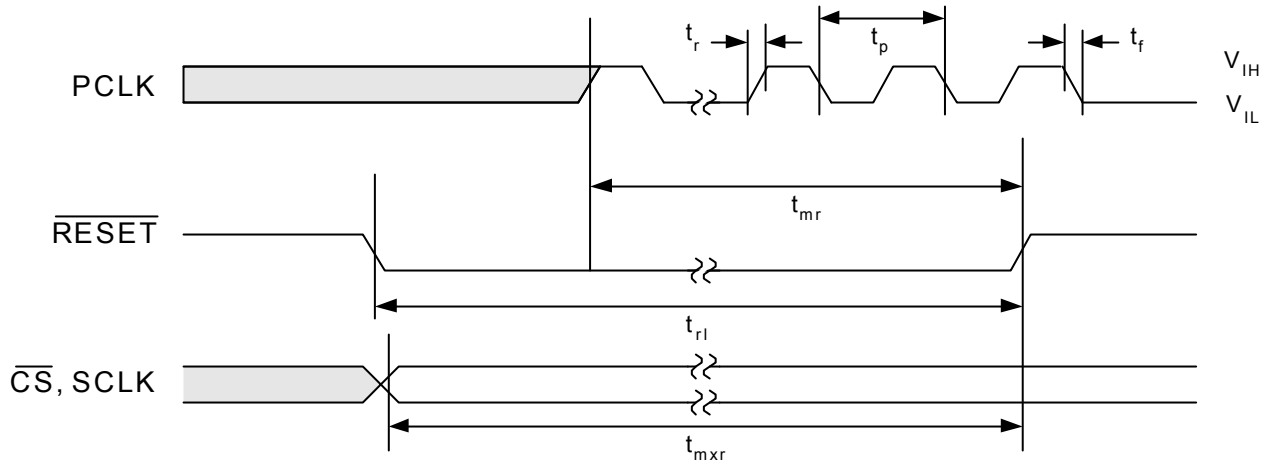


Figure 2. General Inputs Timing Diagram

Table 7. Switching Characteristics—Serial Peripheral Interface

(V_{IO} = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter*	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		61.03	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{CS}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SCLK to $\overline{CS}$ Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SCLK Rise to SDI Transition	t_{h2}		20	—	—	ns
Delay time between chip selects	t_{cs}		220	—	—	ns
Propagation Delay, SDI to SDITHRU			—	6	—	ns

***Note:** All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

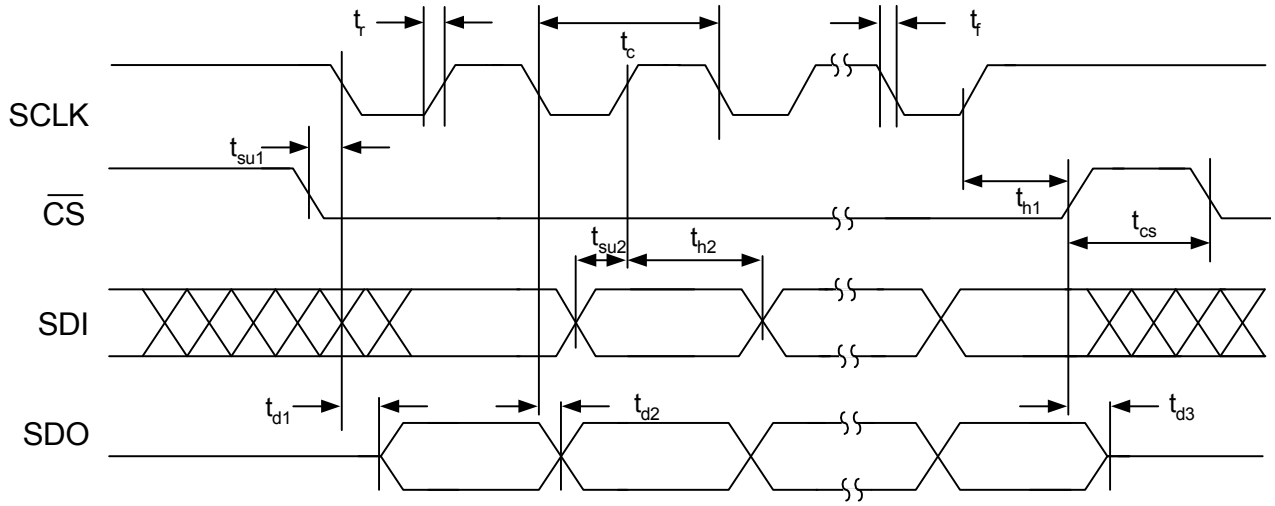


Figure 3. SPI Timing Diagram

Table 8. Switching Characteristics—PCM Highway Serial Interface

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
Cycle Time PCLK	t_p		122	—	3906	ns
Valid PCLK Inputs			— — — — — — — —	256 512 768 1.024 1.536 2.048 4.096 8.192	— — — — — — — —	kHz kHz kHz MHz MHz MHz MHz MHz
FSYNC Period[2]	t_{fp}		—	125	—	µs
PCLK Duty Cycle	t_{dty}		40	50	60	%
PCLK Jitter-Tolerance	t_{jitter}		—	—	2	ns
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-State[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O - 0.4$ V, V_{IL} = 0.4 V, rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC must be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tri-state when that mode is selected.

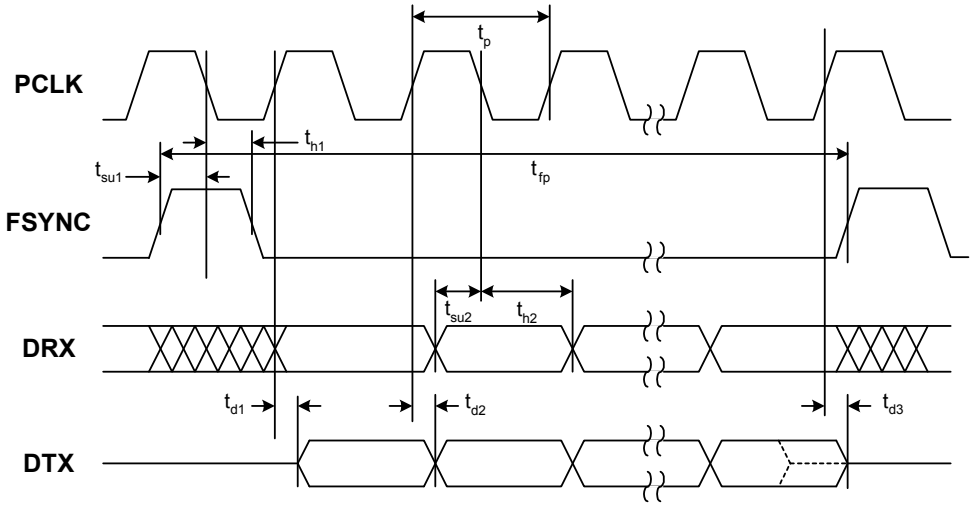


Figure 4. PCM Highway Interface Timing Diagram (RXS = TXS = 1)

Table 9. Switching Characteristics—GCI Highway Serial Interface

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
Cycle Time PCLK (Single Clocking Mode)	t_p		—	488	—	ns
Cycle Time PCLK (Double Clocking Mode)	t_p		—	244	—	ns
Valid PCLK Inputs			— —	2.048 4.096	— —	MHz MHz
FSYNC Period[2]	t_{fp}		—	125	—	µs
PCLK Duty Cycle	t_{dty}		40	50	60	%
PCLK Jitter Tolerance	t_{jitter}		—	—	2	ns
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-State[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns

Notes:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O - 0.4$ V, V_{IL} = 0.4 V, rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC must be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tri-state when that mode is selected.

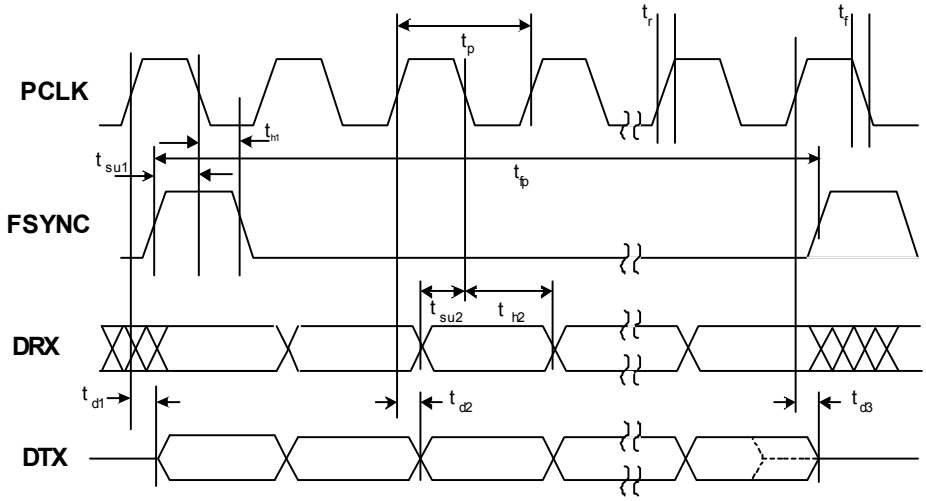


Figure 5. GCI Highway Interface Timing Diagram (1x PCLK Mode)

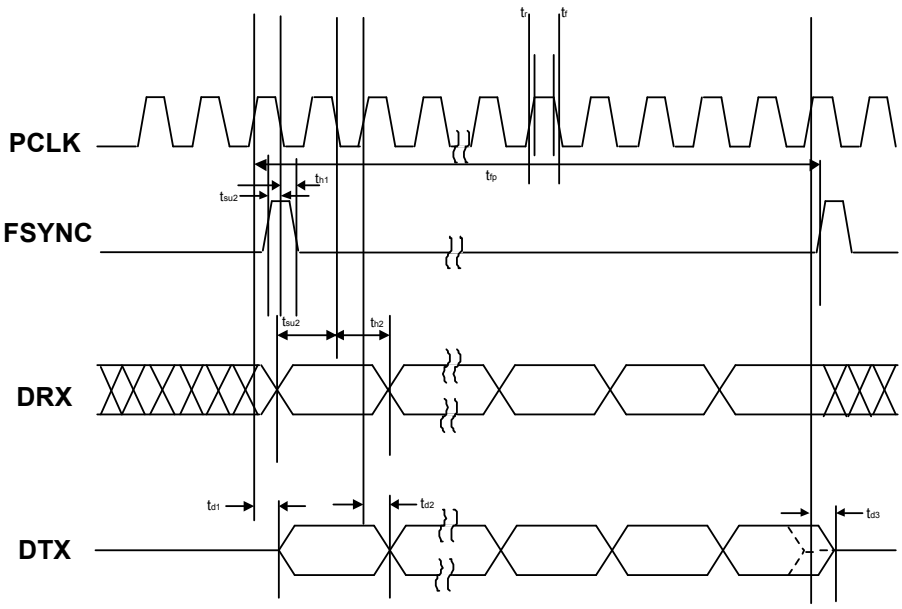


Figure 6. GCI Highway Interface Timing Diagram (2x PCLK Mode)

Table 10. Digital FIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 7, 8, 9, and 10.					

Table 11. Digital IIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	s
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 11, 12, 13, and 14. Figures 15 and 16 show group delay versus input frequency.					

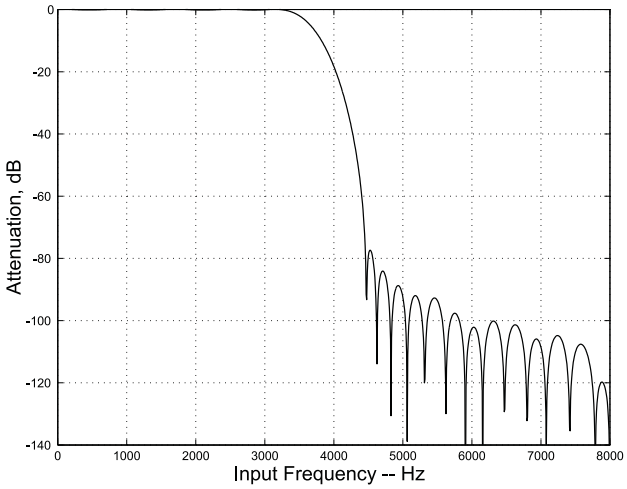


Figure 7. FIR Receive Filter Response

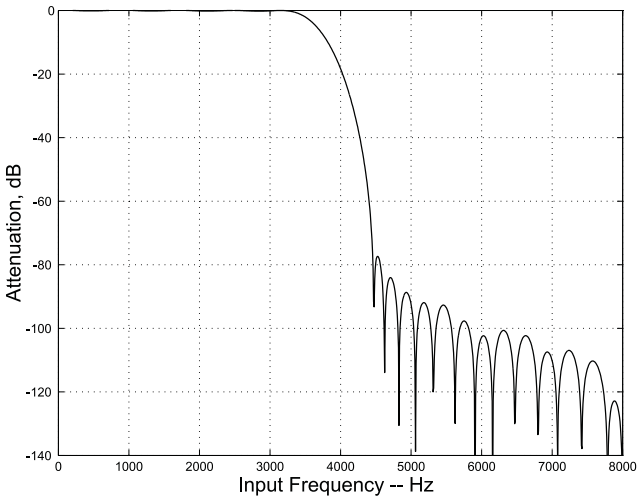


Figure 9. FIR Transmit Filter Response

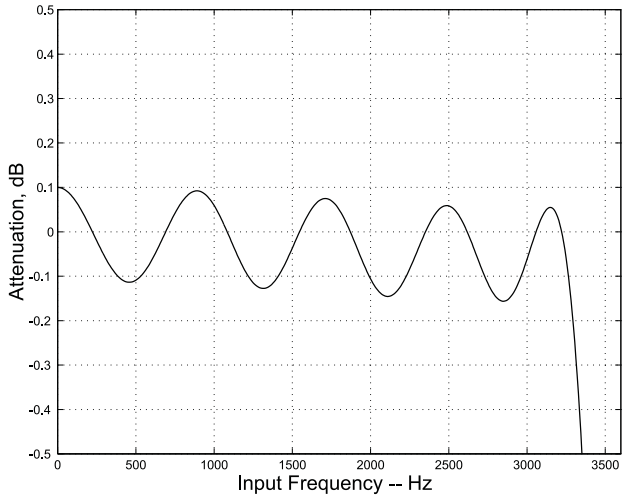


Figure 8. FIR Receive Filter Passband Ripple

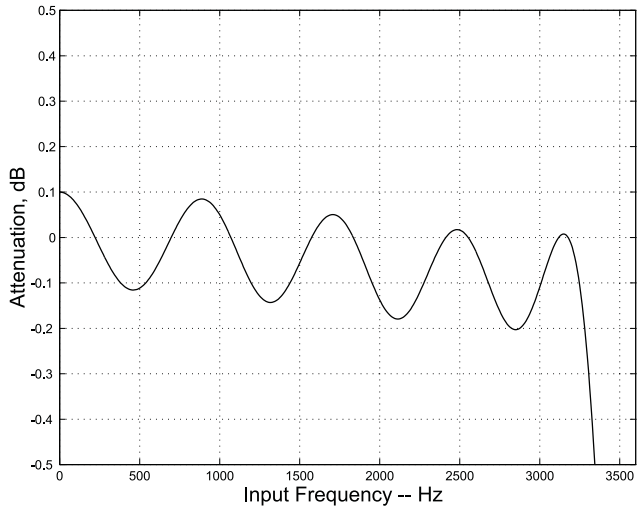


Figure 10. FIR Transmit Filter Passband Ripple

For Figures 7–10, all filter plots apply to a sample rate of Fs = 8 kHz.

For Figures 11–14, all filter plots apply to a sample rate of Fs = 8 kHz.

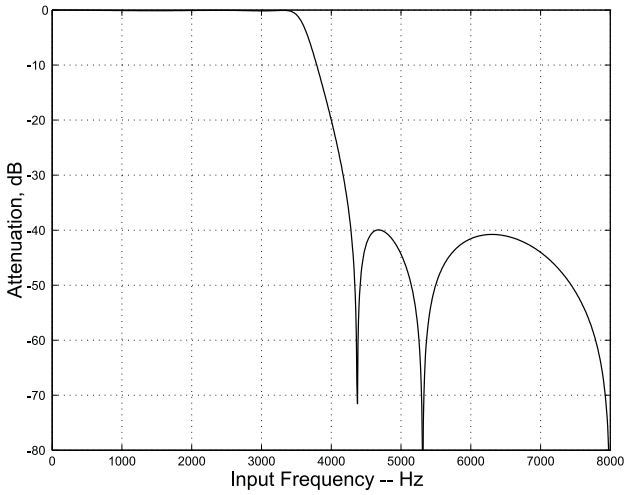


Figure 11. IIR Receive Filter Response

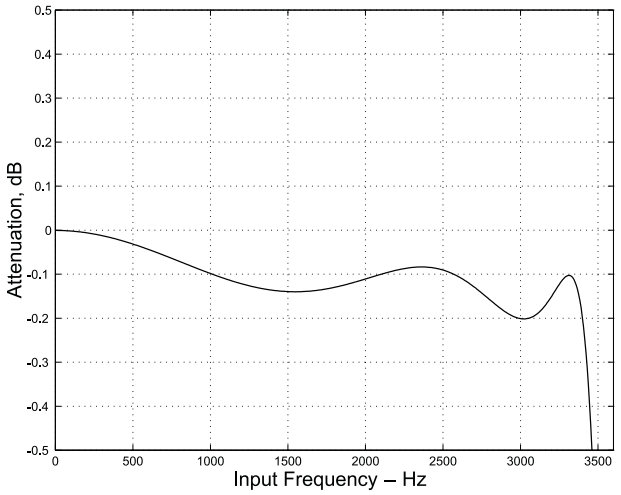


Figure 14. IIR Transmit Filter Passband Ripple

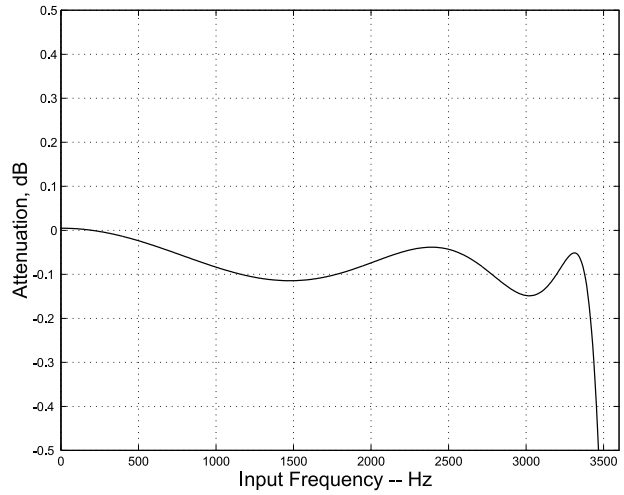


Figure 12. IIR Receive Filter Passband Ripple

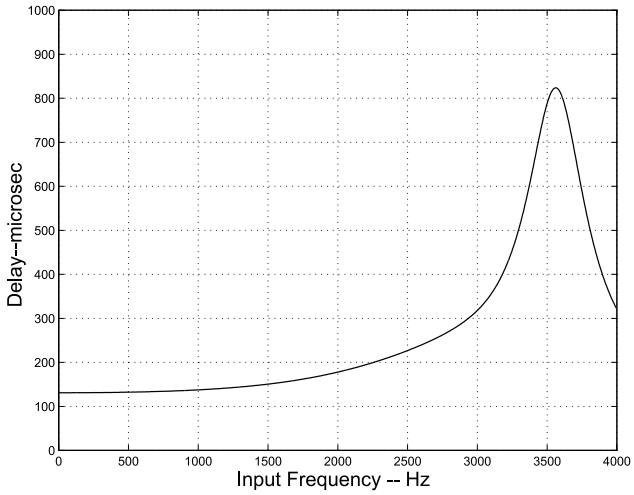


Figure 15. IIR Receive Group Delay

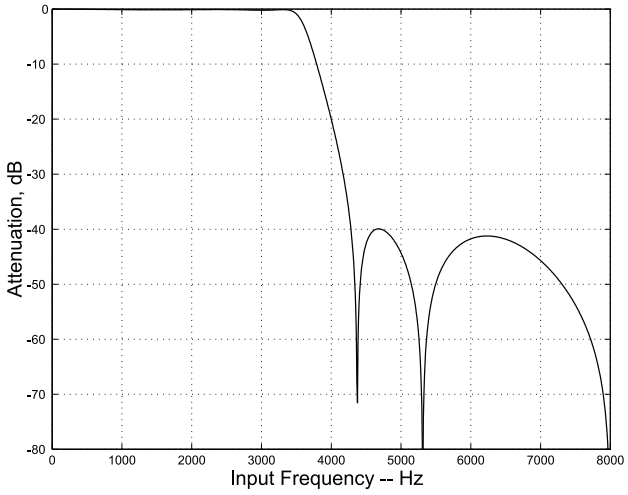


Figure 13. IIR Transmit Filter Response

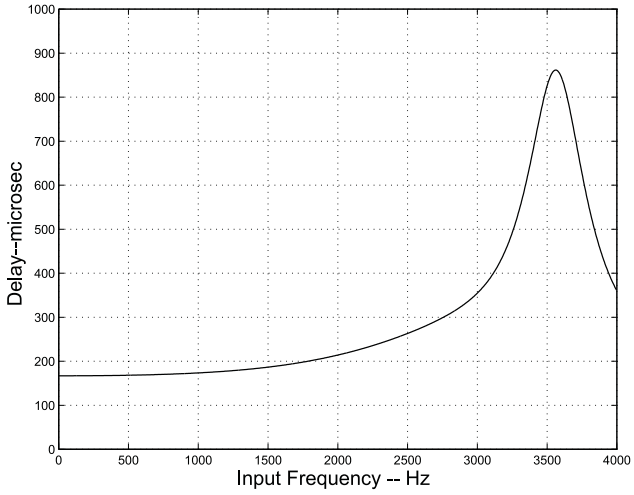


Figure 16. IIR Transmit Group Delay

2. Typical Application Schematic

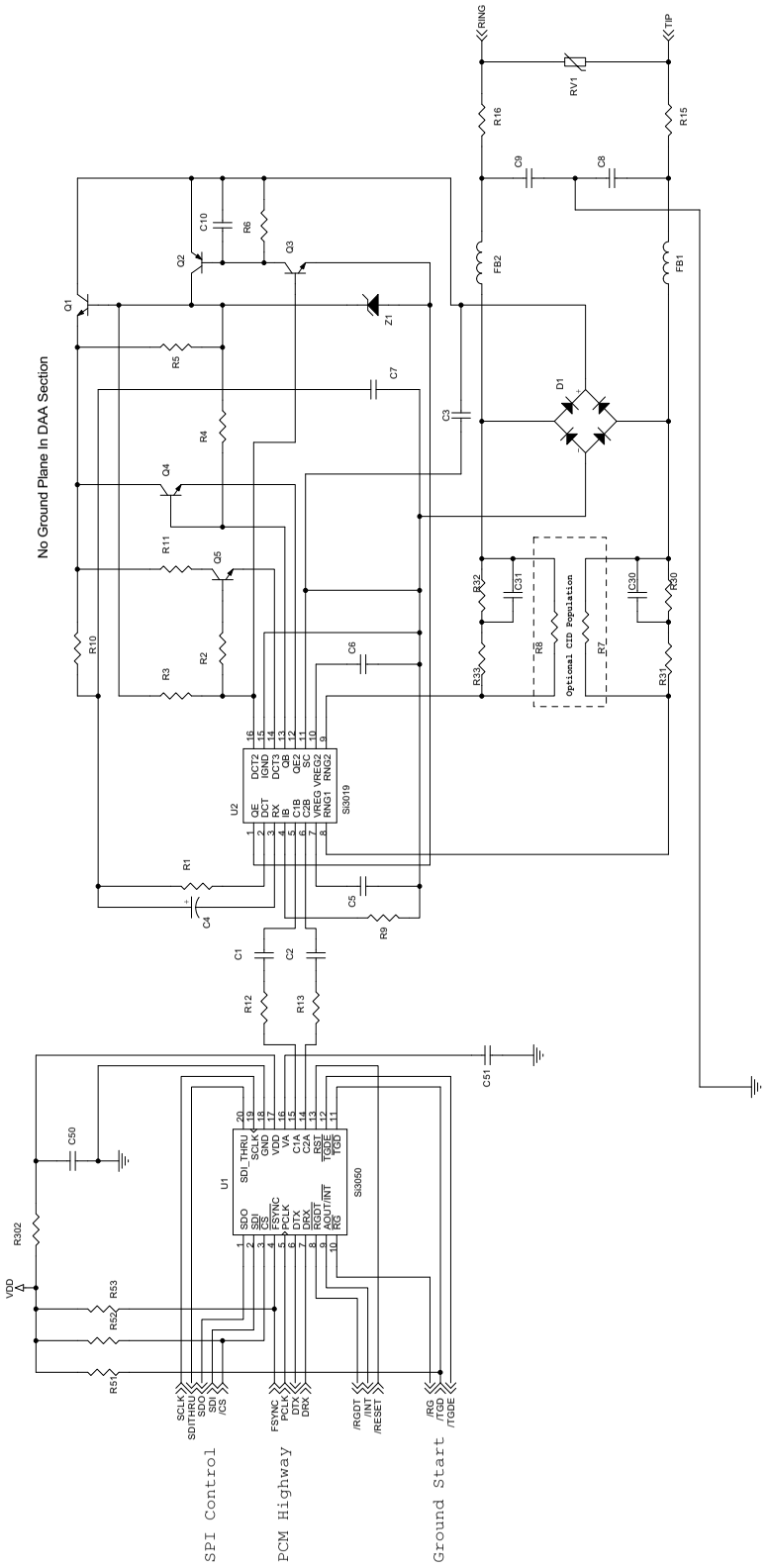


Figure 17. Typical Application Circuit for the Si3050 and Si3018/19
(Refer to "AN67: Si3050/52/54/56 Layout Guidelines" for Recommended Layout Guidelines)

3. Bill of Materials

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3[1]	3.9 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C51	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 µF, 16 V, X7R, ±20%	Venkel, SMEC
C30, C31[1]	120 pF, 250 V, X7R, ±10%	Venkel, SMEC
D1, D2[2]	Dual Diode, 225 mA, 300 V, (CMPD2004S)	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM18AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	Central OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	Central OnSemi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	Central OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Diodes Inc., Shindengen
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8[1]	Not Installed, 20 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13[3]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R15, R16[4]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R30, R32[1]	15 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R31, R33[1]	5.1 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R51, R52, R53	4.7 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
U1	Si3050	Silicon Labs
U2	Si3018/19	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	General Semi, On Semi, Diodes Inc.

Notes:

1. R7–R8 may be substituted for R30–R33 and C30–C31 for lower cost, but reduced CID performance.
2. Several diode bridge configurations are acceptable. Parts, such as a single HD04, a DF-04S, or four 1N4004 diodes, may be used (suppliers include General Semiconductor, Diodes Inc., etc.).
3. 56 Ω, 1/16, 1% resistors may be substituted for R12–R13 (0 Ω) to decrease emissions. (See AN81.)
4. Murata BLM18AG601SN1 may be substituted for R15–R16 (0 Ω) to decrease emissions. (See AN81.)

4. AOUT PWM Output

Figure 18 illustrates an optional circuit to support the pulse width modulation (PWM) output capability of the Si3050 for call progress monitoring purposes.To enable this mode, the INTE bit (Register 2) should be set to 0, the PWME bit (Register 1) set to 1, and the PWMM bits (Register 2) set to 00.

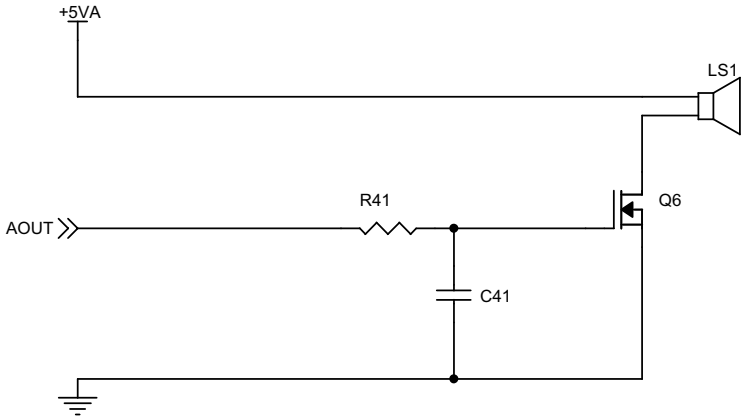


Figure 18. AOUT PWM Circuit for Call Progress

Table 12. Component Values—AOUT PWM

Component	Value	Supplier
LS1	Speaker BRT1209PF-06	Intervox
Q6	NPN KSP13	Fairchild
C41	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
R41	150 Ω, 1/10 W, ±5%	Venkel, SMEC, Panasonic

Registers 20 and 21 allow the receive and transmit paths to be attenuated linearly. When these registers are set to all 0s, the transmit and receive paths are muted. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

The PWMM[1:0] bits (Register 1, bits 5:4) select one of three different PWM output modes for the AOUT signal, including a delta-sigma data stream, a 32 kHz return to 0 PWM output, and a balanced 32 kHz PWM output.

5. Functional Description

The Si3050 is an integrated direct access arrangement (DAA) providing a programmable line interface that meets global telephone line requirements. The Si3050 implements Silicon Laboratories' patented isolation capacitor technology, which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two highly-integrated ICs.

The Si3050 DAA is fully software programmable to meet global requirements and is compliant with FCC, TBR21, JATE, and other country-specific PTT specifications as shown in Table 13. In addition, the Si3050 meets the most stringent global requirements for out-of-band energy, emissions, immunity, high-voltage surges, and safety, including FCC Parts 15 and 68, EN55022, EN55024, and many other standards.

5.1. Line-Side Device Support

Two different line-side devices are available for use with the Si3050 system-side device. Both line-side devices support the following features:

- Global compliance.
- Selectable 5 Hz or 200 Hz RX low-pass filter pole.
- –16.5 to 13.5 dB digital gain/attenuation adjustment in 0.1 dB increments for the transmit and receive paths.

5.1.1. Si3018

- Globally-compliant line-side device—targets global DAA requirements for voice applications. This line-side device supports both FCC-compliant countries and non-FCC-compliant countries.
  - Selectable dc terminations.
  - Four selectable ac terminations to increase return loss and trans-hybrid loss performance.
  - +6 dBm TX/RX level mode (600 Ω)

5.1.2. Si3019

- Globally-compliant, enhanced features line-side device—targets global DAA requirements for voice applications.
  - Selectable dc terminations
  - Sixteen selectable ac terminations to further increase return loss and trans-hybrid loss performance.
  - Line voltage monitoring in on- and off-hook modes to enable line in-use/parallel handset detection.
  - Programmable line current / voltage threshold interrupt.
  - Polarity reversal interrupt.
  - +3.2 dBm TX/RX level mode (600 Ω)
  - +6 dBm TX/RX level mode (600 Ω)
  - Higher resolution (1.1 mA/bit) loop current measurement.

Table 13. Country Specific Register Settings

Register	16	31	16	16	26	26	26	30
Country	**OHS**	**OHS2**	**RZ**	**RT**	**ILIM**	**DCV[1:0]**	**MINI[1:0]**	**ACIM[3:0]**
Argentina	0	0	0	0	0	11	00	0000
Australia[1]	1	0	0	0	0	01	01	0011
Austria	0	1	0	0	1	11	00	0010
Bahrain	0	1	0	0	1	11	00	0010
Belgium	0	1	0	0	1	11	00	0010
Brazil	0	0	0	0	0	11	00	0001
Bulgaria	0	1	0	0	1	11	00	0011
Canada	0	0	0	0	0	11	00	0000
Chile	0	0	0	0	0	11	00	0000
China	0	0	0	0	0	11	00	1010
Colombia	0	0	0	0	0	11	00	0000
Croatia	0	1	0	0	1	11	00	0010
Cyprus	0	1	0	0	1	11	00	0010
Czech Republic	0	1	0	0	1	11	00	0010
Denmark	0	1	0	0	1	11	00	0010
Ecuador	0	0	0	0	0	11	00	0000
Egypt	0	1	0	0	1	11	00	0010
El Salvador	0	0	0	0	0	11	00	0000
Finland	0	1	0	0	1	11	00	0010
France	0	1	0	0	1	11	00	0010
Germany	0	1	0	0	1	11	00	0010
Greece	0	1	0	0	1	11	00	0010
Guam	0	0	0	0	0	11	00	0000
Hong Kong	0	0	0	0	0	11	00	0000
Hungary	0	1	0	0	1	11	00	0010
Iceland	0	1	0	0	1	11	00	0010
India	0	0	0	0	0	11	00	0000
Indonesia	0	0	0	0	0	11	00	0000

Note:

1. See "5.16. DC Termination" on page 30 for DCV and MINI settings.
2. Supported for loop current ≥ 20 mA.
3. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.

Table 13. Country Specific Register Settings (Continued)

Register	16	31	16	16	26	26	26	30
Country	**OHS**	**OHS2**	**RZ**	**RT**	**ILIM**	**DCV[1:0]**	**MINI[1:0]**	**ACIM[3:0]**
Ireland	0	1	0	0	1	11	00	0010
Israel	0	1	0	0	1	11	00	0010
Italy	0	1	0	0	1	11	00	0010
Japan	0	0	0	0	0	10	01	0000
Jordan	0	0	0	0	0	01	01	0000
Kazakhstan	0	0	0	0	0	11	00	0000
Kuwait	0	0	0	0	0	11	00	0000
Latvia	0	1	0	0	1	11	00	0010
Lebanon	0	1	0	0	1	11	00	0010
Luxembourg	0	1	0	0	1	11	00	0010
Macao	0	0	0	0	0	11	00	0000
Malaysia[2]	0	0	0	0	0	01	01	0000
Malta	0	1	0	0	1	11	00	0010
Mexico	0	0	0	0	0	11	00	0000
Morocco	0	1	0	0	1	11	00	0010
Netherlands	0	1	0	0	1	11	00	0010
New Zealand	0	0	0	0	0	11	00	0100
Nigeria	0	1	0	0	1	11	00	0010
Norway	0	1	0	0	1	11	00	0010
Oman	0	0	0	0	0	01	01	0000
Pakistan	0	0	0	0	0	01	01	0000
Peru	0	0	0	0	0	11	00	0000
Philippines	0	0	0	0	0	01	01	0000
Poland	0	1	0	0	1	11	00	0010
Portugal	0	1	0	0	1	11	00	0010
Romania	0	1	0	0	1	11	00	0010
Russia	0	0	0	0	0	11	00	0000
Saudi Arabia	0	0	0	0	0	11	00	0000
Singapore	0	0	0	0	0	11	00	0000

Note:

1. See "5.16. DC Termination" on page 30 for DCV and MINI settings.
2. Supported for loop current ≥ 20 mA.
3. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.

Table 13. Country Specific Register Settings (Continued)

Register	16	31	16	16	26	26	26	30
Country	**OHS**	**OHS2**	**RZ**	**RT**	**ILIM**	**DCV[1:0]**	**MINI[1:0]**	**ACIM[3:0]**
Slovakia	0	1	0	0	1	11	00	0010
Slovenia	0	1	0	0	1	11	00	0010
South Africa	0	0	1	0	0	11	00	0011
South Korea	0	0	1	0	0	11	00	0000
Spain	0	1	0	0	1	11	00	0010
Sweden	0	1	0	0	1	11	00	0010
Switzerland	0	1	0	0	1	11	00	0010
Taiwan	0	0	0	0	0	11	00	0000
TBR21[3]	0	0	0	0	1	11	00	0010
Thailand	0	0	0	0	0	01	01	0000
UAE	0	0	0	0	0	11	00	0000
United Kingdom	0	1	0	0	1	11	00	0101
USA	0	0	0	0	0	11	00	0000
Yemen	0	0	0	0	0	11	00	0000

Note:

1. See "5.16. DC Termination" on page 30 for DCV and MINI settings.
2. Supported for loop current ≥ 20 mA.
3. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.

5.2. Power Supplies

The Si3050 operates from a 3.3 V power supply. The Si3050 input pins can only accept 3.3 V CMOS signal levels. If support of 5 V signal levels is necessary, a level shifter is required. The Si3018/19 derives its power from two sources: the Si3050 and the telephone line. The Si3050 supplies power over the patented isolation capacitor link between the two devices, allowing the Si3019 to communicate with the Si3050 while on-hook and perform other on-hook functions, such as line voltage monitoring. When off-hook, the Si3018/19 also derives power from the line current supplied from the telephone line. This feature is exclusive to DAAs from Silicon Labs and allows the most cost-effective implementation for a DAA while still maintaining robust performance over all line conditions.

5.3. Initialization

Each time the Si3050 is powered up, assert the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is deasserted, the registers have default values to guarantee the line-side device (Si3018/19) is powered down without the possibility of loading the line (i.e., off-hook). An example initialization procedure follows:

1. Power up and de-assert $\overline{\text{RESET}}$.
2. Wait until the PLL is locked. This time is less than 1 ms from the application of PCLK.
3. Enable PCM (Register 33) or GCI (Register 42) mode.
4. Set the desired line interface parameters (i.e., DCV[1:0], MINI[1:0], ILIM, DCR, ACIM[3:0], OHS, RT, RZ, TGA2, and TXG2[3:0]) shown in Table 13 on page 21.
5. Set the FULL (or FULL2) + IIRE bits as required.
6. Write a 0x00 into Register 6 to power up the line-side device (Si3018/19).

When this procedure is complete, the Si3018/19 is ready for ring detection and off-hook operation.

5.4. Isolation Barrier

The Si3050 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' patented signal processing techniques. Differential capacitive communication eliminates signal degradation from capacitor mismatches, common mode interference, or noise coupling. As shown in the "2. Typical Application Schematic" on page 17, the C1, C2, C8, and C9 capacitors isolate the Si3050 (system-side) from the Si3018/19 (line-side). Transmit, receive, control, ring detect, and caller ID data are passed across this barrier.

The communications link is disabled by default. To enable it, the PDL bit (Register 6, bit 4) must be cleared. No communication between the Si3050 and Si3018/19 can occur until this bit is cleared. Allow the PLL to lock to the PCLK and FSYNC input signals before clearing the PDL bit.

5.5. Power Management

The Si3050 supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full powerdown mode. The power management modes are controlled by the PDN and PDL bits (Register 6).

On powerup, or following a reset, the Si3050 is in reset operation. The PDL bit is set, and the PDN bit is cleared. The Si3050 is operational, except for the communications link. No communication between the Si3050 and line-side device (Si3018/19) can occur during reset operation. Bits associated with the line-side device are invalid in this mode.

In typical applications, the DAA will predominantly be operated in normal mode. In normal mode, the PDL and PDN bits are cleared. The DAA is operational and the communications link passes information between the Si3050 and the Si3018 or Si3019.

The Si3050 supports a low-power sleep mode that supports ring validation and wake-up-on-ring features. To enable the sleep mode, the PDN bit must be set. When the Si3050 is in sleep mode, the PCLK signal must remain active. In low-power sleep mode, the Si3050 is non-functional except for the communications link and the $\overline{\text{RGDT}}$ signal. To take the Si3050 out of sleep mode, pulse the reset pin ($\overline{\text{RESET}}$) low.

In summary, the powerdown/up sequence for sleep mode is as follows:

1. Ensure the PDL bit (Register 6, bit 4) is cleared.
2. Set the PDN bit (Register 6, bit 3).
3. The device is now in sleep mode. PCLK must remain active.
4. To exit sleep mode, reset the Si3050 by pulsing the $\overline{\text{RESET}}$ pin.
5. Program registers to desired settings.

The Si3050 also supports an additional Powerdown mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) bits are set, the chipset enters a complete powerdown mode and draws negligible current (deep sleep mode). In this mode, the Si3050 is non-functional. The $\overline{\text{RGDT}}$ pin does not function and the Si3050 will not detect a ring. Normal operation can be restored using the same process for taking the Si3050 out of sleep mode.

5.6. Calibration

The Si3050 initiates two auto-calibrations by default when the device goes off-hook or experiences a loss of line power. A 17 ms resistor calibration is performed to allow circuitry internal to the DAA to adjust to the exact line conditions present at the time of going off-hook. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5). A 256 ms ADC calibration is also performed to remove offsets that might be present in the on-chip A/D converter, which could affect the A/D dynamic range. The ADC auto-calibration is initiated after the DAA dc termination stabilizes and the resistor calibration completes. Due to the large variation in line conditions and line card behavior presented to the DAA, it might be beneficial to use manual ADC calibration instead of auto-calibration.

Manual ADC calibration should be executed as close as possible to 256 ms before valid transmit/receive data is expected.

The following steps should be taken to implement manual ADC calibration:

1. The CALD bit (auto-calibration disable—Register 17) must be set to 1.
2. The MCAL bit (manual calibration) must be toggled to one and then 0 to begin and complete the calibration.
3. The calibration is completed in 256 ms.

5.7. In-Circuit Testing

The Si3050's advanced design provides the designer with an increased ability to determine system functionality during production line tests and support for end-user diagnostics. Six loopback modes allow increased coverage of system components. For four of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 1 on page 6 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side device.

For the start-up loopback test mode, no line-side power is necessary, and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line side is in a powerdown mode, and the system-side is in a digital loopback mode. In this mode, data received on DRX passes through the internal filters and is transmitted on DTX. This path introduces approximately 0.9 dB of attenuation on the DRX signal received. The group delay of both transmit and receive filters exists between DRX and DTX. Clearing the PDL bit disables this mode, and the DTX data switches to the receive data from the line side. When the PDL bit is cleared, the FDT bit (Register 12, bit 6) becomes active to indicate that successful communication between the line side and system side is established. This provides verification that the communications link is operational.

The digital data loop-back mode offers a way to input data on the DRX pin and have the identical data output on the DTX pin through bypassing the transmit and receive filters. Setting the DDL bit (Register 10, bit 0) enables this mode, which provides an easy way to verify communication between the host processor/DSP and the DAA. No line-side power or off-hook sequence is required for this mode.

The remaining test modes require an off-hook sequence to operate. The following sequence lists the off-hook requirements:

1. Powerup or reset.
2. Allow the internal PLL to lock on PCLK and FSYNC.
3. Enable line-side by clearing PDL bit.
4. Issue an off-hook command.
5. Delay 402.75 ms for calibration to occur.
6. Set desired test mode.

The communications link digital loopback mode allows the host processor to provide a digital input test pattern on DRX and receive that digital test pattern back on DTX. To enable this mode, set the IDL bit (Register 1, bit 1). The communications link is tested in this mode. The digital stream is delivered across the isolation capacitors, C1 and C2, of the "2. Typical Application Schematic" on page 17, to the line-side device and returned across the same path. In this digital loopback mode, the 0.9 dB attenuation and filter group delays also exist.

The PCM analog loopback mode extends the signal path of the analog loopback mode. In this mode, an analog signal is driven from the line into the line-side device. This analog signal is converted to digital data and then passed across the communications link to the system-side device. The data passes through the receive filter, through the transmit filter, and is then passed across the communications link and sent back out onto the line as an analog signal. Set the PCML bit (Register 33, bit 7) to enable this mode.

With the final testing mode, internal analog loopback, the system can test the operation of the transmit and receive paths on the line-side device and the external components in the "2. Typical Application Schematic" on page 17. The host provides a digital test waveform on DRX. Data passes across the isolation barrier, is transmitted to and received from the line, passes back across the isolation barrier, and is presented to the host on DTX. Clear the HBE bit (Register 2, bit 1) to enable this mode.