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Si3210/Si3211

ProSLIC® Programmable CMOS SLIC/Codec with Ringing/Battery Voltage Generation

Features

- 100% programmable global solution
- Performs all BORSCHT functions
- DC-DC controller provides tracking battery from a 3.3–35V input (Si3210)
  - Minimizes power in all modes
  - Dynamic 0 to –94.5 V output
  - Choice of inductor (low cost) or transformer (high efficiency)
- Programmable line-feed parameters
  - 2-wire AC impedance and hybrid
  - Constant current feed (20 to 41 mA)
  - Loop closure and ring trip thresholds and filtering
- Internal balanced ringing up to $90V_{PK}$
  - 5 REN up to 4 kft; 3 REN up to 8 kft
  - Programmable frequency, amplitude, cadence, and wave shape
- Programmable audio processing
  - DTMF encoding and decoding
  - 12 kHz/16 kHz pulse metering
  - Phase-continuous FSK (caller ID)
  - Dual tone generators
- μ-Law/A-Law and linear PCM audio
- Extensive test and diagnostic features
  - Multiple loopback test modes
  - DC line V/I measurements
  - Supports GR-909 MLT
- Comprehensive design tools
  - Reference schematic and PCB layout
  - *ProSLIC API* abstracts SLIC functions, minimizing software development
- RoHS-compliant packages
- SPI and PCM bus digital interfaces

Applications

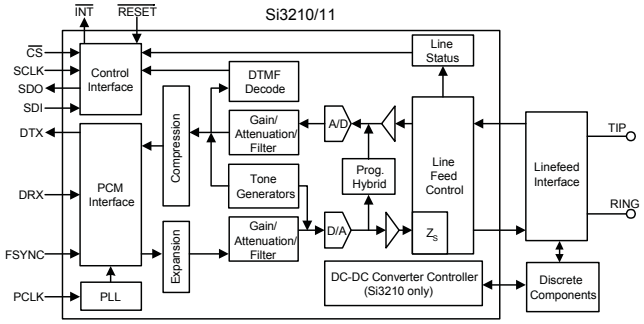
- Fixed Wireless (cellular) Terminals
- Terminal Adapters
- PBX/IP-PBX/Key telephone systems
- Voice-over-IP Systems:
  - DSL/EMTAs/FTTx
  - WiMax/LTE

Description

The Si3210/11 ProSLIC® chipset provides a complete analog telephone interface ideal for customer premise equipment (CPE). It integrates a subscriber line interface circuit (SLIC), voice codec, and battery generation (Si3210) or battery selection (Si3211) into a single CMOS integrated circuit. The battery supply continuously adapts its output voltage to minimize power dissipation and enables the entire circuit to be powered from a single 3.3 or 5 V supply (Si3210). The CMOS ProSLIC interfaces to the line through either the Si3201 Line-feed IC or a discrete line-feed circuit.

Si3210/11 features include software-configurable 5 REN internal ringing up to 90 VPK, DTMF generation and decoding, Caller ID generation, and a comprehensive set of telephony signaling capabilities for global operation with a single hardware solution. The Si3210/11 is packaged in a 38-pin QFN or TSSOP, and the Si3201 is packaged in a thermally-enhanced 16-pin SOIC.

Functional Block Diagram



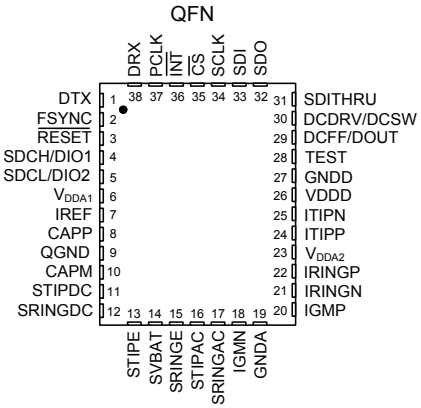
Ordering Information

See page 130.

QFN Pin Assignments

Si3210/11

QFN



U.S. Patent #6,567,521

U.S. Patent #6,812,744

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1. Electrical Specifications

Table 1. Absolute Maximum Ratings and Thermal Information[1]

Parameter	Symbol	Value	Unit
Si3210/11			
DC Supply Voltage	V_{DDD}, V_{DDA1}, V_{DDA2}	–0.5 to 6.0	V
Input Current, Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_{DDD} + 0.3)	V
Operating Temperature Range[2]	T_A	–40 to 100	C
Storage Temperature Range	T_{STG}	–40 to 150	C
TSSOP-38 Thermal Resistance, Typical	θ_{JA}	70	C/W
QFN-38 Thermal Resistance, Typical	θ_{JA}	35	C/W
Continuous Power Dissipation[2]	P_D	0.7	W
Si3201			
DC Supply Voltage	V_{DD}	–0.5 to 6.0	V
Battery Supply Voltage	V_{BAT}	–104	V
Input Voltage: TIP, RING, SRINGE, STIPE pins	V_{INHV}	(V_{BAT} – 0.3) to (V_{DD} + 0.3)	V
Input Voltage: ITIPP, ITIPN, IRINGP, IRINGN pins	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature Range[2]	T_A	–40 to 100	C
Storage Temperature Range	T_{STG}	–40 to 150	C
SOIC-16 Thermal Resistance, Typical[3]	θ_{JA}	55	C/W
Continuous Power Dissipation[2]	P_D	0.8 at 70 °C	W
		0.6 at 85 °C	

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Operation above 125 °C junction temperature may degrade device reliability.
3. Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
Ambient Temperature	T_A	G-grade	–40	25	85	°C
Si3210/11 Supply Voltage	V_{DDD},V_{DDA1}, V_{DDA2}		3.13	3.3/5.0	5.25	V
Si3201 Supply Voltage	V_{DD}		3.13	3.3/5.0	5.25	V
Si3201 Battery Voltage	V_{BAT}	$V_{BATH} = V_{BAT}$	–96	—	–10	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated. Product specifications are only guaranteed for the typical application circuit (including component tolerances).

Table 3. AC Characteristics

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level	THD = 1.5%	2.5	—	—	V_{PK}
Single Frequency Distortion[1]	2-wire – PCM or PCM – 2-wire: 200 Hz–3.4 kHz	—	—	–45	dB
Signal-to-(Noise + Distortion) Ratio[2]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any ZAC	Figure 1	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[2]	0 dBm0, Active off-hook, and OHT, any Zac	45	—	—	dB
Intermodulation Distortion		—	—	–45	dB
Gain Accuracy[2]	2-wire to PCM, 1014 Hz	–0.5	0	0.5	dB
	PCM to 2-wire, 1014 Hz	–0.5	0	0.5	dB
Gain Accuracy over Frequency		Figure 3,4	—	—	
Group Delay over Frequency		Figure 5,6	—	—	
Gain Tracking[3]	1014 Hz sine wave, reference level –10 dBm signal level:				
	3 to –37 dB	–0.25	—	0.25	dB
	–37 to –50 dB	–0.5	—	0.5	dB
	–50 to –60 dB	–1.0	—	1.0	dB
Round-Trip Group Delay	at 1000 Hz	—	1100	—	µs
Gain Step Accuracy	–6 to +6 dB	–0.017	—	0.017	dB
Gain Variation with Temperature	All gain settings	–0.25	—	0.25	dB
Gain Variation with Supply	$V_{DDA} = V_{DDA}$ = 3.3/5 V ±5%	–0.1	—	0.1	dB

Table 3. AC Characteristics (Continued)

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
2-Wire Return Loss	200 Hz to 3.4 kHz	30	35	—	dB
Transhybrid Balance	300 Hz to 3.4 kHz	30	—	—	dB
Noise Performance					
Idle Channel Noise[4]	C-Message Weighted	—	—	15	dBrnC
	Psophometric Weighted	—	—	–75	dBmP
	3 kHz flat	—	—	18	dBrn
PSRR from VDDA	RX and TX, DC to 3.4 kHz	40	—	—	dB
PSRR from VDDD	RX and TX, DC to 3.4 kHz	40	—	—	dB
PSRR from VBAT	RX and TX, DC to 3.4 kHz	40	—	—	dB
Longitudinal Performance					
Longitudinal to Metallic or PCM Balance	200 Hz to 3.4 kHz, $\beta_{Q1,Q2} \geq$ 150, 1% mismatch	56	60	—	dB
	$\beta_{Q1,Q2}$ = 60 to 240[5]	43	60	—	dB
	$\beta_{Q1,Q2}$ = 300 to 800[5]	53	60	—	dB
	Using Si3201	53	60	—	dB
Metallic to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING Register selectable ETBO/ETBA				
	00	—	33	—	Ω
	01	—	17	—	Ω
	10	—	17	—	Ω
Longitudinal Current per Pin	Active off-hook 200 Hz to 3.4 kHz Register selectable ETBO/ETBA				
	00	—	4	—	mA
	01	—	8	—	mA
	10	—	12	—	mA

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency will be smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} - V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
5. Assumes normal distribution of betas.

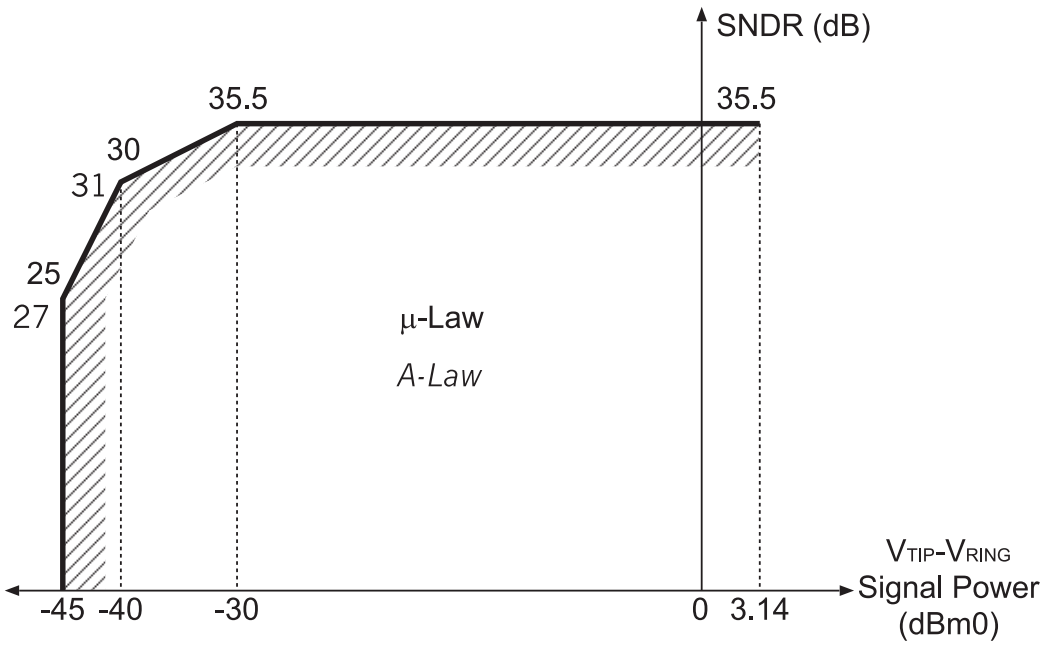


Figure 1. Transmit and Receive Path SNDR

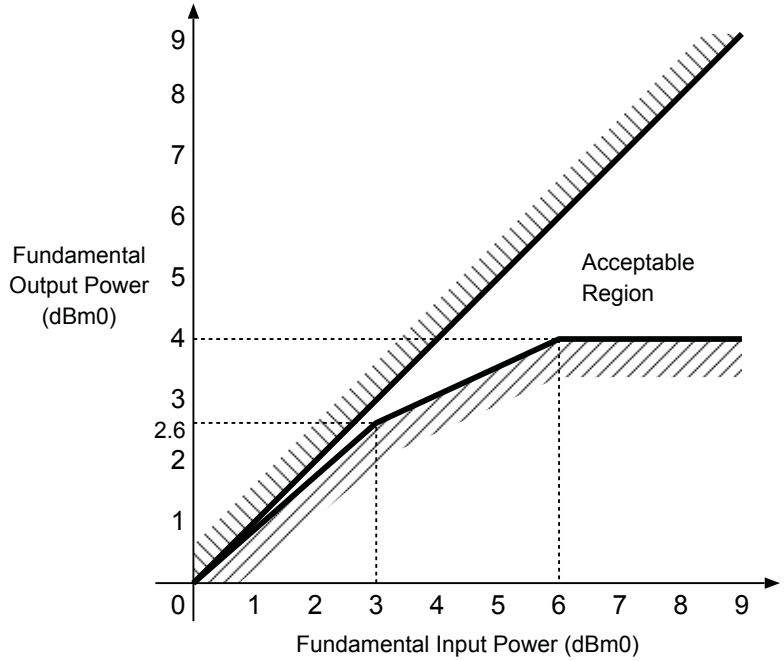


Figure 2. Overload Compression Performance

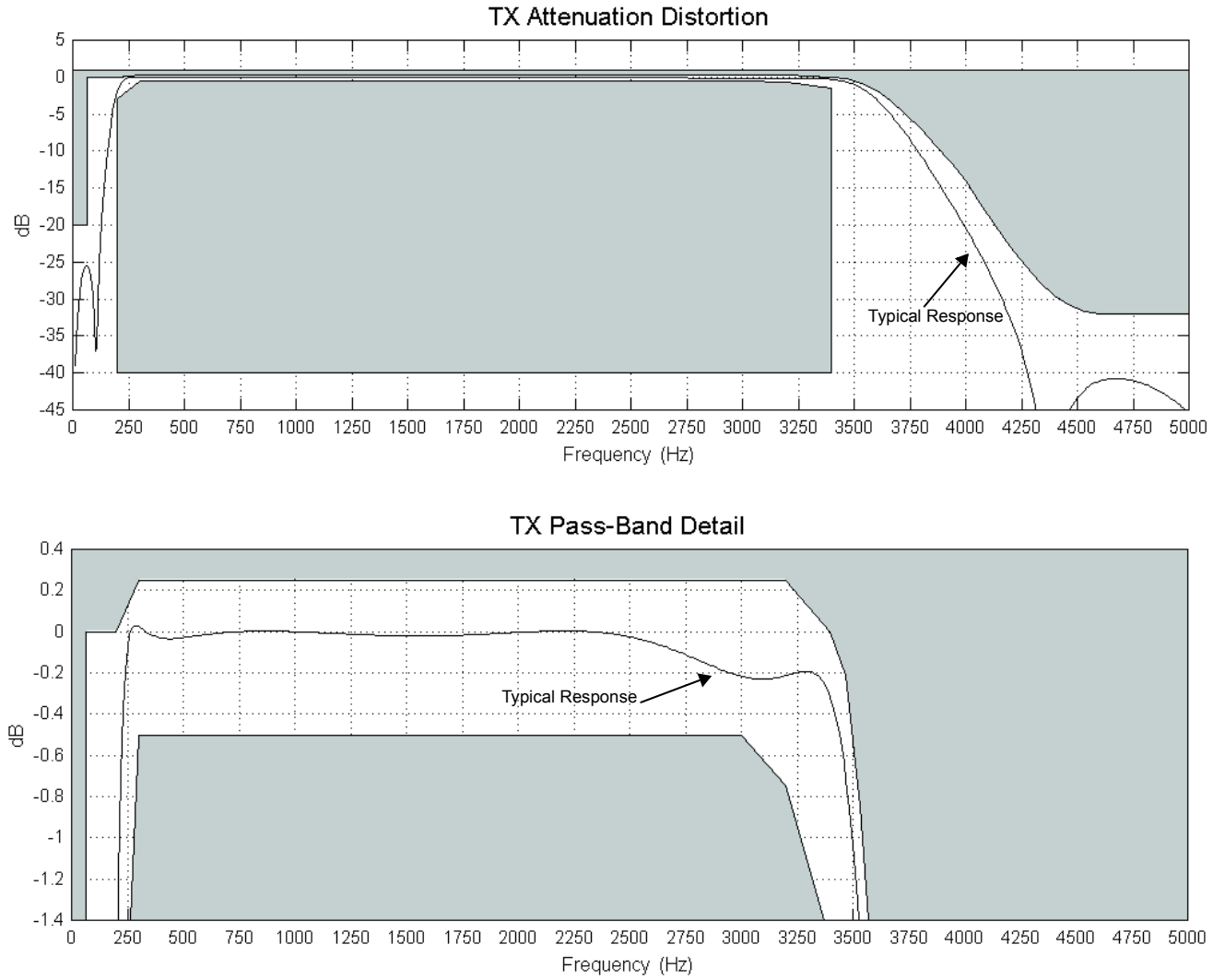


Figure 3. Transmit Path Frequency Response

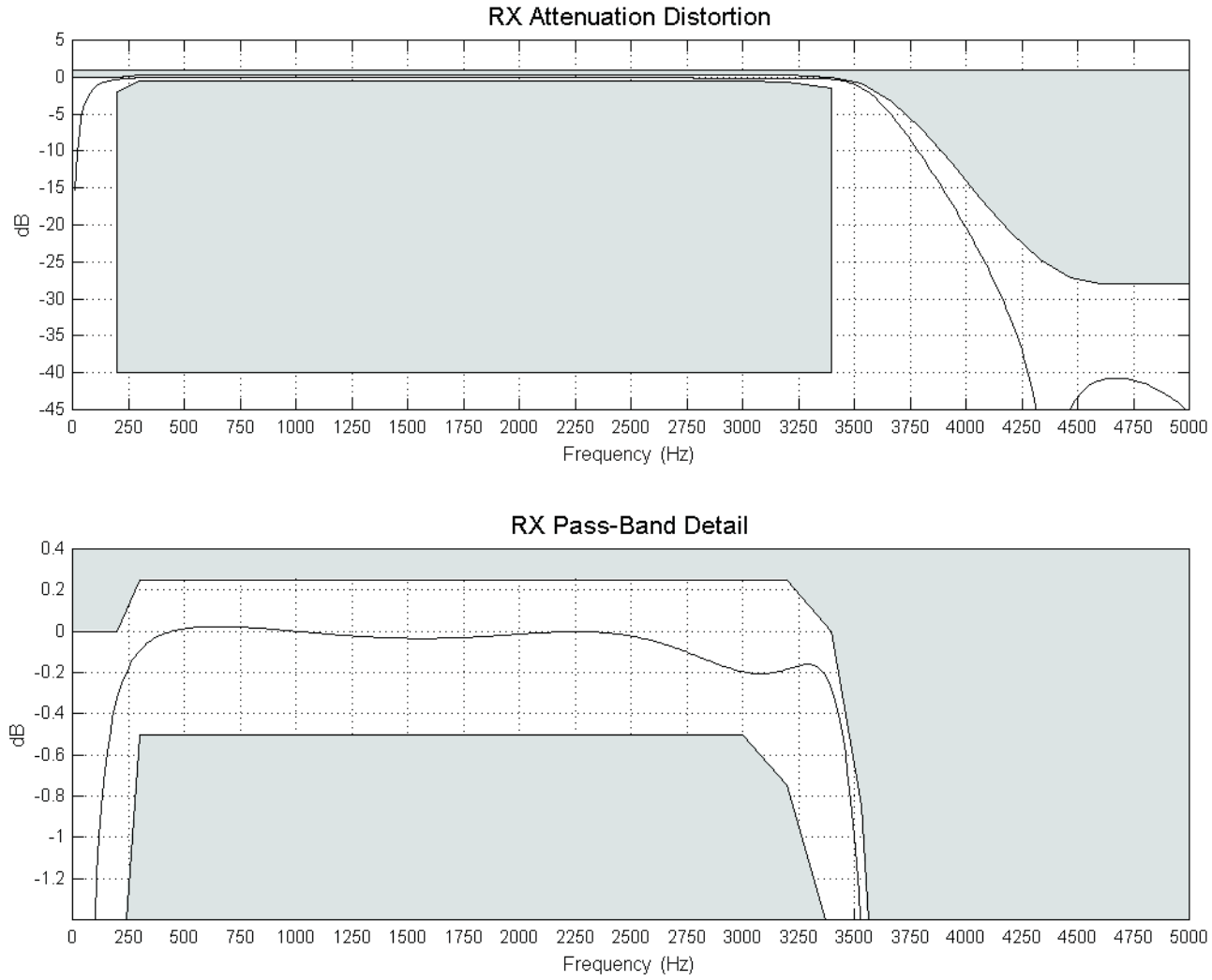


Figure 4. Receive Path Frequency Response

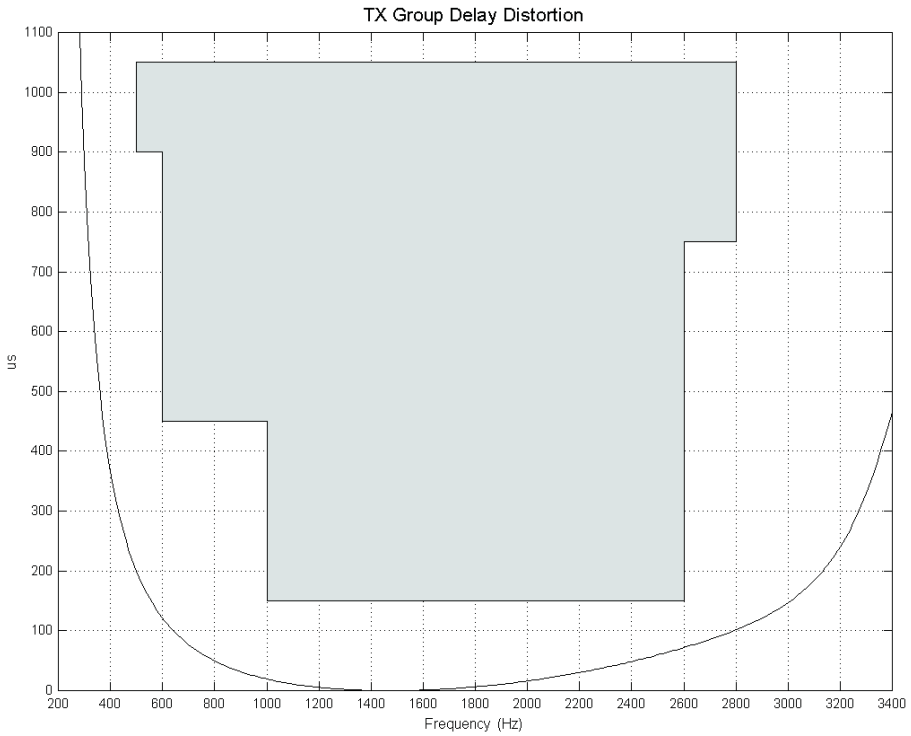


Figure 5. Transmit Group Delay Distortion

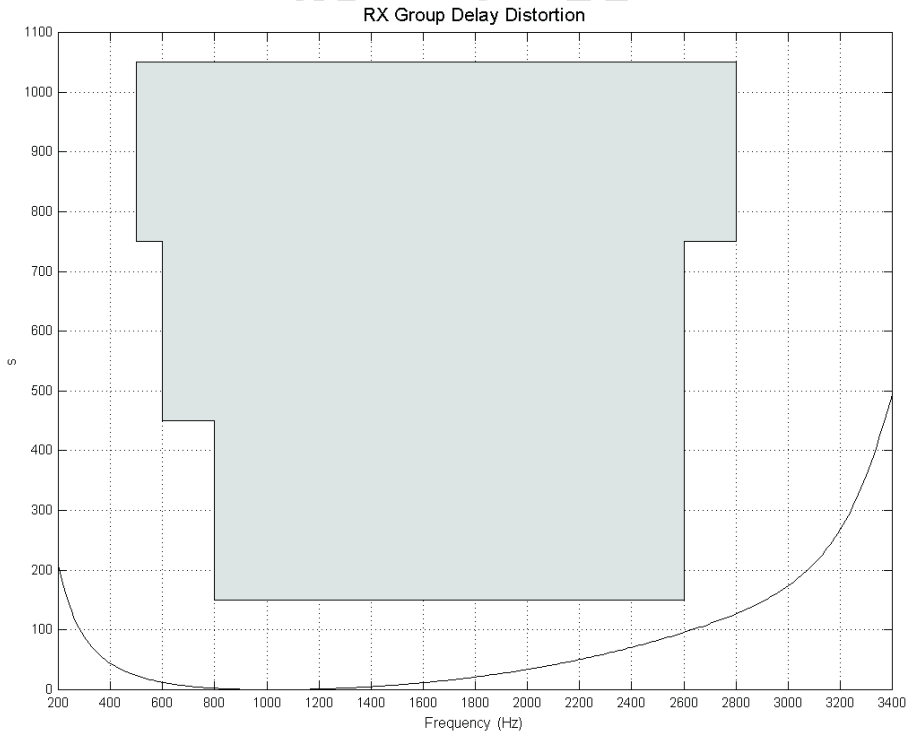


Figure 6. Receive Group Delay Distortion

Table 4. Linefeed Characteristics

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Resistance Range*	R_{LOOP}	See *Note.	0	—	160	Ω
DC Loop Current Accuracy		I_{LIM} = 29 mA, ETBA = 4 mA	–10	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} - V_{RING}$	–4	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	—	160	—	Ω
DC Open Circuit Voltage—Ground Start	V_{OCTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground V_{OC} = 48 V	–4	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	—	160	—	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	150	—	—	kΩ
Loop Closure/Ring Ground Detect Threshold Accuracy		I_{THR} = 11.43 mA	–20	—	20	%
Ring Trip Threshold Accuracy		I_{THR} = 40.64 mA	–10	—	10	%
Ring Trip Response Time		User Programmable Register 70 and Indirect Register 36	—	—	—	
Ring Amplitude	V_{TR}	5 REN load; sine wave; R_{LOOP} = 160 Ω, V_{BAT} = –75 V	44	—	—	V_{rms}
Ring DC Offset	R_{OS}	Programmable in Indirect Register 19	0	—	—	V
Trapezoidal Ring Crest Factor Accuracy		Crest factor = 1.3	–.05	—	.05	
Sinusoidal Ring Crest Factor	R_{CF}		1.35	—	1.45	
Ringing Frequency Accuracy		f = 20 Hz	–1	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF Times	–50	—	50	ms
Calibration Time		↑CAL to ↓CAL Bit	—	—	600	ms
Power Alarm Threshold Accuracy		At Power Threshold = 300 mW	–25	—	25	%

***Note:** DC resistance round trip; 160 Ω corresponds to 2 kft, 26 gauge AWG.

Table 5. Monitor ADC Characteristics

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (6-bit resolution)	DNLE		–1/2	—	1/2	LSB
Integral Nonlinearity (6-bit resolution)	INLE		–1	—	1	LSB
Gain Error (Voltage)			—	—	10	%
Gain Error (Current)			—	—	20	%

Table 6. Si321x DC Characteristics, $V_{DDA} = V_{DDD} = 5.0$ V

(V_{DDA},V_{DDD} = 4.75 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DDD}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DDD}	V
High Level Output Voltage	V_{OH}	DIO1,DIO2,SDITHRU: I_O = –4 mA SDO, DTX:I_O = –8 mA	V_{DDD} – 0.6	—	—	V
		DOUT: I_O = –40 mA	V_{DDD} – 0.8	—	—	V
Low Level Output Voltage	V_{OL}	DIO1,DIO2,DOUT,SDITHRU: I_O = 4 mA SDO,$\overline{INT}$,DTX:I_O = 8 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA

Table 7. Si321x DC Characteristics, $V_{DDA} = V_{DDD} = 3.3$ V

(V_{DDA},V_{DDD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DDD}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DDD}	V
High Level Output Voltage	V_{OH}	DIO1,DIO2,SDITHRU: I_O =–2 mA SDO, DTX:I_O = –4 mA	V_{DDD} – 0.6	—	—	V
		DOUT: I_O = –40 mA	V_{DDD} – 0.8	—	—	V
Low Level Output Voltage	V_{OL}	DIO1,DIO2,DOUT,SDITHRU: I_O = 2 mA SDO,$\overline{INT}$,DTX:I_O = 4 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA

Table 8. Power Supply Characteristics

(Unless otherwise noted, V_{DDA}, V_{DDD}=3.13 to 5.25 V; T_A=0 to 70°C for F-grade, –40 to 85°C for G-grade)

Parameter	Symbol	Test Condition	Typ[1]	Typ[2]	Max	Unit
Power Supply Current, Analog and Digital	$I_A + I_D$	Sleep ($\overline{RESET}$ = 0), V_{DDA}=V_{DDD}=3.13 to 3.465 V	0.1	—	0.3	mA
		Sleep ($\overline{RESET}$ = 0), V_{DDA}=V_{DDD}=4.75 to 5.25 V, T_A=0 to 70C/F-grade	—	0.1	0.3	mA
		Sleep ($\overline{RESET}$ = 0), V_{DDA}=V_{DDD}=4.75 to 5.25 V, T_A=–40 to 85C/G-grade	—	0.1	0.35	mA
		Open	33	42.8	49	mA
		Active on-hook ETBO = 4 mA, codec and Gm amplifier powered down	37	53	68	mA
		Active OHT ETBO = 4 mA	57	72	83	mA
		Active off-hook ETBA = 4 mA, I_{LIM} = 20 mA	73	88	99	mA
		Ground Start	36	47	55	mA
		Ringing sinewave, REN = 1, V_{PK} = 56 V	45	55	65	mA
V_{DD} Supply Current (Si3201)	I_{VDD}	Sleep mode, RESET = 0	100	100	—	µA
		Open (high impedance)	100	100	—	µA
		Active on-hook standby	110	110	—	µA
		Forward/reverse active off-hook, no I_{LOOP}, ETBO = 4 mA, V_{BAT} = –24 V	1	1	—	mA
		Forward/reverse OHT, ETBO = 4 mA, V_{BAT} = –70 V	1	1	—	mA
V_{BAT} Supply Current[3]	I_{BAT}	Sleep ($\overline{RESET}$ = 0)	0	0	—	mA
		Open (DCOF = 1)	0	0	—	mA
		Active on-hook V_{OC} = 48 V, ETBO = 4 mA	3	3	—	mA
		Active OHT ETBO = 4 mA	11	11	—	mA
		Active off-hook ETBA = 4 mA, I_{LIM} = 20 mA	30	30	—	mA
		Ground Start	2	2	—	mA
		Ringing: V_{PK_RING} = 56 V_{PK}, Sinewave ringing: REN = 1	5.5	5.5	—	mA
V_{BAT} Supply Slew Rate		When using Si3201	—	—	10	V/µs

Table 8. Power Supply Characteristics (Continued)

(Unless otherwise noted, V_{DDA}, V_{DDD}=3.13 to 5.25 V; T_A=0 to 70°C for F-grade, –40 to 85°C for G-grade)

Parameter	Symbol	Test Condition	Typ[1]	Typ[2]	Max	Unit

Notes:
1. V_{DDD}, V_{DDA} = 3.3 V.
2. V_{DDD}, V_{DDA} = 5.25 V.
3. I_{BAT} = current from V_{BAT} (the large negative supply). For a switched-mode power supply regulator efficiency of 71%, the user can calculate the regulator current consumption as $I_{BAT} \times V_{BAT}/(0.71 \times V_{DC})$.

Table 9. Switching Characteristics (General Inputs)[1]

V_{DDA} = V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{\text{RESET}}$	t_r	—	—	20	ns
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}	100	—	—	ns

Notes:
1. All timing (except rise and fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D – 0.4$ V, V_{IL} = 0.4 V. Rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. Additional initialization guidelines apply; see section 1.2 ProSLIC Initialization in AN35.

Table 10. Switching Characteristics (SPI)

V_{DDA} = V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		0.062	—	—	µs
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{\text{CS}}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{\text{CS}}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, $\overline{\text{CS}}$ to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects (Continuous SCLK)	t_{cs}		440	—	—	ns
Delay Time between Chip Selects (Non-continuous SCLK)	t_{cs}		220	—	—	ns

Table 10. Switching Characteristics (SPI)

V_{DDA} = V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF

SDI to SDITHRU Propagation Delay	t_{d4}		—	4	10	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DDD} –0.4 V, V_{IL} = 0.4 V						

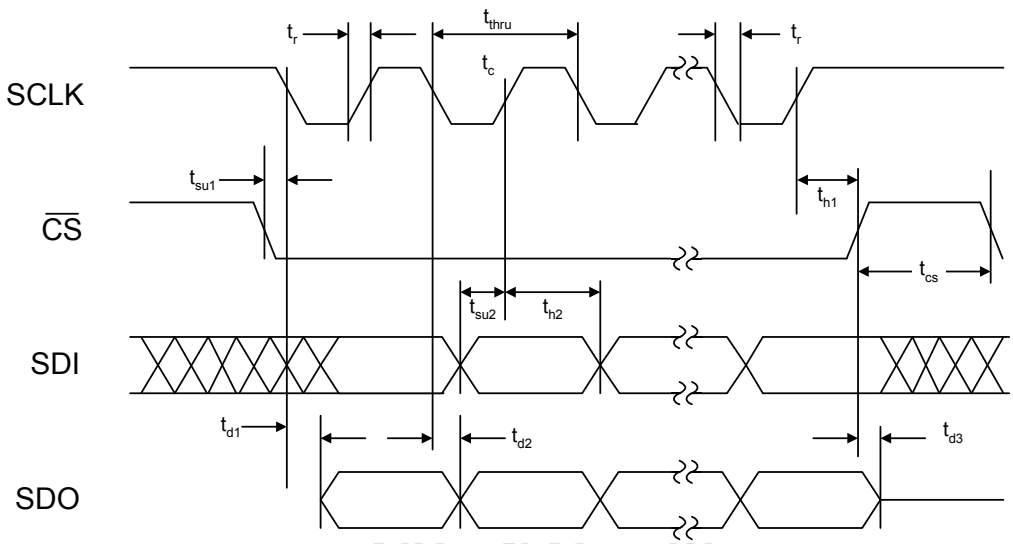


Figure 7. SPI Timing Diagram

Table 11. Switching Characteristics—PCM Highway Serial Interface

V_D = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF

Parameter	Symbol	Test Conditions	Min [1]	Typ [1]	Max [1]	Units
PCLK Frequency	$1/t_c$		— — — — — — — —	0.256 0.512 0.768[2] 1.024 1.536[2] 2.048 4.096 8.192	— — — — — — — —	MHz MHz MHz MHz MHz MHz MHz MHz
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
PCLK-to-FSYNC Jitter Tolerance	t_{jitter}		–120	—	120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-state[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns

Table 11. Switching Characteristics—PCM Highway Serial Interface

V_D = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF

Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} _ $V_{I/O}$ _0.4V, V_{IL} = 0.4 V.
2. Not a valid PCLK frequency for GCI mode.
3. Specification applies to PCLK fall to DTX tri-state when that mode is selected (TRI = 0).

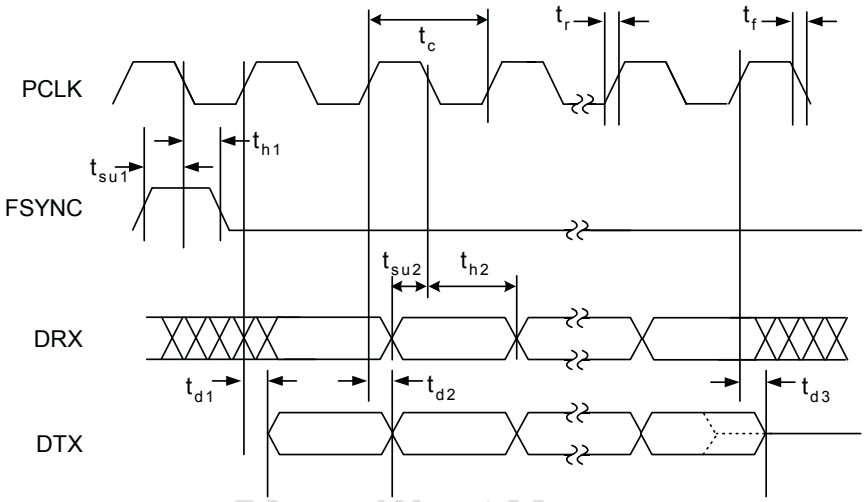
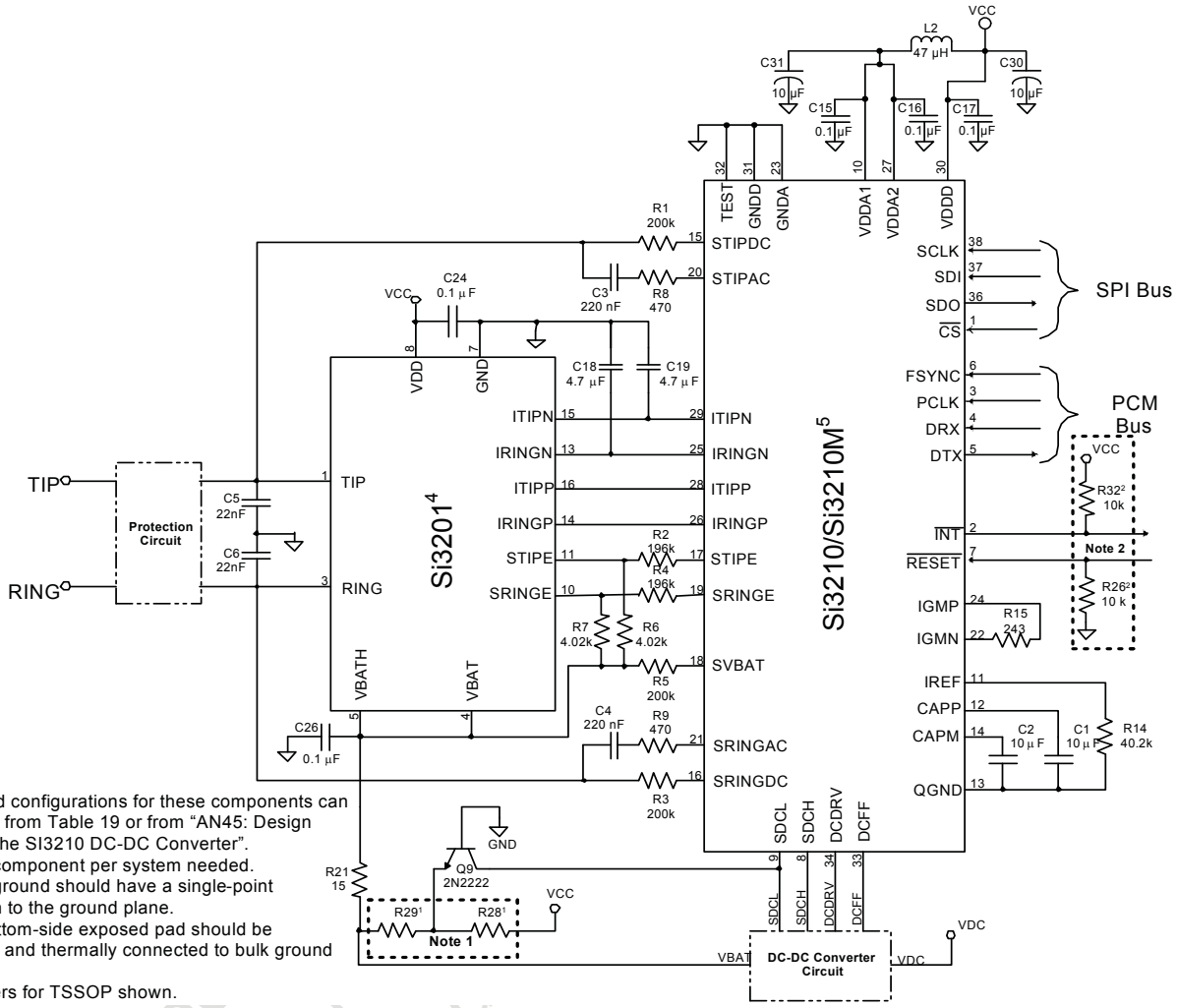


Figure 8. PCM Highway Interface Timing Diagram



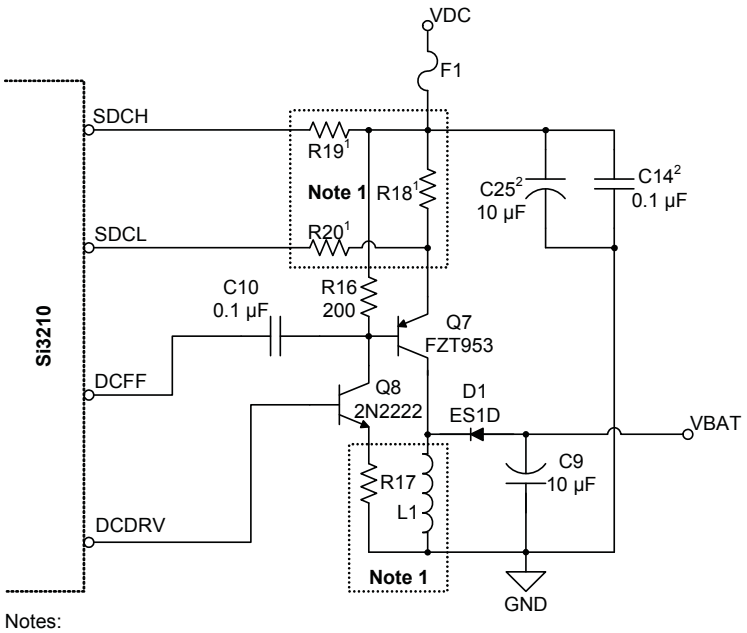
Notes:
1. Values and configurations for these components can be derived from Table 19 or from “AN45: Design Guide for the SI3210 DC-DC Converter”.
2. Only one component per system needed.
3. All circuit ground should have a single-point connection to the ground plane.
4. Si3201 bottom-side exposed pad should be electrically and thermally connected to bulk ground plane.
5. Pin numbers for TSSOP shown.

Figure 9. Si3210/Si3210M Application Circuit Using Si3201

Table 12. Si3210/Si3210M + Si3201 External Component Values

Component(s)	Value	Package	Supplier
C1,C2	10 µF, 6 V Ceramic or 16 V Low Leakage Electrolytic, ±20%	Radial	Murata, Nichicon URL1C100MD
C3,C4	220 nF, 100 V, X7R, ±20%	1812	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, ±20%	1206	Murata, Johanson, Novacap, Venkel
C15,C16,C17,C24	0.1 µF, 6 V, Y5V, ±20%	603	Murata, Johanson, Novacap, Venkel
C18,C19	4.7 µF, ceramic, 6 V, X7R, ±20%	1206	Murata, Johanson, Novacap, Venkel
C26	0.1 µF, 100 V, X7R, ±20%	1210	Murata, Johanson, Novacap, Venkel
C30,C31	10 µF, 10 V, Electrolytic, ±20%	Radial	Panasonic
L2	47 µH, 150 mA	SMD	Coilcraft
R1[1],R3[1],R5[1]	200 kΩ, 1/10 W, ±1%	805	
R2[1],R4[1]	196 kΩ, 1/10 W, ±1%	805	
R6,R7	4.02 kΩ, 1/10 W, ±1%	805	
R8,R9	470 Ω, 1/10 W, ±1%	805	
R14	40.2 kΩ, 1/10 W, ±1%	805	
R15	243 Ω, 1/10 W, ±1%	805	
R21	15 Ω, 1/4 W, ±5%	805	
R26[2]	10 kΩ, 1/10 W, ±1%	805	
R28,R29	1/10 W, 1% (See “AN45: Design Guide for the Si3210 DC-DC Converter” or Table 19 for value selection)	805	
R32[2]	10 kΩ, 1/10 W, ±5%	805	
Q9	60 V, General Purpose Switching NPN	SOT-23	ON Semi MMBT2222ALT1; Central Semi CMPT2222A; Zetex FMMT2222

Notes:
1. These resistors must be in an 0805 or larger package.
2. Only one component per system needed.



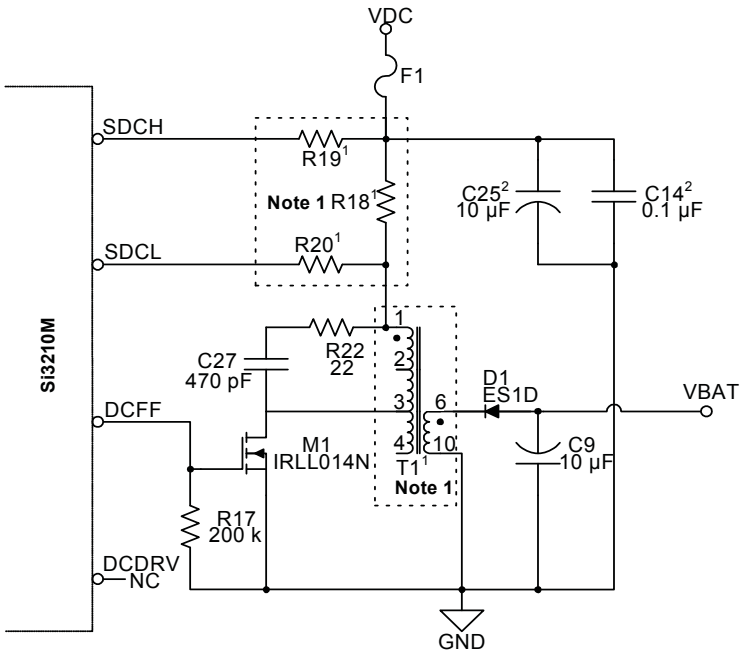
Notes:
1. Values and configurations for these components can be derived from "AN45: Design Guide for the Si3210 DC-DC Converter" or Table 21.
2. Voltage rating for C14 and C25 must be greater than VDC.

Figure 10. Si3210 BJT/Inductor DC-DC Converter Circuit

Table 13. Si3210 BJT/Inductor DC-DC Converter Component Values

Component(s)	Value	Package	Supplier
C9	10 µF, 100 V, Electrolytic, ±20%	Radial	Panasonic
C10	0.1 µF, 50 V, X7R, ±20%	1210	Murata, Johanson, Novacap, Venkel
C14*	0.1 µF, X7R, ±20%	1210	Murata, Johanson, Novacap, Venkel
C25*	10 µF, Electrolytic, ±20%	Radial	Panasonic
R16	200 Ω, 1/10 W, ±5%	805	
R17	1/10 W, ±5% (See AN45 or Table 21 for value selection)	805	
R18	1/4 W, ±5% (See AN45 or Table 21 for value selection)	1206	
R19,R20	1/10 W, ±1% (See AN45 or Table 21 for value selection)	805	
F1	Fuse	SMD	Belfuse SSQ Series
D1	Ultra Fast Recovery 200 V, 1A Rectifier	DO214-AA	General Semi ES1D; Central Semi CMR1U-02
L1	1 A, Shielded Inductor (See AN45 or Table 21 for value selection)	SMD	API Delevan SPD127 series, Sumida CDRH127 series, Datatronics DR340-1 series, Coilcraft DS5022, TDK SLF12565
Q7	120 V, High Current Switching PNP	SOT-223	Zetex FZT953, FZT955, ZTX953, ZTX955; Sanyo 2SA1552
Q8	60 V, General Purpose Switching NPN	SOT-23	ON Semi MMBT2222ALT1, MPS2222A; Central Semi CMPT2222A; Zetex FMMT2222

***Note:** Voltage rating of this device must be greater than V_{DC}.

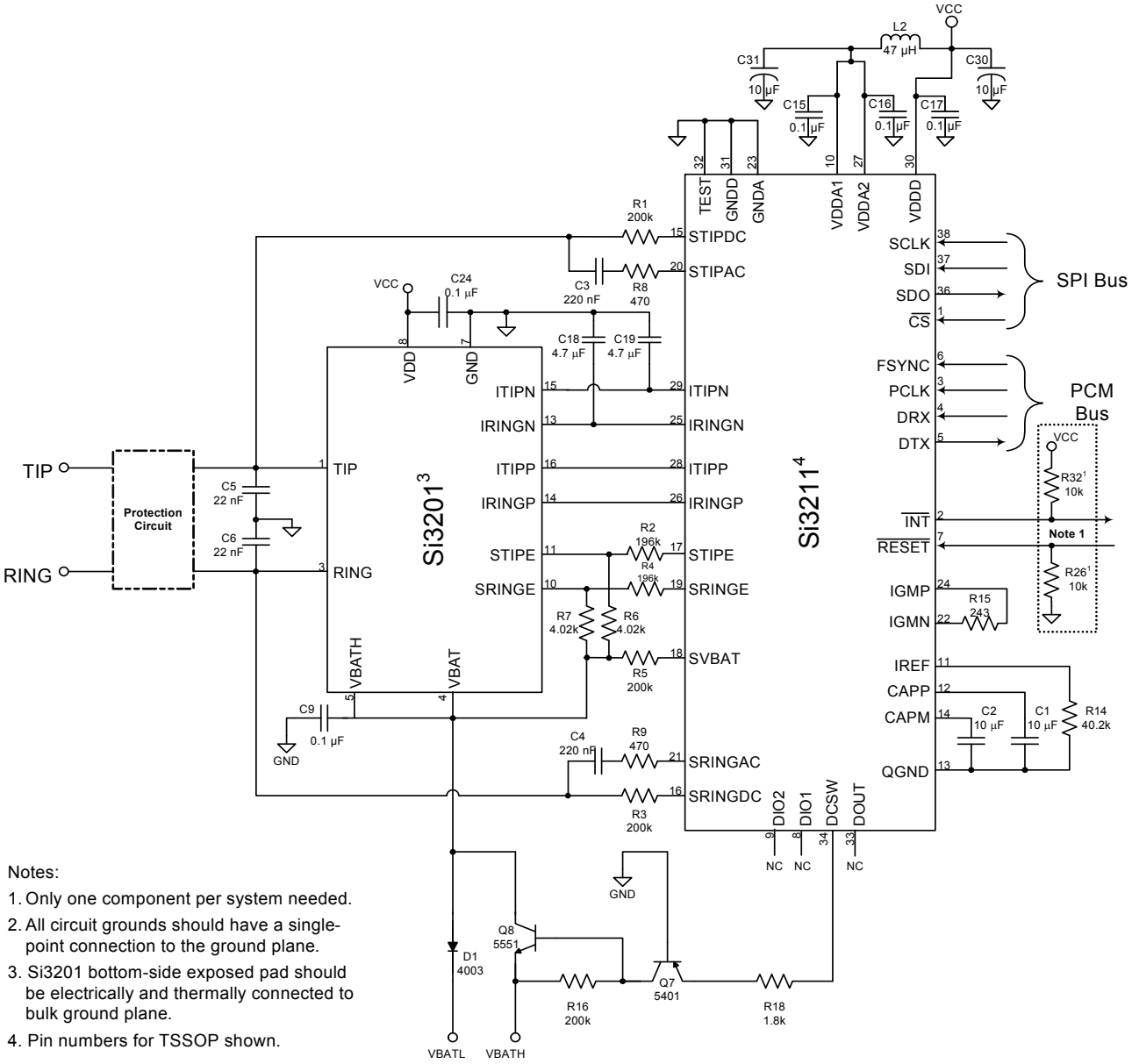


Notes:
1. Values and configurations for these components can be derived from AN45 or Table 20.
2. Voltage rating for C14 and C25 must be greater than VDC.

Figure 11. Si3210M MOSFET/Transformer DC-DC Converter Circuit

Table 14. Si3210M MOSFET/Transformer DC-DC Converter Component Values

Component(s)	Value	Package	Supplier
C9	10 µF, 100 V, Electrolytic, ±20%	Radial	Panasonic
C14*	0.1 µF, X7R, ±20%	1210	Murata, Johanson, Novacap, Venkel
C25*	10 µF, Electrolytic, ±20%	Radial	Panasonic
C27	470 pF, 100 V, X7R, ±20%	1206	Murata, Johanson, Novacap, Venkel
R17	200 kΩ, 1/10 W, ±5%	805	
R18	1/4 W, ±5% (See "AN45: Design Guide for the Si3210 DC-DC Converter" or Table 20 for value selection)	1206	
R19,R20	1/10 W, ±1% (See AN45 or Table 20 for value selection)	805	
R22	22 Ω, 1/10 W, ±5%	805	
F1	Fuse	SMD	Belfuse SSQ Series
D1	Ultra Fast Recovery 200 V, 1 A Rectifier	D214-AA	General Semi ES1D; Central Semi CMR1U-02
T1	Power Transformer	SMD	Coiltronic CTX01-15275; Datatronics SM76315; Midcom 31353R-02
M1	100 V, Logic Level Input MOSFET	SOT-223	Intl Rect. IRLL014N; Intersil HUF76609D3S; ST Micro STD5NE10L, STN2NE10L
***Note:** Voltage rating of this device must be greater than V_{DC}.			



Notes:

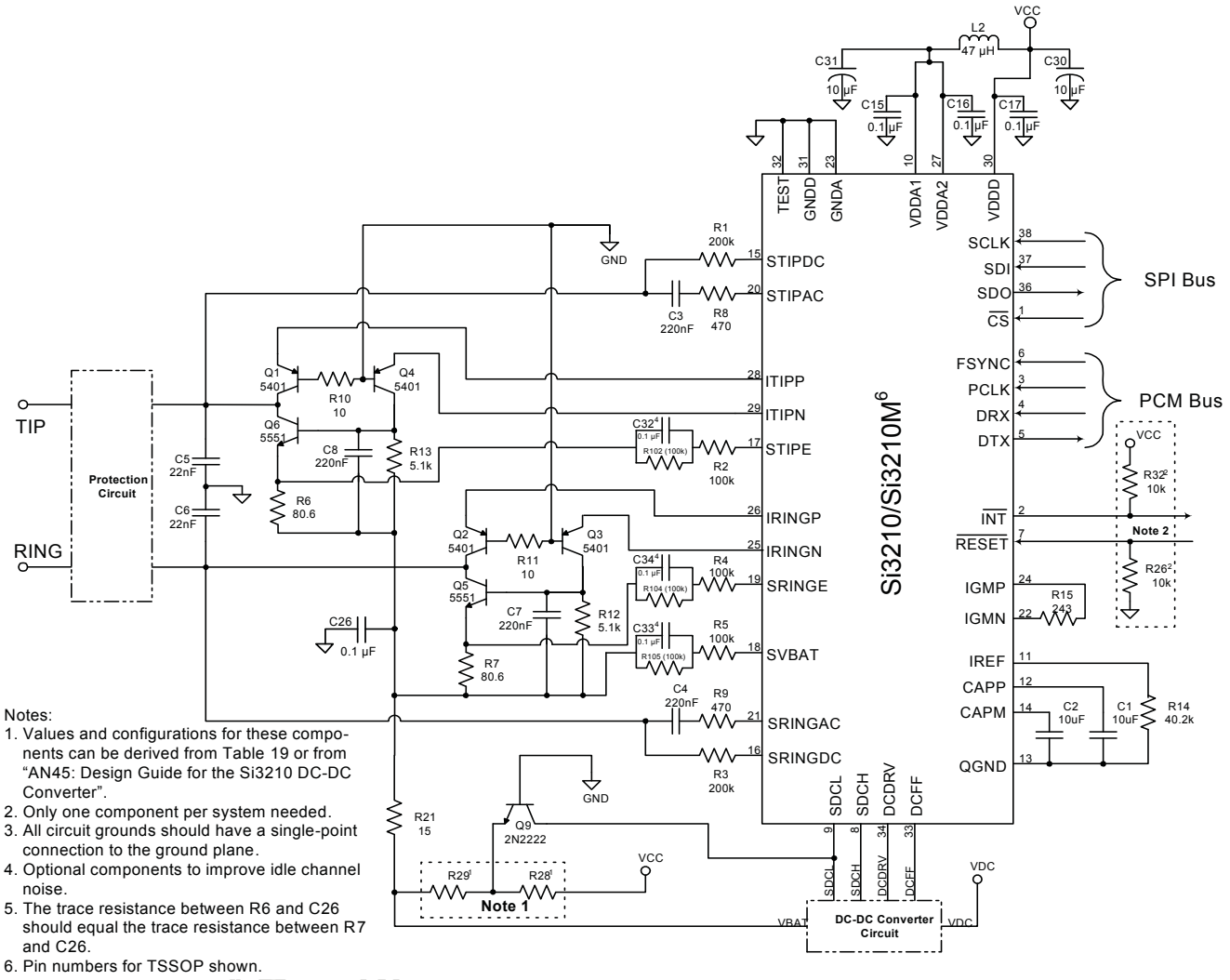
1. Only one component per system needed.
2. All circuit grounds should have a single-point connection to the ground plane.
3. Si3201 bottom-side exposed pad should be electrically and thermally connected to bulk ground plane.
4. Pin numbers for TSSOP shown.

Figure 12. Si3211 Typical Application Circuit Using Si3201

Table 15. Si3211 + Si3201 External Component Values

Component(s)	Value	Package	Supplier
C1,C2	10 µF, 6 V Ceramic or 16 V, Low-Leakage Electrolytic, ±20%	Radial	Murata, Nichicon URL1C100MD
C3,C4	220 nF, 100 V, X7R, ±20%	1812	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, ±20%	1206	Murata, Johanson, Novacap, Venkel
C9	0.1 µF, 100 V, X7R, ±20%	1210	Murata, Johanson, Novacap, Venkel
C15,C16,C17,C24	0.1 µF, 6 V, Y5V, ±20%	1206	Murata, Johanson, Novacap, Venkel
C18,C19	4.7 µF Ceramic, 6 V, X7R, ±20%	1206	Murata, Johanson, Novacap, Venkel
C30,C31	10 µF, 10 V, Electrolytic, ±20%	Radial	Panasonic
L2	47 µH, 150 mA	SMD	Coilcraft
D1	200 V, 1 A Rectifier	MELF	ON Semi: MRA4003, IN4003
Q7	120 V, PNP, BJT	SOT-89	ON Semi: 2N5401
Q8	120 V, NPN, BJT	SOT-223	ON Semi: 2N5551
R1[1],R3[1],R5[1],R16[1]	200 kΩ, 1/10 W, ±1%	805	
R2[1],R4[1]	196 kΩ, 1/10 W, ±1%	805	
R6,R7	4.02 kΩ, 1/10 W, ±1%	805	
R8,R9	470 Ω, 1/10 W, ±1%	805	
R14	40.2 kΩ, 1/10 W, ±1%	805	
R15	243 Ω, 1/10 W, ±1%	805	
R18	1.8 kΩ, 1/10 W, ±5%	805	
R26[2]	10 kΩ, 1/10 W, ±1%	805	
R32[2]	10 kΩ, 1/10 W, ±5%	805	

Notes:
1. These resistors must be in an 0805 or larger package.
2. Only one component per system needed.



Notes:
1. Values and configurations for these components can be derived from Table 19 or from "AN45: Design Guide for the Si3210 DC-DC Converter".
2. Only one component per system needed.
3. All circuit grounds should have a single-point connection to the ground plane.
4. Optional components to improve idle channel noise.
5. The trace resistance between R6 and C26 should equal the trace resistance between R7 and C26.
6. Pin numbers for TSSOP shown.

Figure 13. Si3210/Si3210M Typical Application Circuit Using Discrete Components

Table 16. Si3210/Si3210M External Component Values—Discrete Solution

Component(s)	Value	Package	Supplier/Part Number
C1,C2	10 µF, 6 V Ceramic or 16 V Low-Leakage Electrolytic, ±20%	Radial	Murata, Panasonic, Nichicon URL1C100MD
C3,C4	220 nF, 100 V, X7R, ±20%	1812	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, ±20%	1206	Murata, Johanson, Novacap, Venkel
C7,C8	220 nF, 50 V, X7R, ±20%	1812	Murata, Johanson, Novacap, Venkel
C15,C16,C17	0.1 µF, 6 V, Y5V, ±20%	603	Murata, Johanson, Novacap, Venkel
C26	0.1 µF, 100 V, X7R, ±20%	1210	Murata, Johanson, Novacap, Venkel
C30,C31	10 µF, 10 V, Electrolytic, ±20%	Radial	Panasonic
C32,C33,C34	0.1 µF, 50 V, ±20%	805	Venkel
L2	47 µH, 150 mA	SMD	Coilcraft
Q1,Q2,Q3,Q4	120 V, PNP, BJT	SOT-23	Central Semi CMPT5401; ON Semi MMBT5401LT1, 2N5401; Zetex FMMT5401; Fairchild 2N5401; Samsung 2N5401
Q5,Q6	120 V, NPN, BJT	SOT-223	Central Semi CZT5551, ON Semi 2N5551; Fairchild 2N5551; Phillips 2N5551
Q9	NPN General Purpose BJT	SOT-23	ON Semi MMBT2222ALT1, MPS2222A; Central Semi CMPT2222A; Zetex FMMT2222
R1[1], R3[1]	200 kΩ, 1/10 W, ±1%	805	
R2[1], R4[1], R5[1], R102[1], R104[1], R105[1]	100 kΩ, 1/10 W, ±1%	805	
R6,R7	80.6 Ω, 1/4 W, ±1%	1210	
R8,R9	470 Ω, 1/10 W, ±1%	805	
R10,R11	10 Ω, 1/10 W, ±5%	805	
R12,R13	5.1 kΩ, 1/10 W, ±5%	805	
R14	40.2 kΩ, 1/10 W, ±1%	805	
R15	243 Ω, 1/10 W, ±1%	805	
R21	15 Ω, 1/4 W, ±1%	805	
R26[2]	10 kΩ, 1/10 W, ±1%	805	
R28,R29	1/10 W, ±1% (See “AN45: Design Guide for the Si3210/15/16 DC-DC Converter” or Table 19 for value selection)	805	
R32[2]	10 kΩ, 1/10 W, ±5%	805	

Notes:
1. These resistors must be in 0805 or larger package.
2. Only one component per system needed.