Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

OCTAL IEEE 802.3AT POE PSE CONTROLLER

Features

- Octal-Port Power Sourcing Equipment (PSE) controller
- IEEE 802.3at Type I and II compliant
- Port priority shutdown control
- Adds enhanced features for maximum design flexibility:
  - Per-port current and voltage monitoring
  - PoE+ support with programmable current limits
  - Multi-point detection
  - Programmable power MOSFET gate drive control
  - Configurable watchdog timer enables failsafe operation
- Maskable interrupt pin
- Comprehensive fault protection circuitry includes:
  - Power undervoltage lockout
  - Output current limit and short-circuit protection
  - Thermal overload detection
- Pin-programmable AUTO modes
- Extended operating temp range: –40 to +85 °C
- 56-pin QFN package (RoHS-compliant)
- On-chip dc-dc converter enables single-rail power operation

Ordering Information:
See page 49.

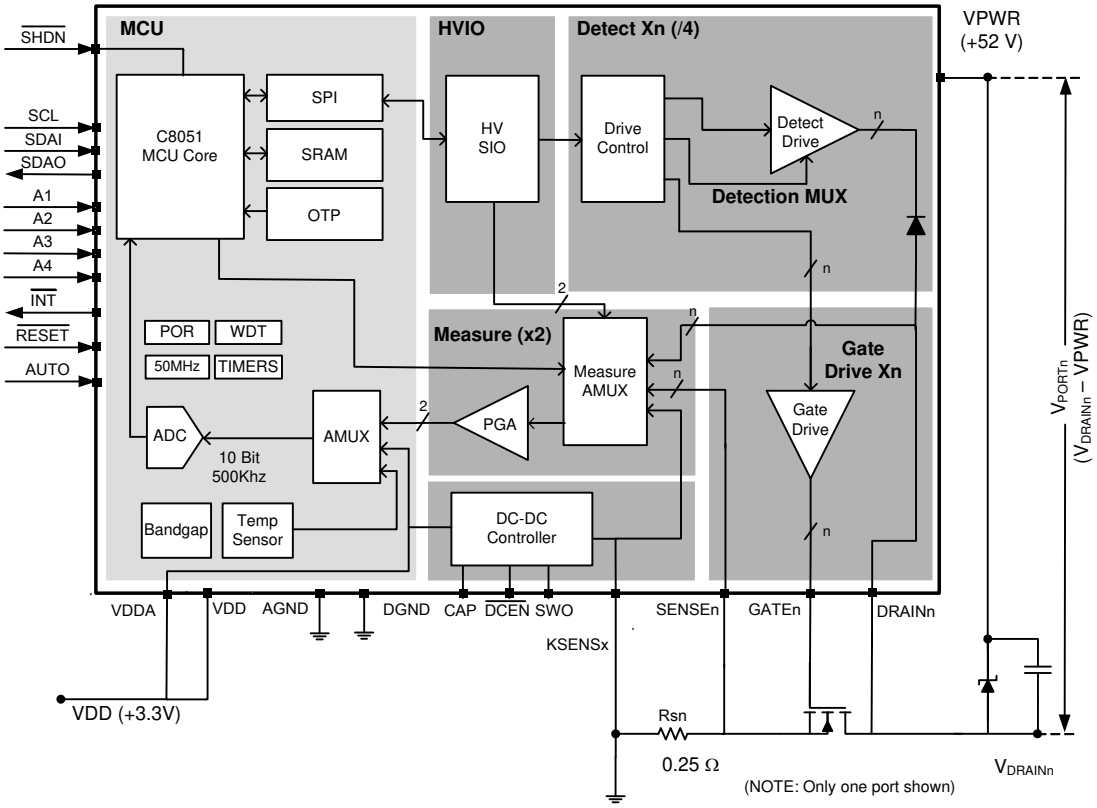
Applications

- IEEE Power Sourcing Equipment (PSE)
- Power over Ethernet Switches
- IP Phone Systems
- Smartgrid Switches
- Ruggedized and Industrial Switches

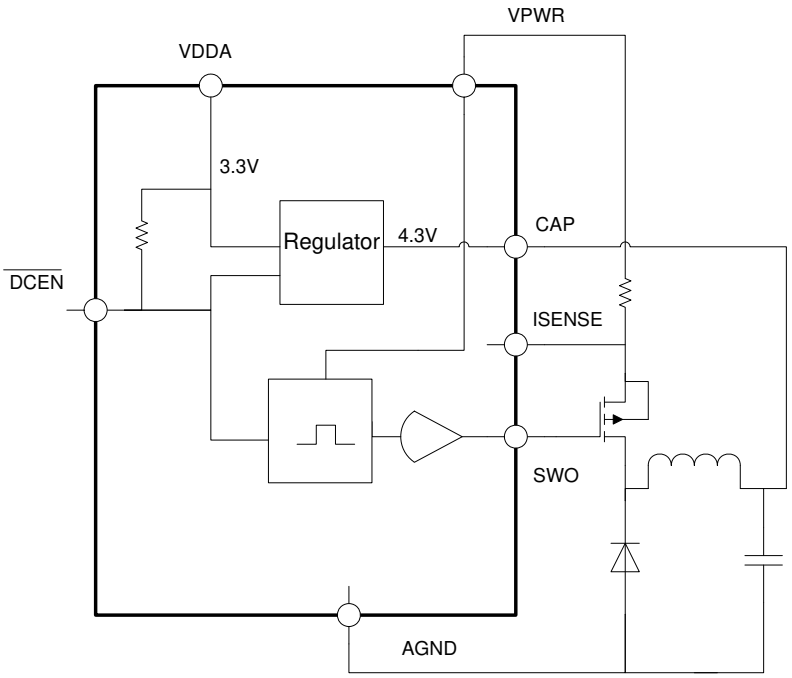
Description

The Si3459 is a fully-programmable, eight-port power management controller for IEEE 802.3 compliant Power Sourcing Equipment (PSE). Designed for use in PSE endpoint (switches), the Si3459 integrates eight independent ports, each with IEEE-required powered device (PD) detection and classification functionality. In addition, the Si3459 features a fully-programmable architecture that enables powered device (PD) disconnect using a dc sense algorithm, a robust multipoint detection algorithm, software-configurable per-port current and voltage monitoring, and programmable current limits to support the IEEE 802.3at standard. Intelligent protection circuitry includes input undervoltage detection, output current limit, and short-circuit protection. The Si3459 operates by host processor control through a three-wire, I^2C-compatible serial interface. Independent serial data input and output pins enable high-voltage isolation through external isolators. An interrupt pin is used to alert the host processor of various status and fault conditions. The device also supports pin-programmable AUTO modes for autonomous operation, without the need for a host processor. The Si3459 also features an on-chip dc-dc converter for creating the digital voltage rail from the PoE voltage, thus enabling single-rail power operation.

Functional Block Diagrams



DC-DC Converter Block Diagram



The case shown has both the DC-DC converter and series regulator enabled.
To enable ONLY the series regulator, tie SWO to VPWR. External components are unnecessary.

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. PSE Port Interface Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Voltages						
VPWR Input Supply Voltage	V_{PWR}	When generating IEEE-compliant output voltage	44	48	57	V
VPWR UVLO Input Voltage (to turn on)[2]	V_{UVLO_ON}		—	32	—	V
VPWR UVLO Input Voltage (to turn off)[2]	V_{UVLO_OFF}		—	44	—	V
VDD Supply Voltage	V_{DD}		3.0	3.3	3.6	V
VDD UVLO Voltage[2]	V_{DD_UVLO}	VDD – AGND	—	2.8	—	V
Hardware Reset Voltage	V_{RESET}	VDD voltage causing an MCU reset	—	1.8	—	V

Notes:

1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 1. PSE Port Interface Recommended Operating Conditions[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Currents[3]						
VPWR Supply Current	I_{VPWR}	During normal operation	—	2	5	mA
VDD Supply Current	I_{DD}		—	18	25	mA
Detection Specification						
Detection Voltage when R_{DET} = 25.5kΩ	V_{PORTn}	Primary detection voltage	—	–4.0	–2.8	V
		Secondary detection voltage	–10	–8.0	—	V
Detection Current Limit	I_{DET}	Measured when V_{PORTn} = 0 V	—	3	4.9	mA
Minimum Signature Resistance @ PD	R_{DET_MIN}		15	—	19	kΩ
Maximum Signature Resistance @ PD	R_{DET_MAX}		26.5	—	33	kΩ
Shorted Port Threshold	R_{SHORT}		150	—	400	Ω
Open Port Threshold	R_{OPEN}		100	—	400	kΩ
Classification Specifications						
Classification Voltage	V_{CLASS}	0 mA < ICLASS < 45 mA	–20.5	—	–15.5	V
Classification Current	I_{CLASS}	Measured when V_{PORTn} = 0 V	55	—	95	mA
Classification Current Region	I_{CLASS_REGION}	Class 0	0	—	5	mA
		Class 1	8	—	13	mA
		Class 2	16	—	21	mA
		Class 3	25	—	31	mA
		Class 4	35	—	45	mA

Notes:
1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 1. PSE Port Interface Recommended Operating Conditions[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Classification Mark Specifications						
Mark Voltage	V_{MARK}	I_{PORT} = 0 mA	–10	—	—	V
		I_{PORT} = 5 mA	—	—	–7	V
Output Voltage Sense						
Threshold Voltage for Power Good Sense	V_{PGOOD}	Measured at V_{DRAINn} to AGND	1	—	3	V
Bias Current of DRAINn Pin	I_{DRAINn}	V_{DRAINn} = 0 V	—	–25	—	µA
Current Sense						
Sense resistor value	R_{SENSE}	1% tolerance	0.2475	0.25	0.2525	Ω
Sense Voltage at Current Limit	V_{ILIM}	V_{SENSEn}–$V_{KSENSEn}$ 1x Power Mode	100	106.25	112.5	mV
		V_{SENSEn}–$V_{KSENSEn}$ 2x Power Mode	200	212.5	225	mV
DC Disconnect Sense Voltage	V_{DC_MIN}	V_{SENSEn} – $V_{KSENSEn}$	1.25	1.875	2.5	mV
SENSEn Pin Bias Current	I_{SENSE}	V_{SENSEn} – AGND	—	–1	—	µA
MOSFET Gate Drive						
Drive Current from GATEn Pin (Active)		GATEn pin active V_{GATEn} = AGND 1x Power Mode	–60	–40	–20	µA
Drive Current from GATEn Pin (Off)		GATEn pin shut off V_{GATEn} = AGND + 5 V	—	50	—	mA
Voltage Difference Between any GATEn and AGND Pin		I_{GATEn} = –1 µA	10.5	12	13	V

Notes:

1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 1. PSE Port Interface Recommended Operating Conditions[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Measurement Accuracy						
Voltage Measurement	V_{PWR}	V_{PWR} = 50 V	47.5	—	52.5	V
Current Measurement	I (I_{PORT})	I_{PORT} = 7.5 mA	5	7.5	10	mA
		I_{PORT} = 350 mA	335	350	365	mA
		I_{PORT} = 700 mA	670	—	730	mA
Bad FET Measurement (Port Voltage at the Beginning of Detection that Causes a Bad FET Indication)	V_{PORTn}	Force port voltage	–20	–15	–10	V
	I_{PORTn}	Force current through sense resistor	0.5	2.0	4.0	mA

Notes:
1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 2. DC-DC Converter Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Regulator Input Voltage	V_{CAP}	—	3.6	4.3	4.6	V
DC-DC Switcher Output Current	I_{LOAD}	—	0.1	—	200	mA
Regulator Output Voltage	V_{DDA}	55 mA load	3.0	3.3	3.6	V
Regulator Output Current	I_{DDA}	—	0.1	—	55	mA

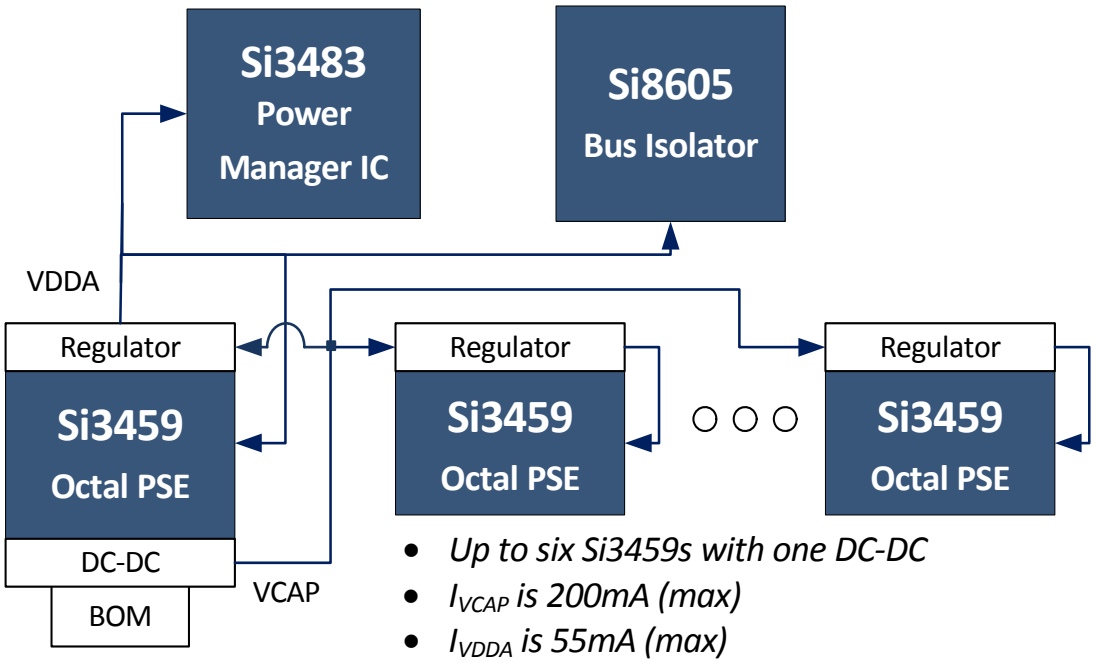


Figure 1. 55 mA and 200 mA Budget Load Components

Table 3. Digital Pin Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Pins	Min	Typ	Max	Unit
Input low Voltage	V_{IL}		$\overline{\text{RESET}}$, SCL, SDAI, A4, A3, A2, A1	—	—	0.8	V
Input High Voltage	V_{IH}		$\overline{\text{RESET}}$, SCL, SDAI, A4, A3, A2, A1	2.0	—	—	V
Input Leakage	I_{IH}	V_{DD} = 4.2 V, Vpin = 4.2 V	$\overline{\text{RESET}}$, SCL, SDAI, A3, AIN, $\overline{\text{INT}}$, $\overline{\text{DCEN}}$	—	—	6	µA
			$\overline{\text{SHDN}}$	—	—	10	µA
	I_{IL}	V_{DD} = 4.2 V, Vpin = 0 V	$\overline{\text{SHDN}}$	—	85	—	µA
	I_{IL}	V_{DD} = 3.3 V, Vpin = 0 V	$\overline{\text{RESET}}$, SCL, SDAI, A4, A3, A2, A1, $\overline{\text{INT}}$, $\overline{\text{DCEN}}$	—	15	50	µA
Output Low Voltage[2]	V_{OL}	I_{SDAO} = 8 mA, $I_{\overline{INT}}$ = 8 mA I_{AOUT} = 8 mA		—	—	0.6	V

Notes:
1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. SDAO and $\overline{\text{INT}}$ are open drain outputs. Tie each pin to V_{DD} with a 1 kΩ resistor for normal operation.

Table 4. AC Timing Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Detection Delay Cycle	t_{DET_CYCLE}	Time from detect command or when PD is connected to port to when detection process is completed.* See Figure 6.	70	—	400	ms
Detection Time	t_{DETECT}	Time required to measure PD signature resistance.* See Figure 6.	—	70	—	ms
Classification Delay Cycle	t_{CLASS_CYCLE}	Time from successful detect in Semi-AUTO mode to classification complete.* See Figure 6.	10	—	30	ms
		Time from classify command in manual mode to class complete.* See Figure 6.	10	—	30	ms
Classification Time	t_{CLASS}	See Figure 6*	10	—	20	ms
Inrush Time	t_{INRUSH}		—	60	—	ms
Overload Time Limit	t_{CUT}		—	60	70	ms
Disconnect Delay	t_{CMPS}		—	360	—	ms
Timer Duration	t_{LIM}	1.71 ms times the value of TLIM12 (TLIM34) field rounded to nearest integer.	0	—	26	ms
DC Disconnect Minimum Pulse Width Sensitivity	t_{DC_SEN}	V_{DRAINn} = –48 V, V_{SENSEn} – AGND > 5 mV	—	—	3	ms
$\overline{SHDN}$ Pin Assertion Threshold (Time from $\overline{SHDN}$ falling edge to port turn off)	T_{SHDN}	Shutdown Priority Mode	1	—	50	µs

***Note:** This timing is determined by the MCU, and the clock reference is guaranteed to be 1 ms ±5%.

Table 5. I²C Bus Timing Specifications[1,2,3,4,5,6]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial Bus Clock Frequency	f_{SCL}	See Figure 5	0	—	800	kHz
SCL High Time	t_{SKH}	See Figure 5	300	—	—	ns
SCL Low Time	t_{SKL}	See Figure 5	650	—	—	ns
Bus Free Time	t_{BUF}	Between STOP and START conditions. See Figure 5	650	—	—	ns
Start Hold Time	t_{STH}	Between START and first low SCL. See Figure 5	300	—	—	ns
Start Setup Time	t_{STS}	Between SCL high and START condition. See Figure 5	300	—	—	ns
Stop Setup Time	t_{SPS}	Between SCL high and STOP condition. See Figure 5	300	—	—	ns
Data Hold Time	t_{DH}	See Figure 5[7]	75	—	—	ns
Data Setup Time	t_{DS}	See Figure 5	100	—	—	ns
Time from Hardware or Software Reset until Start of I²C Traffic	t_{RESET}	Reset to start condition	5	—	—	ms

Notes:

1. All specification voltages are referenced with respect to AGND and DGND at ground. Currents are defined as positive flowing into a pin and negative flowing out of a pin.
2. Not production tested (guaranteed by design).
3. All timing references measured at VIL and VIH.
4. SDAI must be low within ½ SCL clock cycle of SDAO going low for the following reasons:
   a.) During a read transaction, if the Si3459 is letting SDAO go high and another device is driving SDAO low, this should be recognized as bus contention, and the Si3459 should release the bus. If SDAO low is not present on SDAI within ½ clock cycle, the Si3459 will not recognize this as bus contention and will not release the bus.
   b.) During any I²C transaction, the Si3459 will ACK (SDAO low) when its address is sent. The Si3459 "expects" that SDAI will follow within ½ of the SCL clock cycle. If SDAI is not low, the Si3459 will release the bus.
5. SCL and SDA rise and fall times depend on bus pullup resistance and bus capacitance.
6. The time from a fault event to the INT pin being driven is software-defined. The Si3459 produces a new measurement result for the Port voltage or current every 3 msec and every 6 msec for the power supplies and temperature. After each port is monitored, the port status, port event registers, INT register, and INT pin are updated in sequence. For this reason, the INT pin can lag the contents of the event registers by approximately 5 ms.
7. 250 ns minimum and 350 ns maximum for the case where the Si3459 is transmitting data.

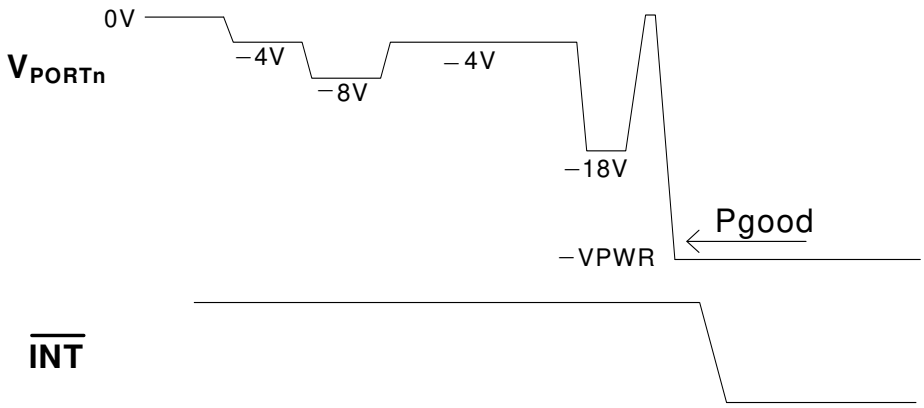


Figure 2. Semi-Auto Timing for Detect, Classification, and Power-Up Sequence

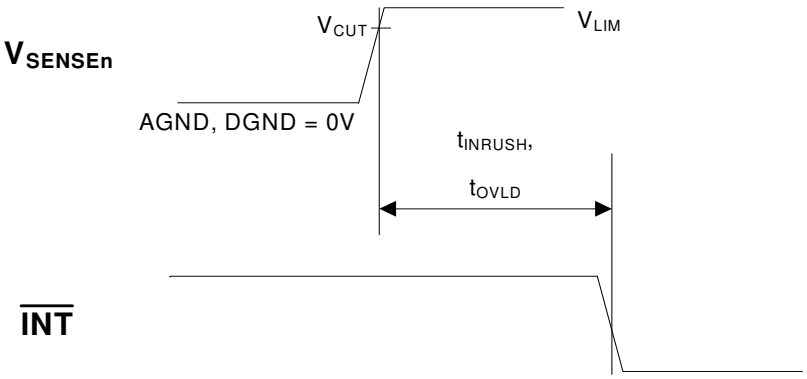


Figure 3. Current Limit Timing

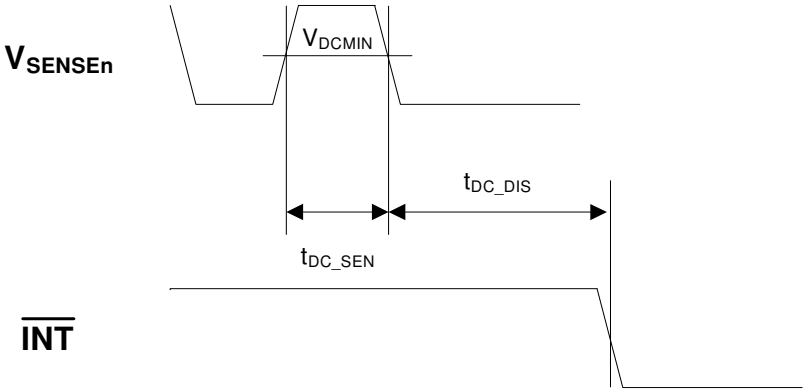


Figure 4. DC Disconnect Timing

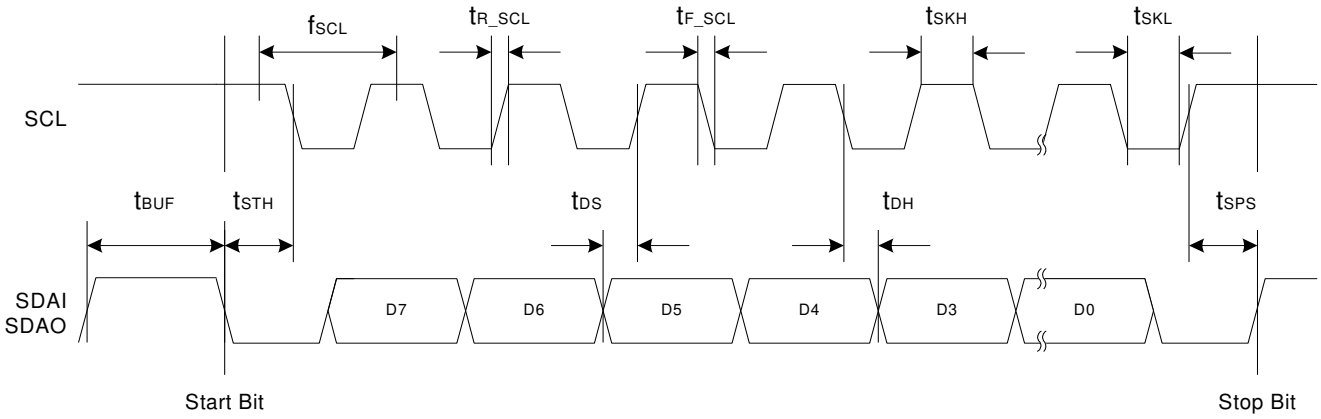


Figure 5. I²C Bus Interface Timing

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Temperature	T_A		–40	—	85	°C
Thermal Impedance	θ_{JA}	4-Layer PCB, no airflow	—	24	—	°C/W
Junction Temperature	T_J		–40	—	125	°C

Table 7. Absolute Maximum Ratings[1]

Type	Parameter	Rating	Unit
Supply Voltages	VPWR to AGND[2]	–0.3 to 70	V
	VDD to DGND[2]	–0.3 to 4.2	V
Voltage on Digital Pins	$\overline{INT}$, $\overline{RESET}$, A4, A3, A2, A1, SCL, SDAI, SDAO, $\overline{SHDN}$, AUTO	DGND–0.3 to DGND+5.8	V
Voltage on Analog Pins	SENSEn	AGND–0.6 to AGND+0.6	V
	GATEn[3,4]	AGND–0.3 to AGND+12	V
	DRAINn	–0.3 to VPWR	V
	KSENSA, KSENSB	AGND–0.6 to AGND+0.6	V
	ISENSE	VPWR–5 to VPWR	V
ESD HBM (Human Body Model[5]) Tolerance		–2 to +2	kV
Maximum Junction Temperature[6]		125	°C
Operating temperature range		–40 to +85	°C
Ambient Storage Temperature		–65 to 150	°C
Lead Temperature (Soldering, 10 Seconds Maximum)		260	°C

Notes:

1. Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Functional operation should be constrained to those conditions specified in Table 1, “PSE Port Interface Recommended Operating Conditions[1],” on page 4 and Table 3, “Digital Pin Recommended Operating Conditions[1],” on page 9.
2. AGND is shorted to DGND inside the package.
3. The GATE pins include an integrated clamp to limit the pins to a minimum of 12 V above AGND, GATE voltages in excess of AGND+12 V may cause permanent disconnect of the affected port.
4. The Si3459 includes protection circuitry to tolerate up to 80 mA of transient current for a maximum of 5 ms.
5. Charged Device Model (CDM), and Cable Discharge Event (CDE) electrical stress tolerance are typically 500 V and 3 kV.
6. Thermal overload protection shuts down the device when the silicon junction temperature exceeds 165 °C, including a temperature hysteresis of 20 °C.

2. Typical Performance Characteristics

This section shows various waveforms that describe typical behaviors and performance of the Si3459. The waveform in Figure 6 shows the part in semi-auto mode with Rgood and Cgood. The Si3459 uses a multi-point detection algorithm. Typically, a Cbad of >10 µF causes an Rlow indication. The Detection Signature is calculated for two measurements at the primary voltage and two measurements at the secondary voltage. For there to be an Rgood indication, the signature must be Rgood in all steps.

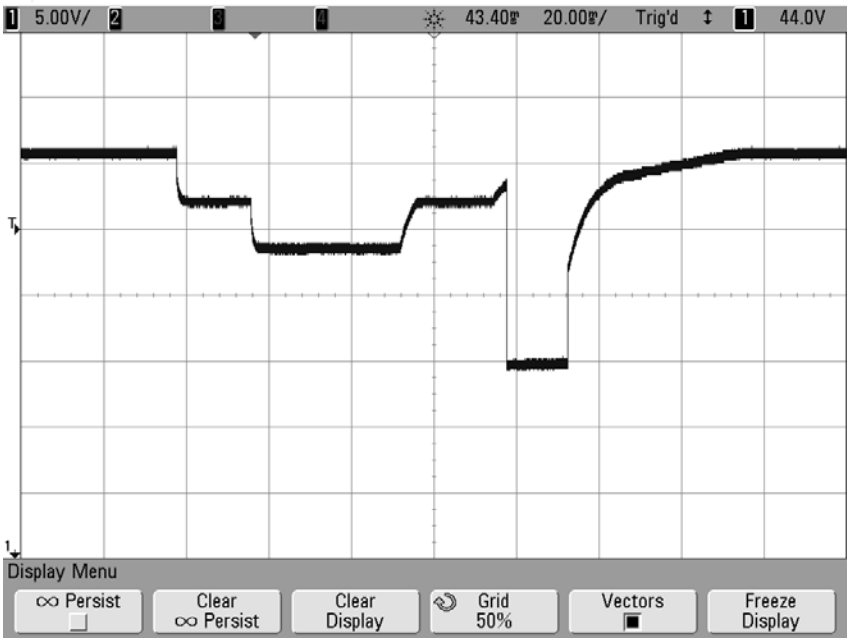


Figure 6. Typical Detect and Classify Sequence (Semi-Auto Mode)

Figure 7 shows the FET gate drive set to 50 µA for FET turn-on. The slew time is about 40 µs with this FET gate drive and is not strongly load-dependent.

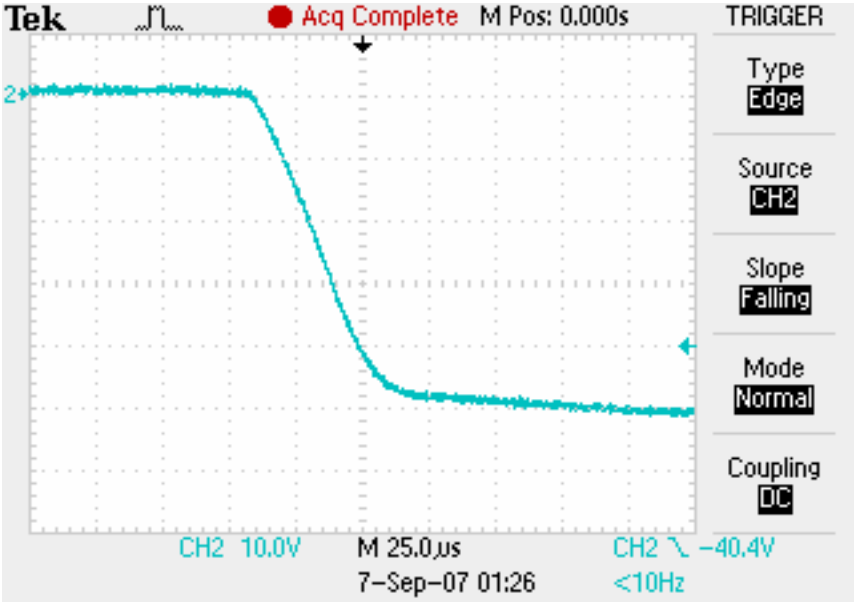


Figure 7. Typical Powerup (220 Ω Load)

The waveform in Figure 8 shows power down when the load is switched to 100 kΩ.

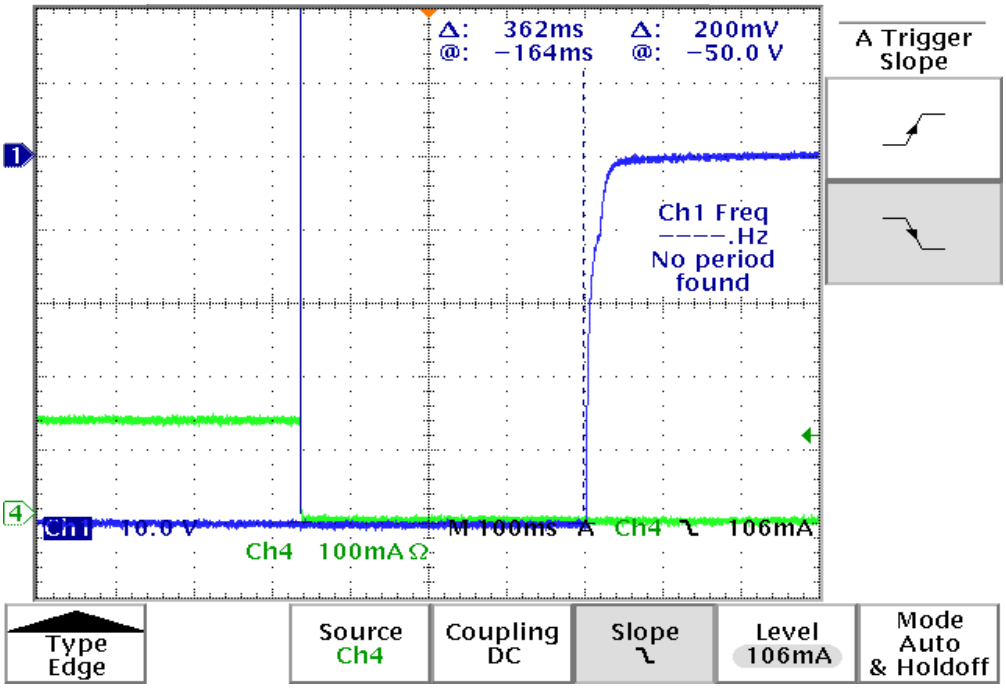


Figure 8. Typical DC Disconnect and Powerdown Sequence

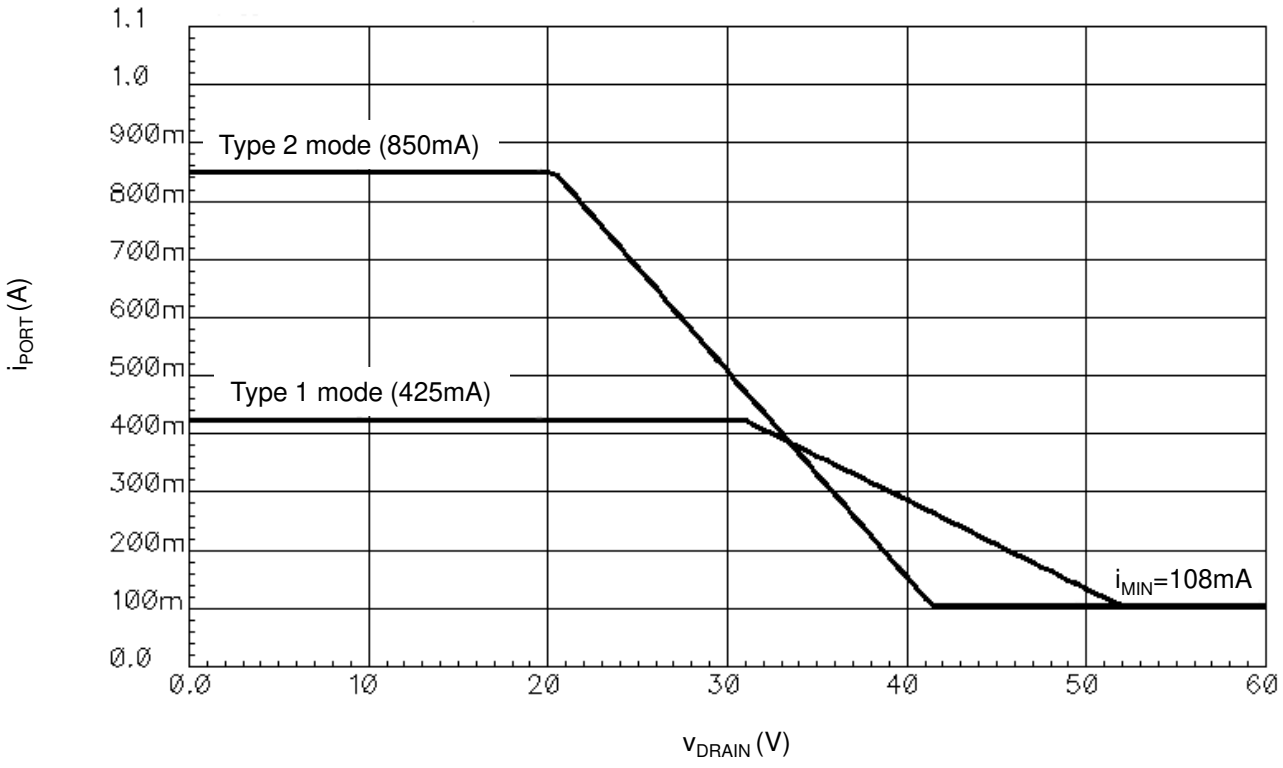


Figure 9. Foldback Current in IEEE 802.3at Type 1 (1X) and Type 2 (2X) Current Limit Modes

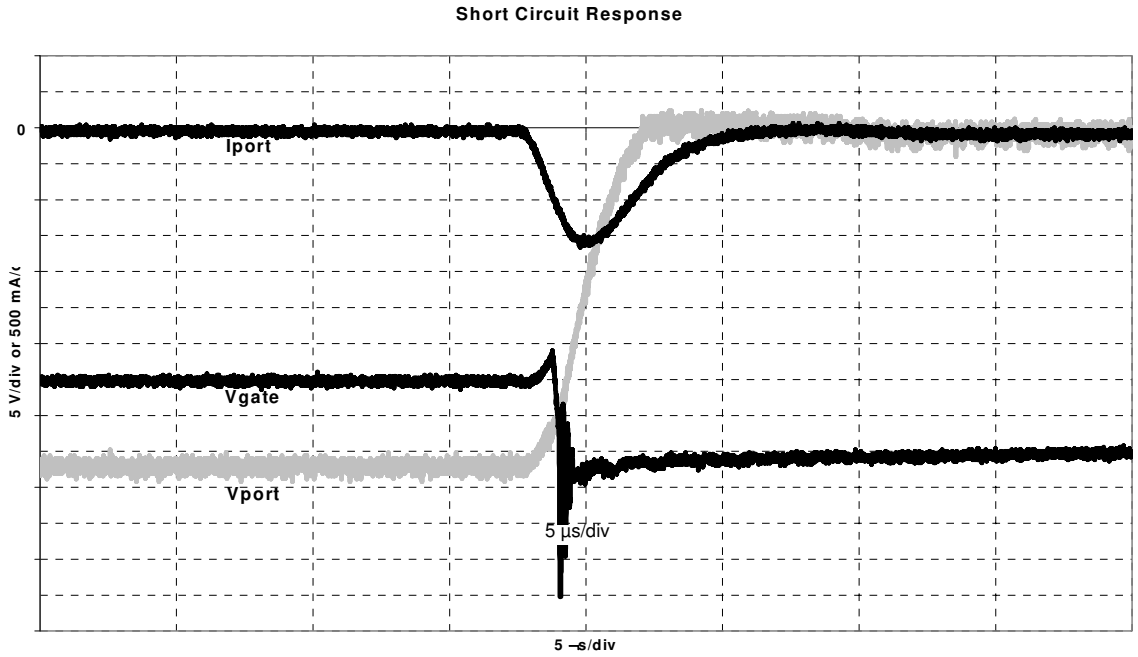


Figure 10. Short Circuit Response

3. Functional Description

Integrating a high-performance microcontroller with high-resolution A/D and D/A capabilities, along with eight independent, high-voltage PSE port interfaces, the Si3459 enables an extremely flexible solution for virtually any PoE switch application. The Si3459 integrates all PSE controller functions needed for an octal-port PoE design.

The Si3459 includes many additional features that can be individually enabled or disabled by programming the extended register set appropriately.

- Per-port current / voltage monitoring and measurement
- Multipoint detection algorithms
- 802.3at support
- Programmable gate drive for external MOSFETs
- Watchdog timer (WDT)

3.1. Octal High-Voltage PSE Port Interfaces

In addition to the IEEE 802.3at detection and classification functionality, the high-voltage port interfaces provide accurate voltage and current control and measurement for each of the eight output ports. The high-voltage port interface circuitry is controlled by the internal microcontroller and includes the following features beyond the 802.3at standard's base requirements.

3.1.1. Per-Port Measurement and Monitoring

The measurement function supports the following capabilities, which enable flexible per-port voltage and current monitoring.

- Detection and classification current measurement with on-chip sense resistors.
- FET current measurement through 0.25 Ω sense resistor with 1 A full-scale.
  - FET current scaling is changed dynamically so as to allow sensitive and accurate dc disconnect, even for a 2x current limit.
- Current measurement offset calibration circuitry.
- V_{PWR} and output voltage measurement.
  - Each channel and range is factory-calibrated.
  - Channel parameters can be read from each port's corresponding registers (output voltage, and current) and are sampled approximately every three milliseconds.
- Supply monitors on V_{DD} and V_{PWR}.

3.1.2. DC Disconnect

DC disconnect may be enabled on any port. If dc disconnect is not enabled when the load is disconnected, the port will not shut off except in response to other fault conditions.

3.1.3. Programmable MOSFET Gate Drivers

To provide maximum system-level design flexibility and optimal EMI performance when interfacing to external high-current MOSFET devices, the Si3459 provides eight independent MOSFET gate drivers with the following features:

- Drive current is 50 µA nominal.
- A 100 mA pull-down that is automatically activated if a current transient of 25% over the programmed current limit is sensed.
- Current limit circuit that can be programmed to 425 or 850 mA typical.
  - Current limit is based on voltage sensed across 0.25 Ω sense resistor.
  - Each channel and range is internally trimmed to ±5% accuracy.
  - Linear foldback behaves as shown in Figure 9 on page 16.

3.2. Operating Modes

The Si3459 normally operates in manual or semi-automatic mode when the AUTO pin is held low. If a valid set voltage level (described in Table 8) is applied to the AUTO pin, the Si3459 enters into fully autonomous operation, independent of a host. When setup voltages indicated as “Reserved” are applied to the AUTO pin, the Si3459 does not enter into fully autonomous mode but remains instead in Shutdown mode. The Si3459 also features dc disconnect detection algorithms to determine when a PD device is disconnected from any of the eight independent ports.

The AUTO mode can be set via the AUTO pin or from the host via I^2C.

At power-up, the Si3459 reads the voltage on the AUTO pin (which can be set by a resistor divider from VDD to GND). If a valid setup voltage is applied, the Si3459 enters into AUTO mode (all ports operate fully autonomously). The AUTO pin voltage level configures the Si3459's behavior through the register default values as summarized in Table 8 below.

In Host-controlled mode, any port can be configured to AUTO mode through the confp_x register. In this case the Host should set the proper port configuration.

Table 8. Auto Pin Configurations

Voltage on the AUTO Pin	IEEE Class	Endpoint vs. Midspan	Restart	Detect+Classify Looping	Register Default Values		
					confp_x	tlimp_x	icutp_x
0 (AUTO pin pulled to GND)	Shutdown				0x00	0x00	0x54
0.22	Reserved						
0.44	Reserved						
0.66	3	Mid	Auto after 2 s	Automatic detect/ class loop	0x7f	0x00	0x54
0.88	Reserved						
1.10	Reserved						
1.32	Reserved						
1.54	3	End	Auto after 2 s	Automatic detect/ class loop	0x3f	0x00	0x54
1.76	Reserved						
1.98	Reserved						
2.20	Reserved						
2.42	4	Mid	Auto after 2 s	Automatic detect/ class loop	0x7f	0x20	0x54
2.64	Reserved						
2.86	Reserved						
3.08	Reserved						
3.30 (AUTO pin pulled to VDD)	4	End	Auto after 2 s	Automatic detect/ class loop	0x3f	0x20	0x54

3.2.1. Additional Operating Modes Notes

- By default the Icut limit is set to 375 mA (**icutp_x** = 0x54; Class 0 or Class 3 limits) initially for all operating modes

3.2.1.1. AUTO Mode-Specific Behaviors

- The “hpen” bit will be set automatically, but only if the 2-event classification was successful
- If there was a successful 2-event classification, then the Icut limit will be increased to 638 mA (Nominal) automatically (**icutp_x** = 0x62)
- The intmask register is set to 0xff in all pin configured AUTO modes

3.2.1.2. Manual and Semi-Auto Mode Behaviors

- To enable IEEE Type 2 Class 4 operation only the “pongen” bit need be set (**tlimp_x** = 0x20)
- It is the host role to set the “hpen” bit, but only if the 2-event classification was successful (the “pongpd” bit is set in the **pwrstatp_x** register)
- It is the host role to set the Icut limit properly

3.2.2. Port ON/OFF Control

The Si3459 offers various options for the Host to control the state of the ports. There is also logic in the part which controls the port state in response to an event.

3.2.2.1. HOST Controlled Port Turn ON

A port can be turned ON in the following ways:

1. In manual Mode, the port can be unconditionally turned on using the proper pushbutton register (set the “on_x” bit (Bit 0) in the **pb_p_x** register).
2. In Semi-Auto mode the port can be also turned on using the proper pushbutton register, but the port will not turn on until a valid PD signature is detected.
3. In Host controlled Auto mode (the AUTO pin is held low), the port will turn on automatically if detection and classification is enabled, a valid signature is detected, and the classification is successful. Otherwise the port can also be turned on using the proper pushbutton register, but in this Mode, the port will not turn on until a valid PD signature is detected. The following steps detail how a port can be turned on in the IEEE Std 802.3at-2012 Type 2 high-power manner:
   a. Enable detection and classification by setting the “detena_x” bit (Bit 2) “classena_x” bit (Bit 3) in the **confp**_x register
   b. Set the “hpen_x” bit (Bit 7) and the “pongen_x” bit (Bit 6) in the **tlimp**_x register to enable the 2-Event classification on the port, and
   c. Set the Icut limit in the **icutp**_x register according to the available power
4. In the Host independent Auto mode (positive voltage is applied to the AUTO pin), the detection and 2-event classification is enabled by default, so the port will turn on automatically if a valid signature is detected and the classification is successful. The current limits are set according to the classification result, so both Type 1 and Type 2 PDs are handled correctly.

3.2.2.2. Autonomous port turn ON

The only occurrence when the port could be turned ON automatically by the Si3459 is when the port is in Auto Mode and the detection and the classification were successful.

3.2.2.3. HOST controlled port turn OFF

A port can be turned OFF at any time using one of the following methods:

1. By setting the “off_x” bit (Bit 1) in the **pb_p_x** registers (0x17, 0x27, 0x37, 0x47): The port is shut down, the event and status registers of the port are set to their default value, and the classification enable and detection enable bits are also cleared in the corresponding **confp**_x register (0x14, 0x24, 0x34, 0x44). The value of the other bits of the **confp**_x register are retained. The associated measurement data registers are also cleared.

2. By setting the “rst_x” bit (Bit 4) in the pb_p_x register: The port is shut down, and all associated events and configurations are cleared (all port registers are set to their default state)

3.2.2.4. Autonomous Port Turn OFF

In the following cases, a port is (or all ports are) turned OFF automatically by the Si3459:

1. In response to the over-temperature event all ports are turned OFF by using the “offall” bit in the **pb_global** register (0x0B). This is equivalent to the situation where the “off_x” of **pb_p_**x registers (0x17, 0x27, 0x37 and 0x47 for ports 1–4, respectively) were set.
2. In response to a UVLO event (either VDD or VPWR UVLO), all ports are reset by using the “rstall” bit in the **pb_global** register (0x0B). This is equivalent to the situation where the “rst_x” of the **pb_p_**x registers were set.
3. In response to the SHDN pin assertion the low priority ports are turned OFF by using the “off_x” bit (Bit 1) of **pb_p_**x register.
4. In response to an over-current event the port is shut down, i.e.: power is removed from the DRAINn pin, and the “pe_x” (Penable bit; Bit 0) and the “pg_x” (Pgood bit, Bit 1) for that port is set.
   The events are not cleared, and the full port configuration is retained.

3.3. V_{DD} Ramp Time

It is recommended that V_{DD} ramp into the operational range within 1 ms if reset is not held low. Slow ramp times are acceptable if reset is held low until V_{DD} is in the operational range. For additional detail on VDD and undervoltage lockout, refer to “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .

3.4. I^2C Protocol

Controlling the features of the Si3459 is possible by programming a series of registers identified in the Register Map (see "4. Register Map" on page 25). Registers are accessible through a three-wire, I^2C-compatible serial interface.

3.4.1. Slave Address

The Si3459 slave base address is pin-assigned by logical ORing HW pins {A[4:1]} with value 0x20.

The complete base address is formed as “01[A4][A3][A2][A1]A0b”.

A0 is not a hardware bit. The device acts as two “virtual” quad devices with the address of the first quad being A0 = 0 and the address of the second quad being A0 = 1 in the I^2C protocol (see Figure 11 on page 22).

3.4.1.1. Available I^2C Transfer Types

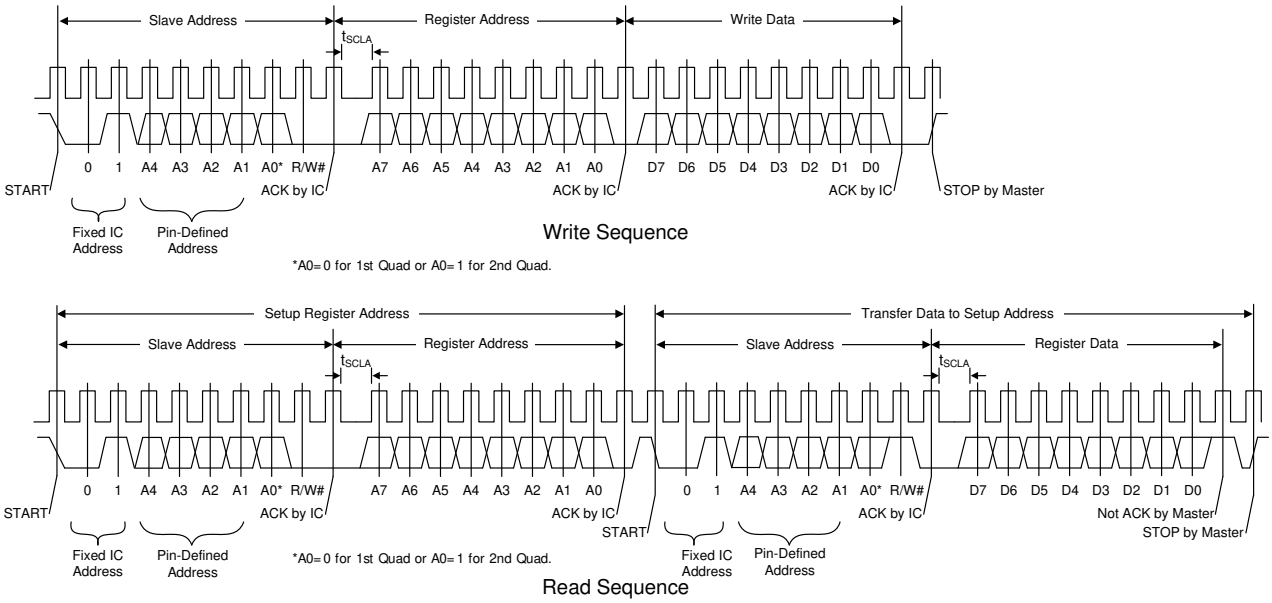


Figure 11. I²C Read and Write Sequences

8-Bit Read

All registers can be accessed this way, but it is not recommended for reading registers storing parametric measurement data (Iport and Vport, registers 0x19–0x1c, 0x29–0x2c, 0x39–0x3c, 0x49–0x4c).

Example Sequence

1. START condition, followed by the target slave's 7-bit address, and a write flag. The sequence is ACKed by the Si3459.
2. Then an 8-bit Si3459 register address is provided followed by an ACK. These steps set up a pointer register within the Si3459 that points to the address of an internal register to be read.
3. The transaction continues by sending a repeated START condition, followed by the target slave's 7-bit address, and a read flag. This sequence is ACKed by the Si3459.
4. Then the 8-bit IC register data is provided by the Si3459 (slave). This occurrence is followed by a master NACK (Not ACK).
5. Then the master frees the bus by sending a STOP condition.

See Figure 11, “I2C Read and Write Sequences,” on page 22 for more details.

8-Bit Write

All registers can be accessed this way (except the read only registers).

Example Sequence

1. START condition, followed by the Si3459 7-bit address, and a write flag. This is ACKed by the IC.
2. Then an 8-bit IC register address is provided followed by an ACK by the Si3459.
3. The transaction is completed by sending 8-bits of register data. This is ACKed by the Si3459.
4. Then the master frees the bus by sending a STOP condition.

See Figure 11, “I2C Read and Write Sequences,” on page 22 for more details.

16-Bit Read

This is the recommended access mode for reading registers storing parametric measurement data (Iport and Vport, registers 0x19–0x1c, 0x29–0x2c, 0x39–0x3c, 0x49–0x4c). Only these registers can be accessed this way in this mode.

The two byte (16-bit) read follows the same protocol described in the 8-bit read paragraph above, with the extra byte appended to the data field before the STOP condition. In this case, the Master should ACK the first byte, and NACK the second byte.

Example: Reading 2 Bytes from Offset 0x19 Gives the Current Measurement of Port 1

1. Start condition, followed by the target slave's 7-bit address, and a write flag. The sequence is ACKed by the Si3459.
2. Then an 8-bit Si3459 register address is provided followed by an ACK. These steps set up a pointer register within the Si3459 that points to the address of an internal register to be read.
3. The transaction continues by sending a repeated START condition, followed by the target slave's 7-bit address, and a read flag. This sequence is ACKed by the Si3459.
4. Then the LSB of PORT1 CURRENT MEASUREMENT (8-bit) data is provided by the Si3459 (slave). This occurrence is followed by a master ACK.
5. Then the MSB of PORT1 CURRENT MEASUREMENT (8-bit) data is provided by the Si3459 (slave). This occurrence is followed by a master NACK.
6. Then the master frees the bus by sending a STOP condition.

See Figure 11, “I2C Read and Write Sequences,” on page 22 for more details.

Quick Access to the Interrupt Register

Whenever a STOP is detected by the slave, its internal register address pointer is reset. Therefore, the next I^2C Read transaction will return the contents of the Interrupt register (0x00).

The transaction has to be executed on both quads using the A0 address bit to read the Interrupt register of both quads.

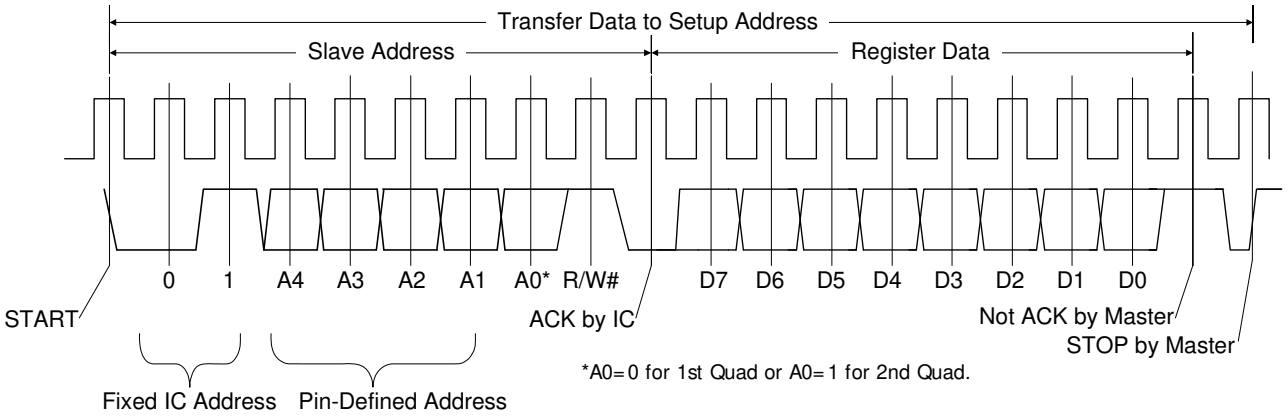


Figure 12. Quick Access Transaction

3.4.1.2. Global Address

Each device on the bus will respond to the global address (100 0000b) in exactly the same way it would to a read or write transaction using its specific slave address. The global address is primarily used to configure (write) all slaves the same after the PSE system is powered up. Global read transactions should be avoided.

3.4.1.3. Alert Response Address (ARA)

The ARA is used by the master as a quick way to determine which slaves are asserting (pulling low) the nINT line. The ARA address is 000 1100b

Each IC (“slave”) implements the following protocol:

- Only slaves that are asserting the nINT line respond when the master uses the ARA in a read cycle. All slaves that are not asserting nINT ignore read cycles that use the ARA.
- Each slave responding to the ARA transmits a byte consisting of its address in the upper 7 bits, and a 1 in the least significant bit.

- As each bit in the byte is transmitted, the slave determines whether to continue transmitting the remainder of the byte or terminate transmission. The slave terminates when it sees a 0 on SDA at a time when it's attempting to send a 1; otherwise it continues transmitting bits until the entire byte has been sent.
- If a slave completes transmission of the entire byte without terminating, it releases (stops asserting) the nINT line. Any slave that terminated transmission continues to assert the nINT line.

The result of this protocol is that the slave with the lowest address will complete the transmission and won't respond to subsequent ARA read transactions until its event registers have been cleared. Other slaves, with higher addresses, terminate but will respond to the next ARA read cycle. Therefore, each time the master performs a read cycle using the ARA it receives the address of a different slave until all slaves have sent their addresses without terminating.

3.5. DC-to-DC Converter Description

The Si3459 includes a dc-dc converter for generation of an approximately 4.3 V intermediate power rail, which is further down-regulated to create the 3.3 V VDD power rail necessary for MCU operation and other support.

The dc-dc converter consists of a buck converter with accompanying external components to step down VPWR to approximately 4.3 V on the enabled "primary" converter. This voltage, called VCAP, can also be bussed to up to five adjacent "secondary" controllers. Each controller includes a series regulator for generation of 3.3 V for local use by that controller and an optional digital bus isolator.

The converter is enabled by asserting (tying low) $\overline{\text{DCEN}}$. In fact, $\overline{\text{DCEN}}$ should be asserted on the primary and all secondary controllers.

While the primary controller requires several external components to enable the dc-dc (see " DC-DC Converter Block Diagram" on page 2), the secondary controllers do not require those external components. On the secondary controllers, the SWO pin should be direct-tied to VPWR.

If $\overline{\text{DCEN}}$ is left floating the dc-dc converter is disabled, which eliminates excess current draw by the VPWR pin. To disable the dc-dc converter, the related pins (DCENb, CAP, and SWO) should be left floating.

The ISENSE pin implements a cycle-by-cycle current limit by comparing a sensed voltage to an internal reference. When the external power FET is conducting, if ISENSE drops more than 200 mV below VPWR, the FET will be shut off immediately to limit excessive currents. An appropriate external resistor should be selected to set the desired peak current level (i.e., Ipeak = 200 mV/Rsense). If ISENSE is left floating, an internal pull-up will effectively disable the current limit feature.

In the event of an extreme overcurrent event (e.g., short-circuit), the dc-dc output voltage, CAP, will drop below its target level of 3.6 V. If CAP falls below 90% of that level (i.e., 3.24 V) a dc-dc fault will be declared and the dc-dc and LDO will power down. The dc-dc will then attempt to restart in 4 ms intervals until the overcurrent fault is removed.

4. Register Map

4.1. Register Set

Table 9 lists the Si3459 registers. The Si3459 appears to software as two “virtual quads” in that there is a complete, independent set of the below registers associated with each virtual quad. The A0 I^2C address bit distinguishes the two virtual quads. A0 is not a hardware pin; it is reported as either 0 or 1 according to which virtual quad is being addressed via the I^2C protocol.

Table 9. Si3459 Registers

Register		R/W	Port[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr[1]	Name											Auto Tied to DGND
Interrupt												
0x00	int	RO	Global	Overtemp	fetbad	uvlo3	uvlo48	p_4_ev	p_3_ev	p_2_ev	p_1_ev	0010 0000
0x01	intmask	R/W	Global	Status	ifault	startfault	dis	class	det	pwrgd	pwrena	1000 0000
Global Event Registers												
0x02	evn_global	RO	Global	Overtemp	fetbad	uvlo3	uvlo48	tsd	Reserved	Reserved	Reserved	0010 0000
0x03	evn_global_cor	COR	Global	Overtemp	fetbad	uvlo3	uvlo48	tsd	Reserved	Reserved	Reserved	0010 0000
Global Status Registers												
0x05	Status	RO	Global	tsd	slave_addr[4:0]					Reserved	Auto	0000 0000
0x06	Temperature	RO	Global	Die Temperature								0000 0000
0x07	VPWR_LSB	RO	Global	Vmain_LSB								0000 0000
0x08	VPWR_MSB	RO	Global	Vmain_MSB								0000 0000

Notes:
1. Register addresses not listed in the table are reserved and should not be written to.
2. The PORT column indicates which ports are associated with each register. For example, “2” means the register is associated with Port 2 only; “Global” refers to slave-level status and control registers.