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Si3480

Functional Block Diagram

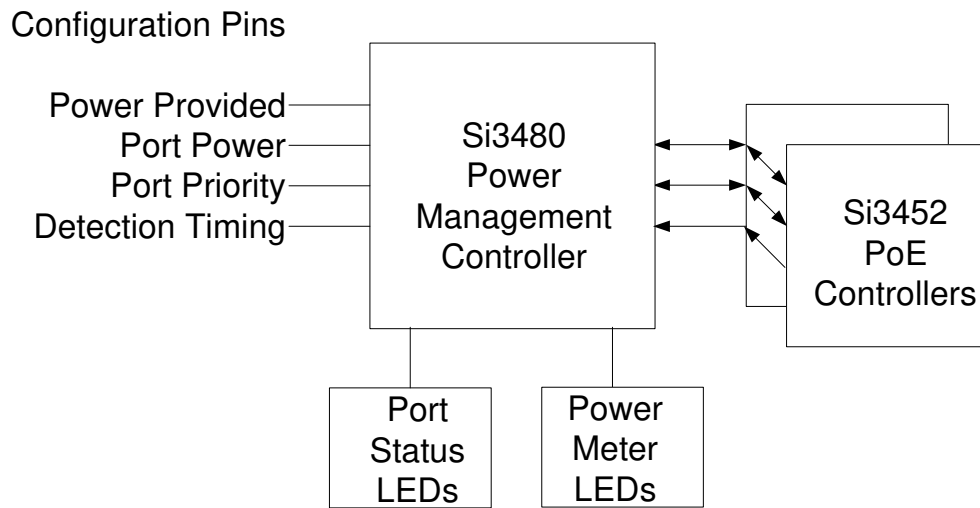


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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Description	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Temperature Range	T_A	No airflow	-40	—	85	°C
V_{DD} Supply Voltage	V_{DD}	All operating modes	2.7	—	3.6	V
LED Current	I_{LED}	LEDBANK pin at 50% duty cycle	—	20	—	mA

Table 2. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient Temperature under Bias		-55	—	125	°C
Storage Temperature		-65	—	150	°C
Voltage on any I/O with respect to GND	$V_{DD} > 2.2$ V	-0.3	—	5.8	V
Voltage on V_{DD} with respect to GND		-0.3	—	4.2	V
Maximum Total LED Current		—	—	500	mA
Maximum LED Current per Pin		—	—	100	mA

Note: Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. Electrical Characteristics*

Description	Symbol	Test Conditions	Min	Typ	Max	Units
Input High	V_{IH}	RST, SCL, SDA, ALTCFG	2.0	—	—	V
Input Low	V_{IL}	RST, SCL, SDA, ALTCFG	—	—	0.8	V
Input Leakage Current	I_{IL}	RST, and all CFG pins SCL and SDA high	—	—	±1	µA
Output Low (LED pins, SCL and SDA)	V_{OL}	$I_{OL} = 8.5$ mA $I_{OL} = 25$ mA	— —	— 1.0	0.6 —	V
Output High (LED Pins)	V_{OH}	$I_{OH} = -3$ mA $I_{OH} = -10$ mA	— —	— $V_{DD}-0.8$	$V_{DD}-0.7$ —	V
Sense Accuracy for Analog Configuration Pins	ΔV_{SENSE}	Percent of V_{DD}	-1.5	—	+1.5	%
V_{DD} Current	I_{DD}	$V_{DD} = 3.0$ V $V_{DD} = 3.6$ V	— —	— —	10 13	mA

*Note: $V_{DD} = 2.7$ to 3.6 V, -40 to 85 °C unless otherwise noted.

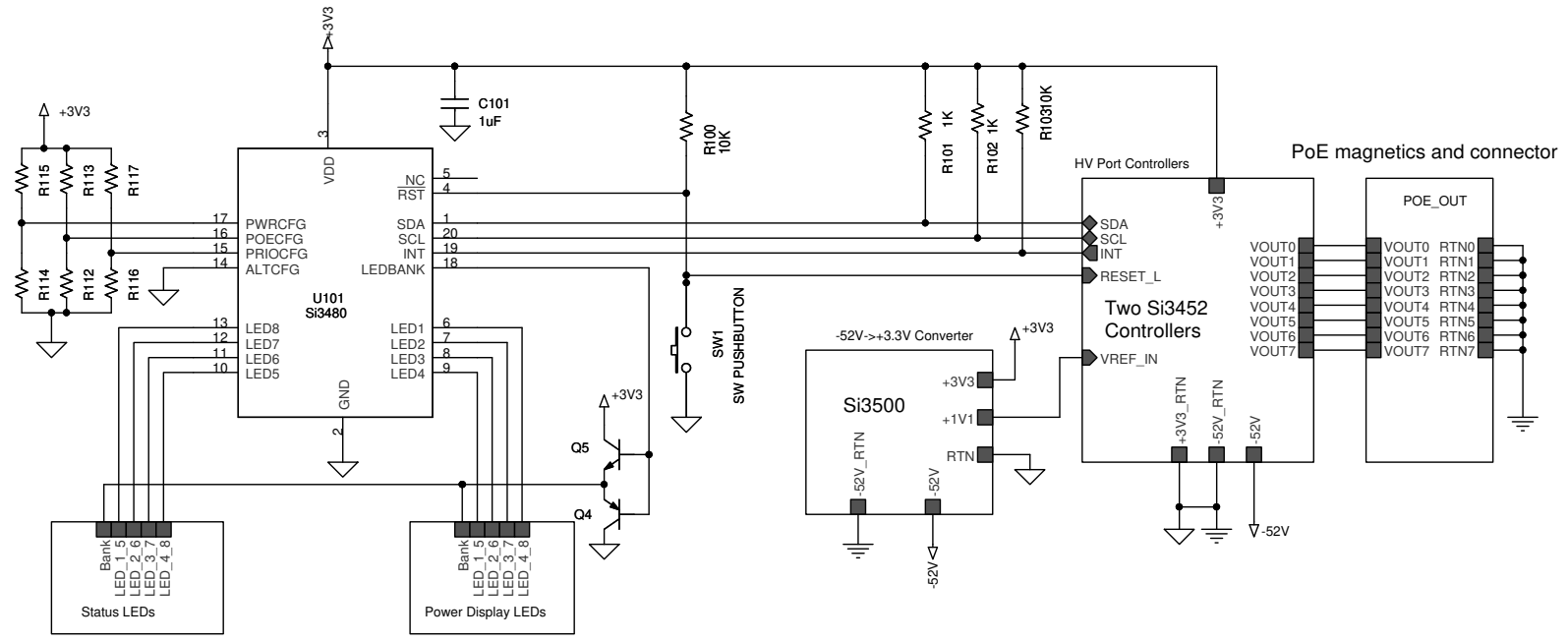


Figure 1. Si3480 Typical Application Schematic

Recommended Designs

2. Typical Application Schematic

3. Functional Description

3.1. Device Initialization and Configuration Pins

The Si3480 will discover Si3452 devices at addresses 0x20 and 0x21 at power up. If only one device is found, it will manage the power for four ports. If two devices are found, the Si3480 will manage power for eight ports. For the case of eight ports, ports 1–4 are associated with the Si3452 at address 0x20, and ports 5–8 are associated with device 0x21. After power-up, the CFG pins are measured to determine how power is to be managed.

3.1.1. Pin PWRCFG

The voltage on pin PWRCFG specifies the power provided by the system power supply. The power provided is:

$$P_{\text{PROVIDED}} = 200 \times V_{\text{PWRCFG}} / V_{\text{DD}} \text{ (Watts)}$$

The total power provided is the rating of the main power supply for continuous output. The amount of total power provided depends on the expected usage. 30 W of total power provided might be realistic for a four-port system that only supports 15.4 W per port and is not expected to have PDs on all ports. 150 W of total power might be realistic for an eight port system that supports 30 W per port and is expected to have category 2 PDs connected to all ports.

To avoid overloads, a port will not be granted power unless the power consumed plus the power requested according to classification (4, 7, 15.4, or 30 W) allows for 15% power supply reserve. If, due to variation in power over time, the total power consumed by all the loads exceeds the power supply capacity, the power manager will shut down ports in priority order.

3.1.2. Pin POECFG

The voltage on the POECFG pins determines how many ports are enabled for 30 W maximum per port. If the voltage is at ground, no ports will be enabled for 30 W maximum. If the voltage is at V_{DD} , all ports are enabled for 30 W maximum. The number of ports enabled for 30 W is:

$$N = 8 \times V_{\text{POECFG}} / V_{\text{DD}} \text{ rounded to the nearest integer}$$

In a four-port system, $V_{\text{POECFG}} > V_{\text{DD}} / 2$ means that 30 W is enabled on all ports.

If a port is enabled for 30 W maximum, special high-current Ethernet transformers should be used, and the user should be aware that the wiring to the PD should be category 5E or better or category 5 manufactured after 1995 (See 802.3 clause 33 for details).

3.1.3. Pin PRIOCFG

The Si3452 implements a port priority set according to the voltage on pin PRIOCFG. Low priority ports may be turned off if a high priority port is requesting power. Also, low-priority ports are shut down before high-priority ports in case the power supply is overloaded. Similar to the POECFG pin, the number of ports that are high priority is:

$$N = 8 \times V_{\text{PRIOCFG}} / V_{\text{DD}} \text{ rounded to the nearest integer}$$

3.1.4. Pin ALTCFG

The Si3480 can be set to put the Si3452 parts in either Alternative A or Alternative B timing mode. Alternative A is used when the power is applied to wire pairs 1,2 and 3,6. Alternative B is used when the power is applied to wire pairs 4,5 and 7,8. Timing between detection pulses is less than 0.5 s for Alternative A and greater than two seconds for Alternative B. The timing is Alternative A if pin ALTCFG is tied low and Alternative B if the pin is tied high.

3.2. I²C Communication

The open drain Si3480 pins (SDA, SCL, and INT) are for I²C communication and connect to the Si3452/53 pins with the same name. See the Si3452/53 data sheet for more detailed information.

3.3. LED Control

The LED pins each connect to two LEDs. The LED being driven is determined by the LEDBANK pin in a normal multiplexing fashion. The LEDBANK pin is driven at 500 Hz (1 msec high and 1 ms low).

4. LEDs

Upon power application or reset (by SW1 in the upper left corner), the Si3480 probes to see whether there are one or two Si3452 ICs connected (4 or 8 ports). The Si3480 then controls the LED display in the start-up sequence described and automatically starts managing the power among the ports as determined by the configuration pins. After start-up, the Si3480 controls the power meter and port status LEDs give a visual indication of the status.

4.1. Start-Up LED Sequence

During start-up, the LEDs are lit in the sequence listed in Table 4 (1 second for each step).

Table 4. LED Sequence

Step	Action
1	All LEDs on.
2	Port 1 LED and either four or eight power meter LEDs to indicate the number of 4-port controllers found by the Si3480 (no LEDs if no controllers are found).
3	Port 2 LED and zero to eight power meter LEDs to indicate the provided power as determined by reading the voltage at the PWRCFG pin in 25 W steps (e.g. two LEDs is 50 W).
4	Port 3 LED and zero to eight power meter LEDs to indicate the number of PoE+ ports as determined by reading the voltage at the POECFG pin.
5	Port 4 LED and zero to eight power meter LEDs to indicate the number of high-priority ports as determined by reading the voltage at the PRIOCFG pin.

4.2. Port Status LEDs

After the start-up sequence, the port status LEDs display the patterns listed in Table 5 to indicate port status.

Table 5. Port LED Pattern Definitions

Port LED Pattern	Meaning
Flashing once every two seconds	Detection and Classification in process
Continuously lit	PoE port is on
Blinks off once every two seconds	PoE+ port is on with a class 4 PD load (30 W granted)
Flashing five times per second	Port overloaded
Flashing twice every two seconds	Power denied due to lack of power

For a port overload, an open circuit must be seen before the port is re-enabled; that is, the PD must be unplugged, and the overload must be cleared.

Ports are turned off in priority order if more than the available power is being consumed. If the amount of power consumed is >10% more than the available power, all low-priority ports are shut off immediately.

Ports are not granted power unless there is enough power available to grant the requested power (based on classification) with 15% margin. The 15% margin generally avoids situations where a port is granted power and then later turned off due to lack of power.

If a port is turned off or denied power due to a lack of available power, the LED continues flashing twice every two seconds until enough power is available to turn the port on or the PD is unplugged.

4.3. Power Meter LEDs

The power meter LEDs light consecutively, indicating the amount of power that is being consumed. There are eight LEDs in the power meter. The LEDs will light in bar graph fashion:

Number_LEDs_Lit = $8 \times \text{Total_Power_Consumed} / (0.85 \times \text{Provided_Power} - 4 \text{ W})$ (rounded down)

The eighth power meter LED is generally a red LED. If this LED is lit, it means that there is not enough power available to grant even a Class 1 load power and maintain a 15% margin. The eighth LED is flashed five times per second if the Si3452 controllers report a power supply undervoltage.

5. Pin Descriptions

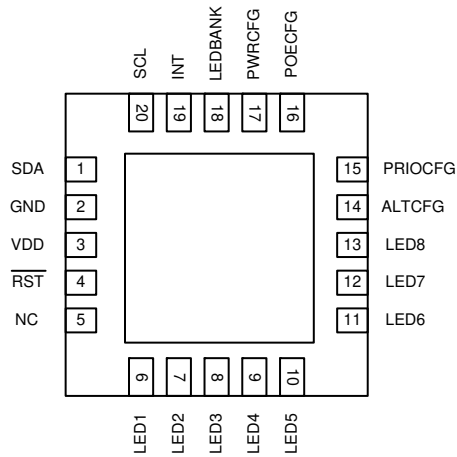


Table 6. Si3480 Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Function
1	SDA	Open Collector	Connect to Si3452 SDA and pull-up resistor.
2	GND	Power	Ground.
3	VDD	Power	VDD.
4	RST	Input	Reset (a low will reset the Si3480).
5	NC	NC	Do not connect to this pin.
6	LED1	Output	Pins LED1–LED4 work with Pin LEDBANK to drive the eight power meter LEDs.
7	LED2	Output	
8	LED3	Output	
9	LED4	Output	
10	LED5	Output	Pins LED5 – LED8 work with Pin LEDBANK to drive the eight port status LEDs.
11	LED6	Output	
12	LED7	Output	
13	LED8	Output	
14	ALTCFG	Input	Low is Alternative A timing, High is Alternative B timing. See "3.1.4. Pin ALTCFG" on page 6.
15	PRIOCFG	Input	This pin sets the number of ports that are high priority. See "3.1.3. Pin PRIOCFG" on page 6.
16	POECFG	Input	The pin sets the number of ports that are high power. See "3.1.2. Pin POECFG" on page 6.
17	PWRCFG	Input	This pin sets the power provided. See "3.1.1. Pin PWRCFG" on page 6.
18	LEDBANK	Output	This pin determines which LED bank is being turned on.
19	INT	Input	Connect to Si3452 INT and pull up resistor.
20	SCL	Open Collector	Connect to Si3452 SCL and pull up resistor.

6. Ordering Guide

Ordering Part Number	Description	Package Information
Si3480-A01-GM	Power management controller	20 pin 4x4 mm QFN RoHS compliant
Si3480 Kit	An eight-port evaluation kit with the Si3480, two Si3452 controllers and the Si3500 for generating the 3.3 V supply from the PoE supply	Evaluation Board

Notes:

1. Add "R" to the part number to denote tape and reel option (Si3480-A01-GMR)
2. The ordering part number is not the same as the device mark. See "9. Top Marking: 20-Pin QFN" for device marking information.

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7. Package Outline

Figure 2 illustrates the package details for the Si3480. Table 7 lists the values for the dimensions shown in the illustration.

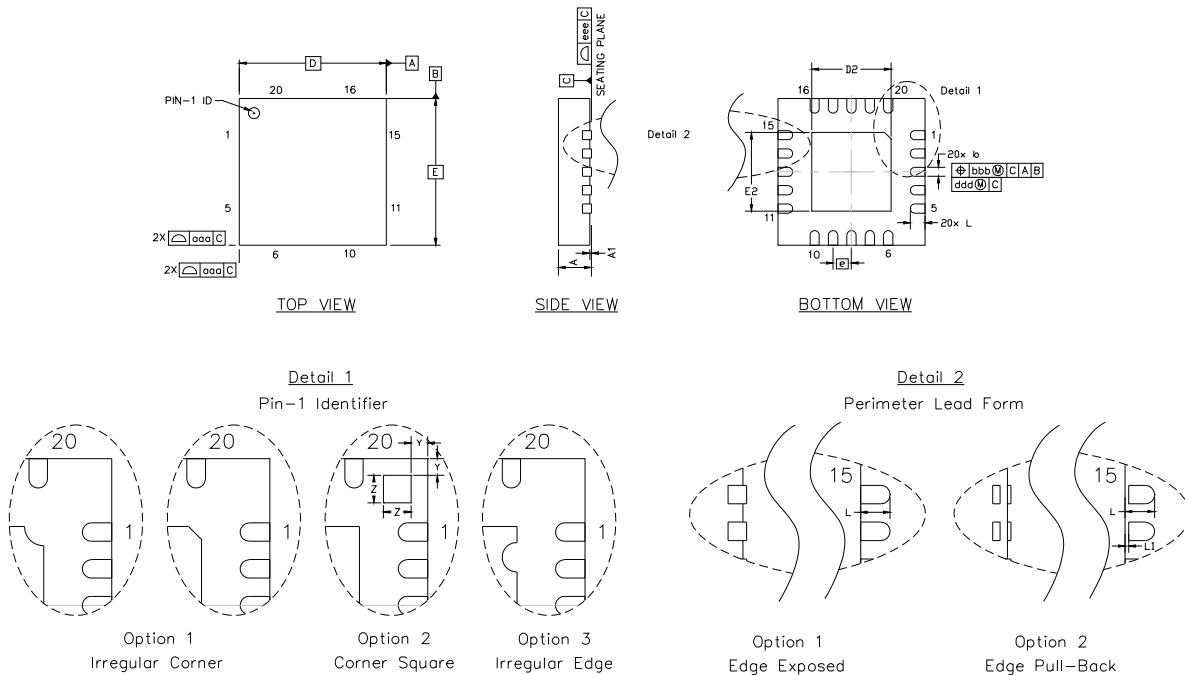


Figure 2. QFN-20 Package Drawing

Table 7. QFN-20 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.80	0.90	1.00	L	0.45	0.55	0.65
A1	0.00	0.02	0.05	L1	0.00	—	0.15
b	0.18	0.25	0.30	aaa	—	—	0.15
D	4.00 BSC.			bbb	—	—	0.10
D2	2.00	2.15	2.25	ddd	—	—	0.05
e	0.50 BSC.			eee	—	—	0.08
E	4.00 BSC.			Z	—	0.43	—
E2	2.00	2.15	2.25	Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VGGD except for custom features D2, E2, Z, Y, and L which are tolerated per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Landing Pattern: 20-Pin QFN

Figure 3 illustrates the landing pattern for the Si3480. Table 8 lists the values for the dimensions shown in the illustration.

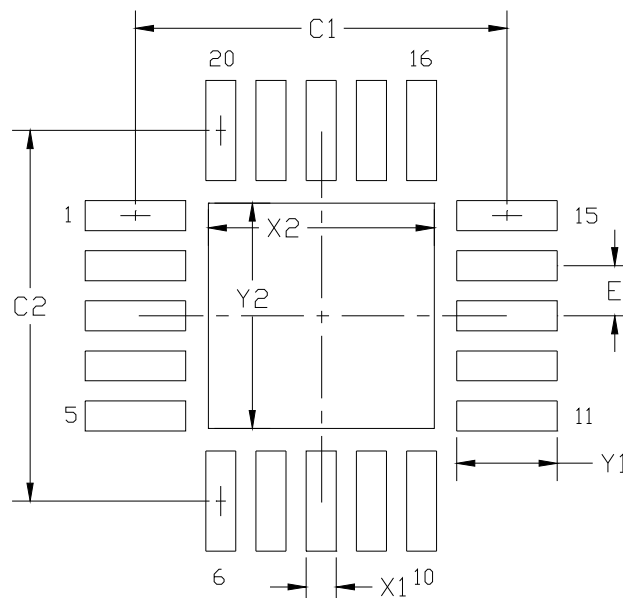


Figure 3. QFN-20 Recommended PCB Land Pattern

Table 8. QFN-20 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	3.70		X2	2.15	2.25
C2	3.70		Y1	0.90	1.00
E	0.50		Y2	2.15	2.25
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 2x2 array of 0.95mm openings on a 1.1 mm pitch should be used for the center pad to assure the proper paste volume (71% Paste Coverage).

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking: 20-Pin QFN

Figure 4 illustrates the top markings for the Si3480. Table 9 explains the values for the markings shown in the illustration.

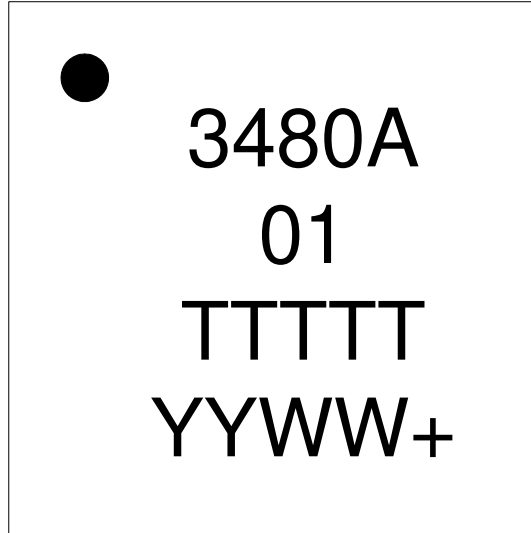


Figure 4. Si3480 Top Marking

Table 9. Top Marking Explanations

Line 1 Marking:	Pin 1 Identifier	Circle, 0.25 mm diameter
	Product ID	Si3480A
Line 2 Marking:		01 = Firmware revision 01
Line 3 Marking:	TTTTT = Trace Code	
Line 4 Marking:	YYWW = Date Code	Assigned by Assembly Contractor YY = Last 2 digits of current year (ex. = 2010) WW = Current Work Week
	Lead Free Designator	+

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 1.0

- Updated Table 3
 - Updated typical output low, typical output high, and sense accuracy.
 - Updated pin description.

Revision 1.0 to Revision 1.1

- Added “Not Recommended for New Designs” watermark.

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