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Si4010-C2

CRYSTAL-LESS SOC RF TRANSMITTER

Features

- Crystal-less operation
  - Optional crystal oscillator input
- High-Speed 8051 µC Core
  - Pipeline instruction architecture
  - 70% of instructions in 1 or 2 clocks
  - Up to 24 MIPs with 24 MHz clock
  - 4 kB RAM/8kB NVM
  - 128 bit EEPROM
  - 256 byte of internal data RAM
  - 12 kB ROM embedded functions
  - 8 byte low leakage RAM
- Extensive Digital Peripherals
  - 128 bit AES accelerator
  - 5/9 GPIO with wakeup functionality
  - LED driver
  - Data serializer
  - High-speed frequency counter
  - On-chip debugging: C2
  - Unique 4 byte serial number
  - Ultra low-power sleep timer
- Single Coin-Cell Battery Operation
  - Supply voltage: 1.8 to 3.6 V
  - Standby current < 10 nA
- High-performance RF transmitter
  - Frequency range: 27–960 MHz
  - +10 dBm output power, adjustable
  - Automatic antenna tuning
  - Symbol rate up to 100 kbps
  - FSK/OOK modulation
  - Manchester, NRZ, 4/5 encoder
- Analog Peripherals
  - LDO regulator with POR circuit
  - Battery voltage monitor
- Temperature range –40 to +85 °C
- Automotive quality option, AEC-Q100 (Pending final qualification testing)
- 10-pin MSOP/14-pin SOIC

Applications

- Garage and gate door openers
- Remote keyless entry
- Home automation and security
- Wireless remote controls

Description

The Si4010 is a fully integrated crystal-less CMOS SoC RF transmitter with an embedded CIP-51 8051 MCU. The device can operate over the –40 to 85 °C temperature range without requiring an external crystal reference source reducing board area and BOM cost. The device includes an 8 kB non volatile memory block for programming the user's application along with a 12 kB ROM of embedded support code for use in the user's application. The Si4010 includes Silicon Laboratories' 2-wire C2 Debug and Programming interface, which allows customers to download their code during the development stage into the on-board RAM for testing and debug prior to programming the NVM.

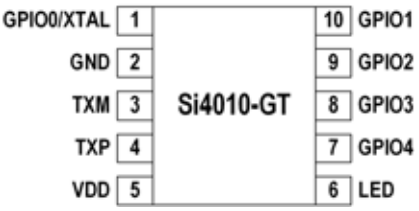
The Si4010 is designed for low power battery applications with standby currents of less than 10 nA to optimize battery life and features automatic wake on button press support to efficiently move from the standby to active mode state with minimal customer code support. Built in AES-128 hardware encryption along with a 128-bit EEPROM can be used to create robust data encryption of the transmitted packets. A unique 4-byte serial number is programmed into each device ensuring non-overlapping device identifiers.

The RF transmitter features a high efficiency PA capable of delivering output power up to +10 dBm and includes an automatic antenna tuning algorithm. This algorithm adjusts the antenna tuning at the start of each packet transmission for optimal output power minimizing the impact of antenna impedance changes due to the remote being held in a user hand. The devices supports FSK and OOK modulations and includes automatic output power shaping to reduce spectral spreading and ease regulatory compliance. The output frequency can be adjusted via software over the entire 27 to 960 MHz range. The output data rate is software adjustable up to a maximum rate of 100 kbps.

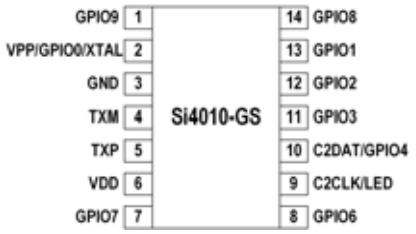
Ordering Information:

See page 15.

Pin Assignments



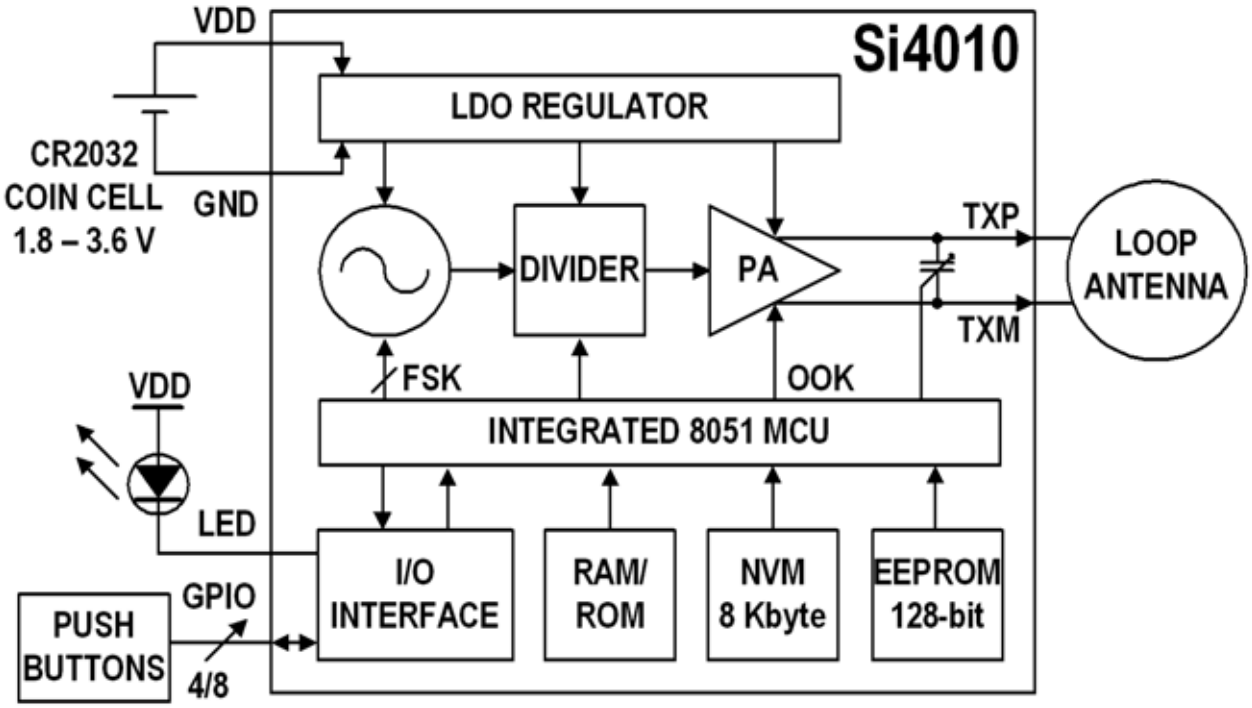
10-Pin MSOP



14-Pin SOIC

Patents pending

Functional Block Diagram



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1. System Overview

The Si4010 is a fully integrated crystal-less CMOS SoC RF transmitter with an embedded CIP-51 8051 MCU designed for the sub 1 GHz ISM frequency bands. This chip is optimized for battery powered applications with operating voltages from 1.8 to 3.6 V and ultra-low current consumption with a standby current of less than 10 nA. The high power amplifier can supply up to +10 dBm output power with 19.5 dB of programmable range. Moreover, the SoC transmitter includes a patented antenna tuning circuit that automatically fine tunes the resonance frequency and impedance matching between the PA output and the connected antenna for optimum transmit efficiency and low harmonic content. FSK and OOK modulation is supported with symbol rates up to 100 kbps. Like all wireless devices, users are responsible for complying with applicable local regulatory requirements for radio transmissions.

The embedded CIP-51 8051 MCU provides the core functionality of the Si4010. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings. A space of 8 kB of on-chip one-time programmable NVM memory is available to store the user program and can also store unique transmit IDs. In case of power outages due to battery removal, 128 bits of EEPROM is available for counter or other operations providing non-volatile storage capability. A library of useful software functions such as AES encryption, a patented 32-bit counter providing 1 M cycles of read/write endurance, and many other functions are included in the 12 kB of ROM to reduce user design time and code space. General purpose input/output pins with push button wake-on touch capability, a programmable system clock, and ultra low power timers are also available to further reduce current consumption.

The Si4010 includes Silicon Laboratories' 2-wire C2 Debug and Programming interface. This debug logic supports memory inspection, viewing and modification of special function registers (SFR), setting break points, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

The device leverages Silicon Labs' patented and proven crystal-less oscillator technology and offers better than ±150 ppm carrier frequency stability over the temperature range of 0 to + 70 °C and ±250 ppm carrier frequency stability over the industrial range of –40 to + 85 °C without the use of an external crystal or frequency reference. The internal MCU automatically calibrates the on-chip voltage controlled oscillator (LCOSC) which forms the output carrier frequency for process and temperature variations. An external 1-pin crystal oscillator option is available for applications requiring tighter frequency tolerances.

Digital integration reduces the amount of required external components compared to traditional offerings, resulting in a solution that only requires a printed circuit board (PCB) implementation area of approximately 25 by 50 mm (including battery, switches, and 25 mm^2 antenna). The high integration of the Si4010 improves the system manufacturing reliability and quality and minimizes costs. This chip offers industry leading RF performance, high integration, flexibility, low BOM, small board area, and ease of design. No production alignment is necessary as all RF functions are integrated into the device.

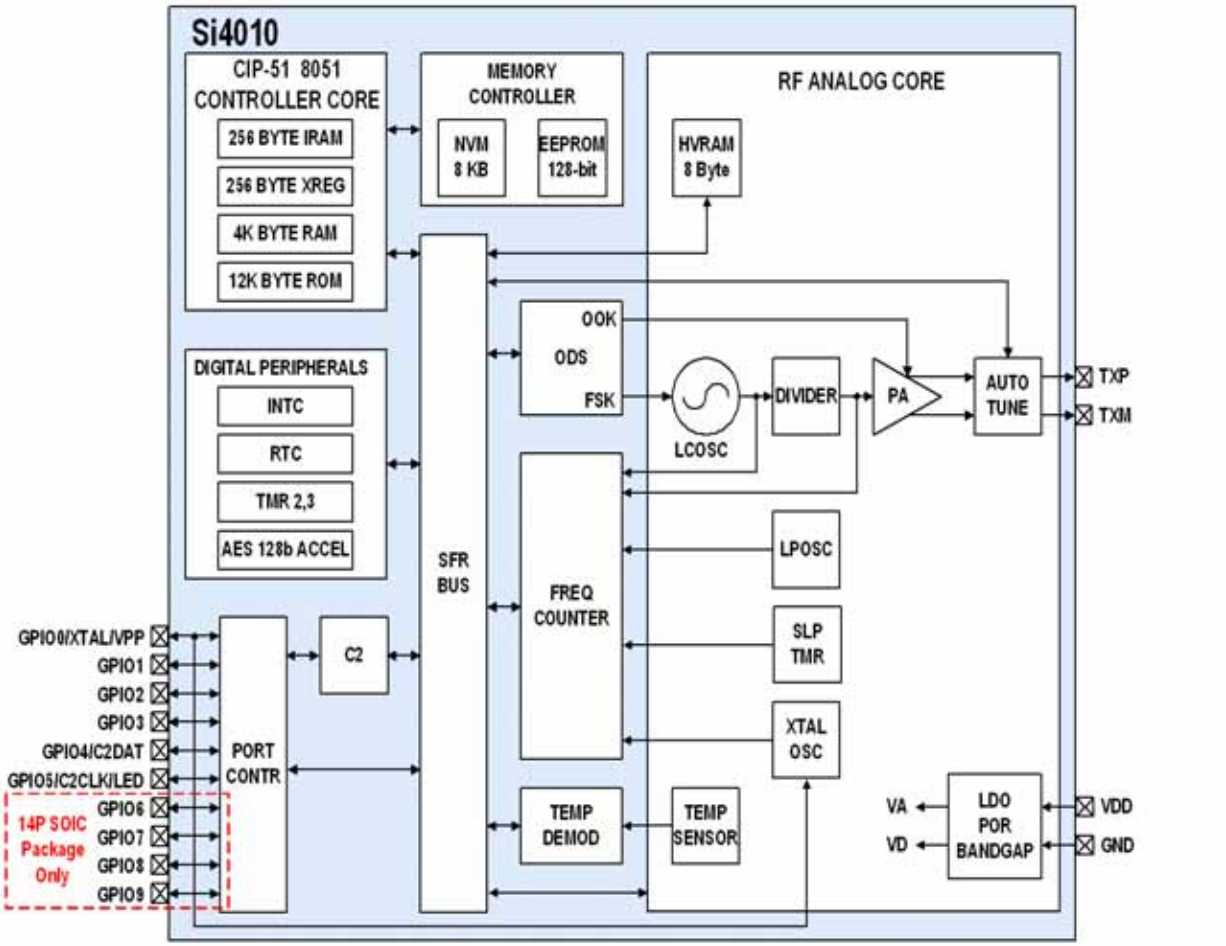


Figure 1.1. Si4010 Block Diagram

2. Test Circuit

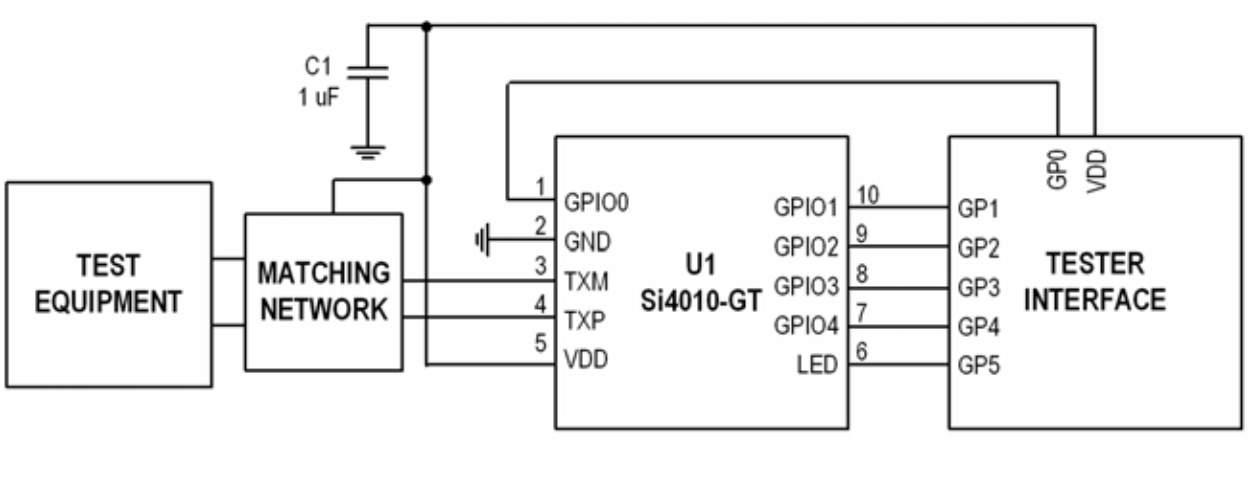


Figure 2.1. Test Block Diagram with 10-Pin MSOP

3. Typical Application Schematic

3.1. Si4010 Used in a 5-Button RKE System with LED Indicator

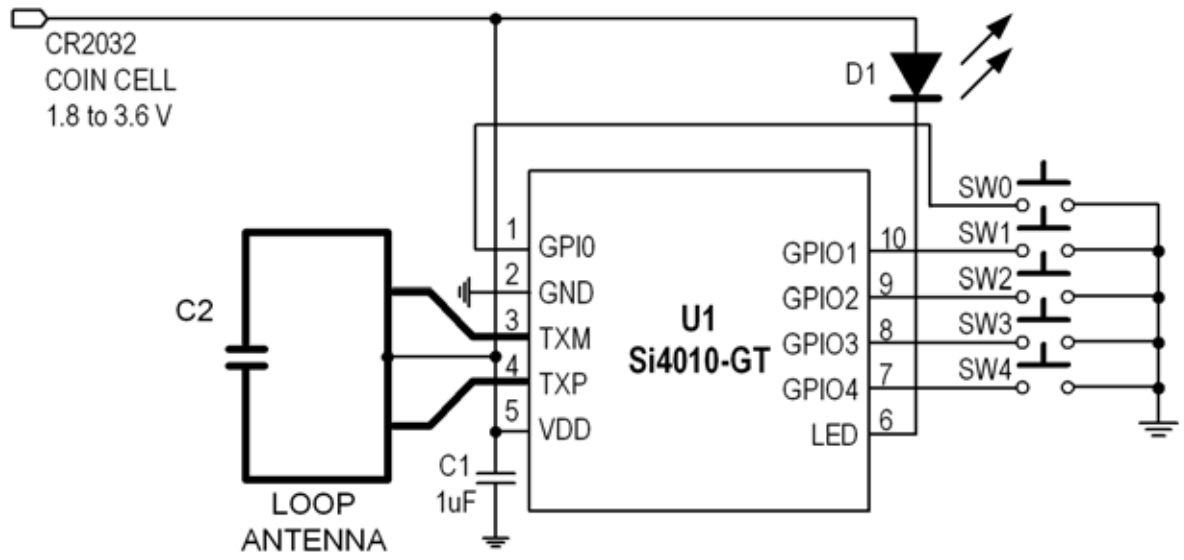


Figure 3.1. Si4010 Used in a 5-button RKE System with LED Indicator

3.2. Si4010 with an External Crystal in a 4-Button RKE System with LED Indicator

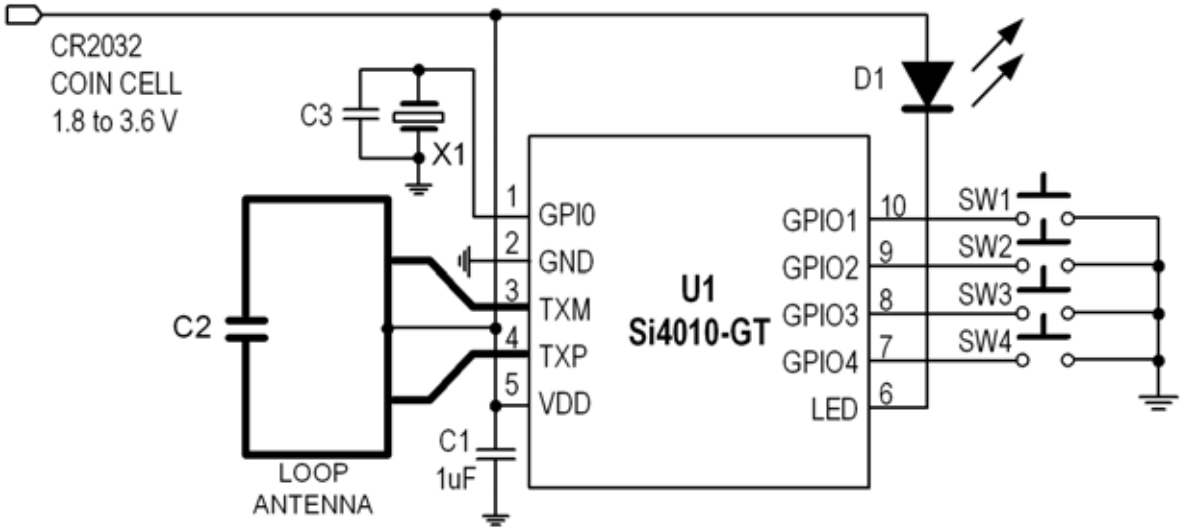


Figure 3.2. Si4010 with an External Crystal in a 4-button RKE System with LED Indicator

4. Ordering Information

Table 4.1. Product Selection Guide

Ordering Part Number[1]	MIPS (Peak)	NVM (OTP) Memory (Bytes)	RAM (Bytes)	Embedded ROM Functions	Internal Data RAM (Bytes)	HVRAM (Bytes)	EEPROM (Bits)	128-Bit AES Accelerator	GPIO with Wakeup[2]	LED Driver	Sleep Timer	+10 dBm RF Transmitter	LDO with POR Circuit	Low Battery Detector	Automotive Qualified[3]	Lead-free (RoHS Compliant)	Package
Si4010-C2-GT	24	8k	4k	Y	256	8	128	Y	**5**	1	Y	Y	Y	Y	—	Y	MSOP-10
Si4010-C2-GS	24	8k	4k	Y	256	8	128	Y	**9**	1	Y	Y	Y	Y	—	Y	SOIC-14
Si4010-C2-AT	24	8k	4k	Y	256	8	128	Y	**5**	1	Y	Y	Y	Y	**Y**	Y	MSOP-10
Si4010-C2-AS	24	8k	4k	Y	256	8	128	Y	**9**	1	Y	Y	Y	Y	**Y**	Y	SOIC-14

Notes:
1. Add an “(R)” at the end of the device part number to denote tape and reel option.
2. Assumes LED driver is used and no external crystal.
3. AEC Q100 qualification is pending.

5. Top Markings

5.1. SOIC

Figure 1. Si4010 Top Marking

Table 1. Top Marking Explanation

Line	Characters	Description
Line 1	Circle = 1.1 mm Diameter Left-Justified	"e3" Pb-Free Symbol
	Customer Part Number	Si4010C2
Line 2	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date.
	TTTTTT = Trace Code	Manufacturing code characters from the Markings section of the Assembly Purchase Order form.

5.2. MSOP

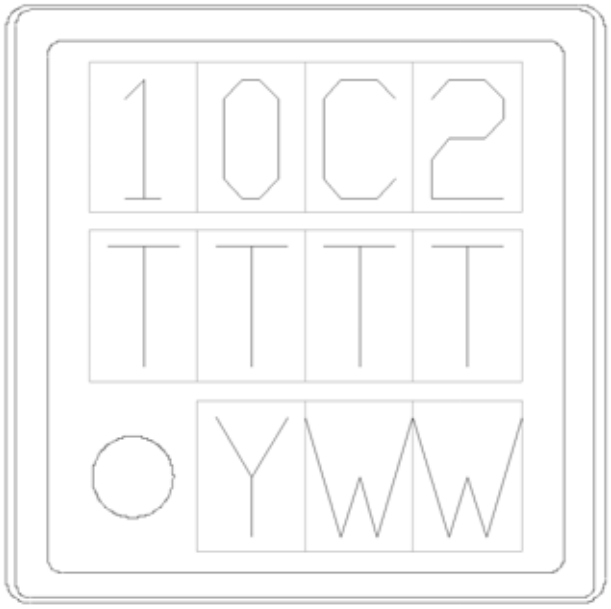


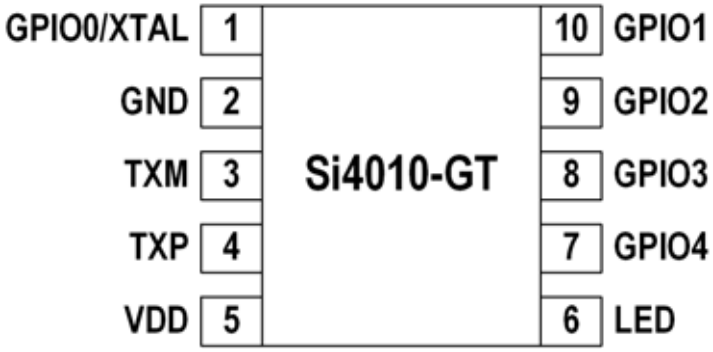
Figure 2. Si4010 Top Marking

Table 2. Top Marking Explanation

Line	Characters	Description
Line 1	Device Part Number	10C2
Line 2	TTTT = Trace Code	Line 2 from the "Markings" section of the Assembly Purchase Order form.
Line 3	YWW = Date Code	Date Code assigned by the assembly house. Y = Last Digit of Current Year (Ex: 2008 = 8) WW = Work Week of Mold Date.

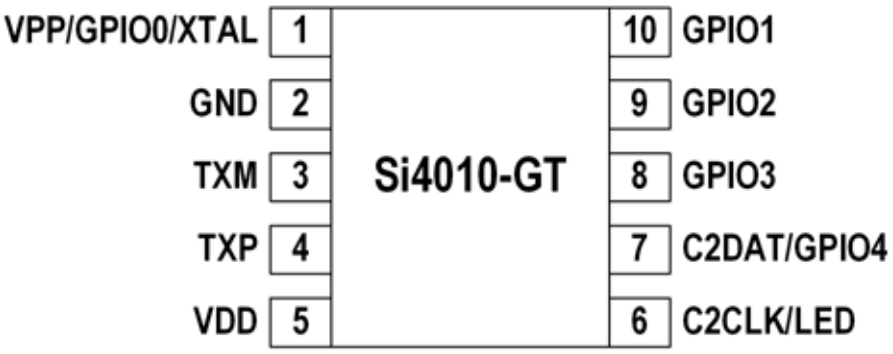
6. Pin Definitions

6.1. MSOP, Application



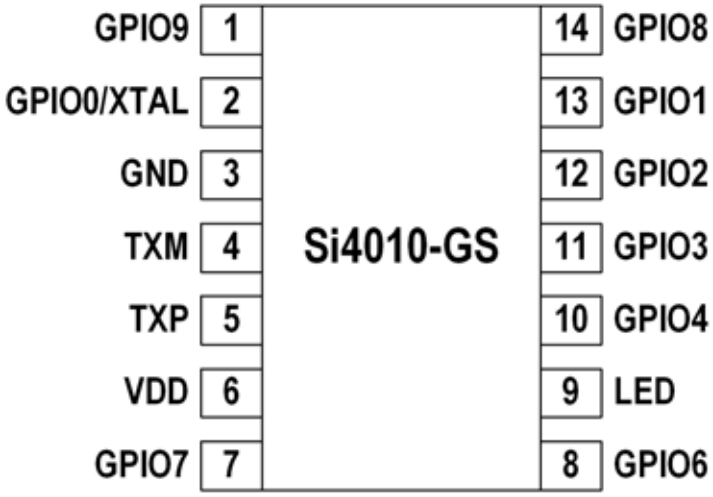
Pin Number(s)	Name	Description
1	GPIO0/XTAL	General purpose input pin. Can be configured as an input pin for a crystal.
2	GND	Ground. Connect to ground plane on PCB.
3, 4	TXM, TXP	Transmitter differential outputs.
5	VDD	Power.
6	LED	Dedicated LED driver.
7, 8, 9, 10	GPIO[4:1]	General purpose input/output pins.

6.2. MSOP, Programming/Debug Mode



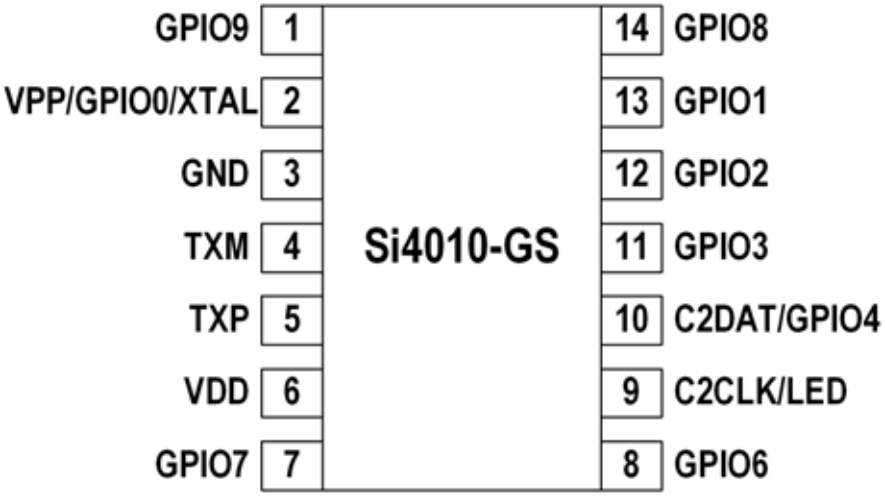
Pin Number(s)	Name	Description
1	VPP	+6.5 V required for NVM (OTP) Memory programming.
2	GND	Ground. Connect to ground plane on PCB.
3	TXM	Transmitter differential output.
4	TXP	Transmitter differential output.
5	VDD	Power.
6	C2CLK	C2 clock interface.
7	C2DAT	C2 data input/output pin.
8, 9, 10	GPIO[3:1]	General purpose input/output pins.

6.3. SOIC Package, Application



Pin Number(s)	Name	Description
1	GPIO9	General purpose input/output pin
2	GPIO0/XTAL	General purpose input pin. Can be configured as an input pin for a crystal
3	GND	Ground. Connect to ground plane on PCB
4,5	TXM, TXP	Transmitter differential outputs
6	VDD	Power
7,8	GPIO[7:6]	General purpose input/output pins
9	LED	Dedicated LED driver
10,11,12,13	GPIO[4:1]	General purpose input/output pins
14	GPIO8	General purpose input/output pin

6.4. SOIC Package, Programming/debug Mode



Pin Number(s)	Name	Description
1	GPIO9	General purpose input/output pin
2	VPP	+6.5 V required for NVM (OTP) Memory programming
3	GND	Ground. Connect to ground plane on PCB
4,5	TXM, TXP	Transmitter differential outputs
6	VDD	Power
7,8	GPIO[7:6]	General purpose input/output pins
9	C2CLK	C2 clock interface
10	C2DAT	C2 data input/output pin
11,12,13	GPIO[4:1]	General purpose input/output pins
14	GPIO8	General purpose input/output pin

7. Package Specifications

7.1. 10-Pin MSOP

Figure 7.1 illustrates the package details for the Si4010, 10-pin MSOP package. Table 7.1 lists the values for the dimensions shown in the illustration.

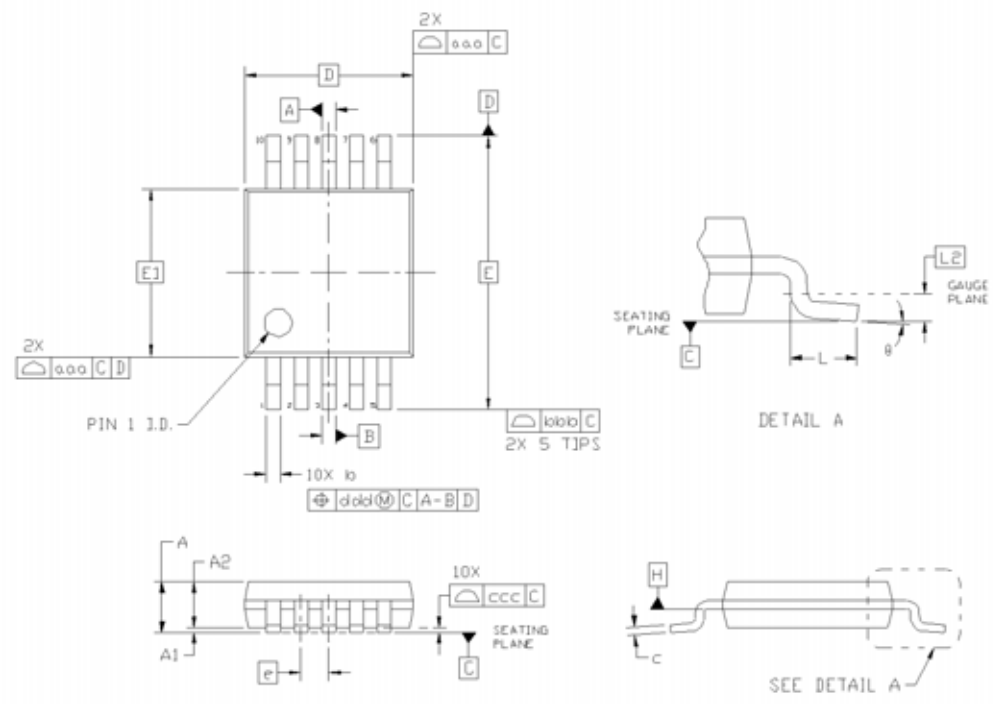


Figure 7.1. 10-Pin MSOP Package

Table 7.1. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		

Symbol	Millimeters		
	Min	Nom	Max
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0°	—	8°
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions are shown in millimeters (mm).
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-187, Variation “BA.”
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2. 14-pin SOIC Package

Figure 7.2 illustrates the package details for the Si4010, 14-pin SOIC package. Table 7.2 lists the values for the dimensions shown in the illustration.

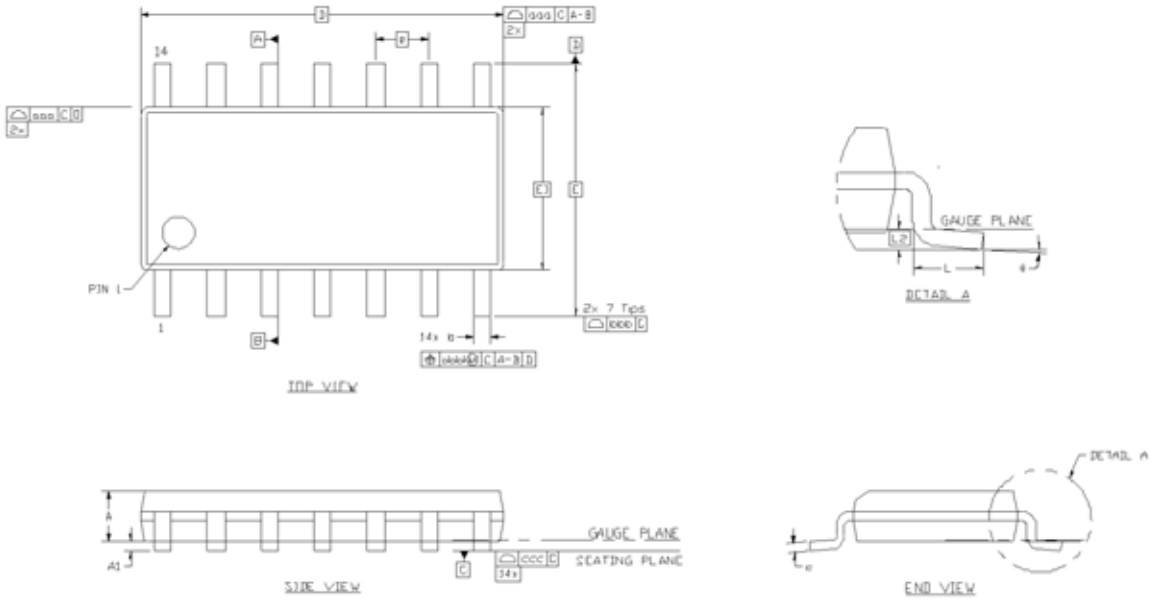


Figure 7.2. 14-Pin SOIC Package

Table 7.2. Package Dimensions

Symbol	Min	Max
A	—	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.17	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	

Symbol	Min	Max
L	0.40	1.27
L2	0.25 BSC	
Q	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions are shown in millimeters (mm).
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS012, variation AB."
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern 10-Pin MSOP

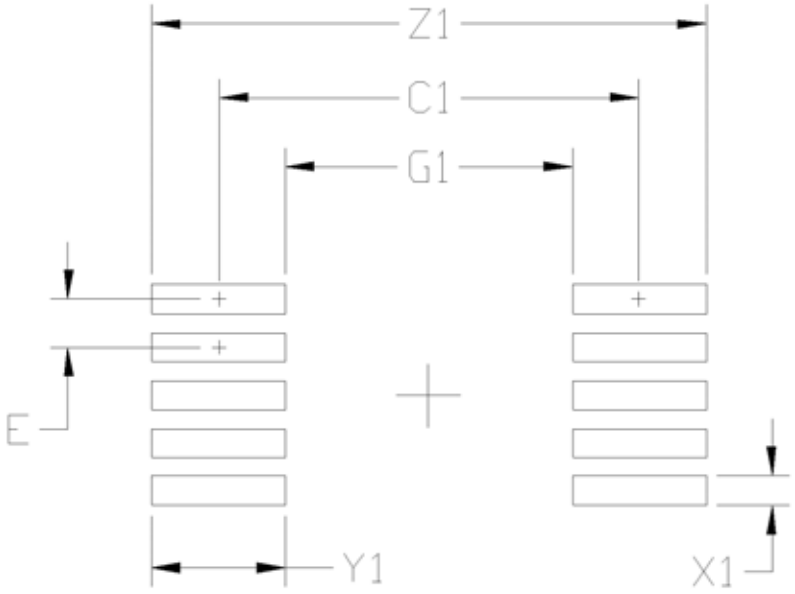


Figure 8.1. 10-Pin MSOP Recommended PCB Land Pattern

Table 8.1. 10-Pin MSOP Dimensions

Dimension	MIN	MAX
C1	4.40 REF	
E	0.50 BSC	
G1	3.00	—
X1	—	0.30
Y1	1.40 REF	
Z1	—	5.80

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.