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Si4136/Si4126

ISM RF Synthesizer With Integrated VCOs For Wireless Communications

Features

- Dual-band RF synthesizers
  - RF1: 2300 MHz to 2500 MHz
  - RF2: 2025 MHz to 2300 MHz
- IF synthesizer
  - 62.5 MHz to 1000 MHz
- Integrated VCOs, loop filters, varactors, and resonators
- Minimal external components required
- Low phase noise
- 5 µA standby current
- 25.7 mA typical supply current
- 2.7 V to 3.6 V operation
- Packages: 24-pin TSSOP, 28-lead QFN
  - Lead-free/RoHS-compliant options available

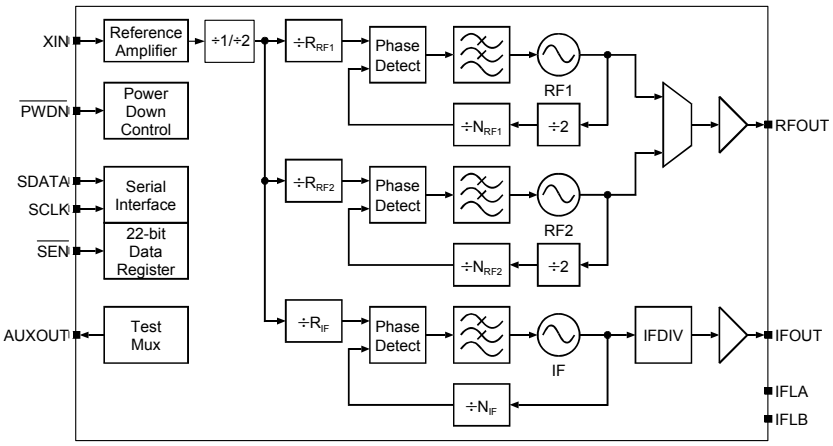
Applications

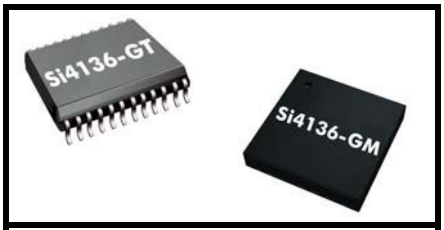
- ISM and MMDS band communications
- Wireless LAN and WAN
- Dual-band communications

Description

The Si4136 is a monolithic integrated circuit that performs both IF and RF synthesis for wireless communications applications. The Si4136 includes three VCOs, loop filters, reference and VCO dividers, and phase detectors. Divider and powerdown settings are programmable through a three-wire serial interface.

Functional Block Diagram



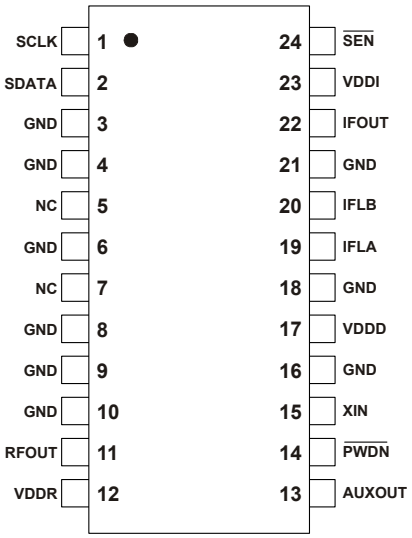


Ordering Information:

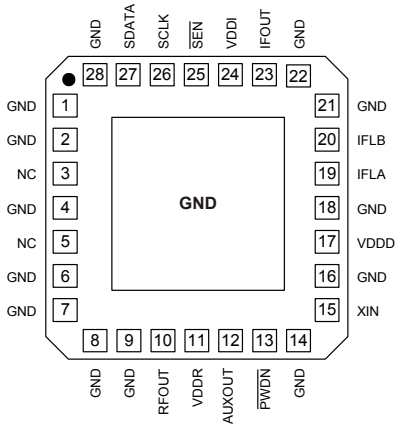
See page 29.

Pin Assignments

Si4136-GT



Si4136-GM



Patents pending

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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Supply Voltages Difference	V_Δ	($V_{DDR} – V_{DDD}$), ($V_{DDI} – V_{DDD}$)	–0.3	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 4.0	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	–55 to 150	°C

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **This device is a high performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDATA, $\overline{SEN}$, $\overline{PWDN}$, and XIN.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Supply Current[1]		RF1 and IF operating	—	25.7	31	mA
RF1 Mode Supply Current[1]			—	15.7	19	mA
RF2 Mode Supply Current[1]			—	15	18	mA
IF Mode Supply Current[1]			—	10	12	mA
Standby Current		$\overline{PWDN}$ = 0	—	1	—	µA
High Level Input Voltage[2]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[2]	I_{IH}	V_{IH} = 3.6 V, V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD} = 3.6 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OH} = 500 µA	—	—	0.4	V

Notes:
1. RF1 = 2.4 GHz, RF2 = 2.1 GHz, IFOUT = 800 MHz, LPWR = 0.
2. For signals SCLK, SDATA, $\overline{SEN}$, and $\overline{PWDN}$.
3. For signal AUXOUT.

Table 4. Serial Interface Timing
(V_{DD} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 1	40	—	—	ns
SCLK Rise Time	t_r	Figure 1	—	—	50	ns
SCLK Fall Time	t_f	Figure 1	—	—	50	ns
SCLK High Time	t_h	Figure 1	10	—	—	ns
SCLK Low Time	t_l	Figure 1	10	—	—	ns
SDATA Setup Time to SCLK↑[2]	t_{su}	Figure 2	5	—	—	ns
SDATA Hold Time from SCLK↑[2]	t_{hold}	Figure 2	0	—	—	ns
$\overline{SEN}$↓ to SCLK↑ Delay Time[2]	t_{en1}	Figure 2	10	—	—	ns
SCLK↑ to $\overline{SEN}$↑ Delay Time[2]	t_{en2}	Figure 2	12	—	—	ns
$\overline{SEN}$↑ to SCLK↑ Delay Time[2]	t_{en3}	Figure 2	12	—	—	ns
$\overline{SEN}$ Pulse Width	t_w	Figure 2	10	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of the waveform. See Figure 2.

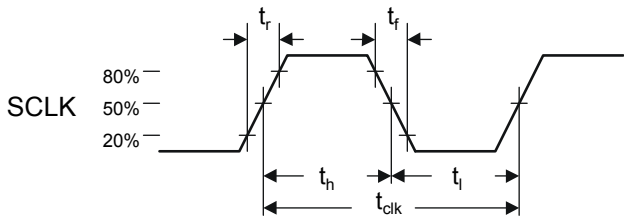


Figure 1. SCLK Timing Diagram

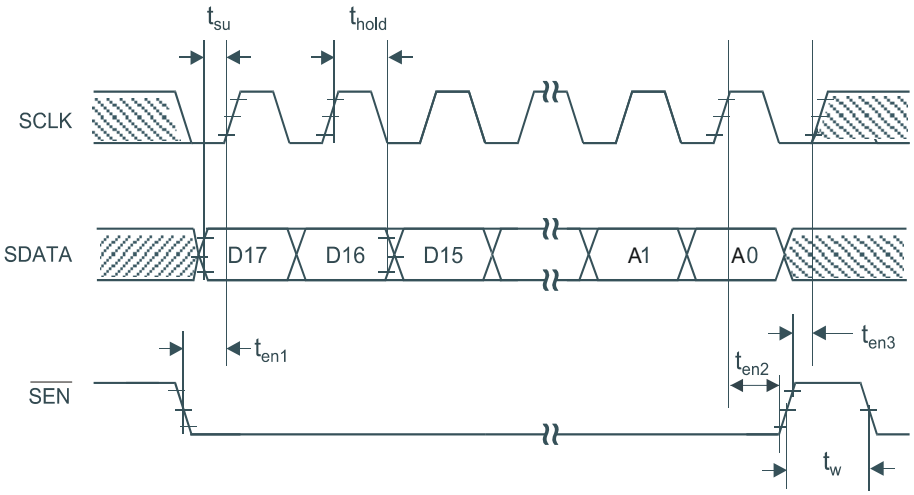


Figure 2. Serial Interface Timing Diagram

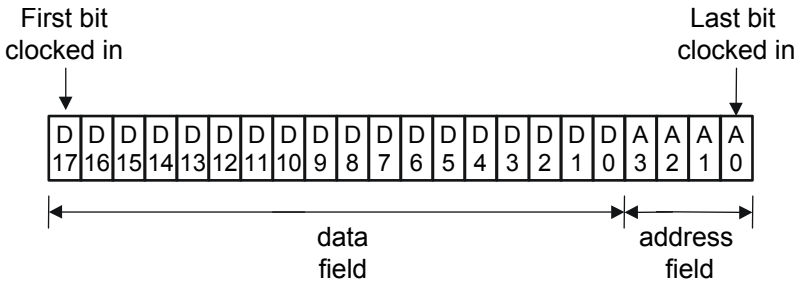


Figure 3. Serial Word Format

Table 5. RF and IF Synthesizer Characteristics

(V_{DD} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}	XINDIV2 = 0	2	—	25	MHz
XIN Input Frequency	f_{REF}	XINDIV2 = 1	25	—	50	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	V_{DD} +0.3 V	V_{PP}
Phase Detector Update Frequency	f_ϕ	$f_\phi = f_{REF}/R$ for XINDIV2 = 0 $f_\phi = f_{REF}/2R$ for XINDIV2 = 1	0.010	—	1.0	MHz
RF1 VCO Tuning Range[2]			2300	—	2500	MHz
RF2 VCO Tuning Range[2]			2025	—	2300	MHz
IF VCO Center Frequency Range	f_{CEN}		526	—	952	MHz
IFOUT Tuning Range from f_{CEN}		with IFDIV	62.5	—	1000	MHz
IFOUT VCO Tuning Range from f_{CEN}		Note: L ±10%	–5	—	5	%
RF1 VCO Pushing		Open loop	—	0.75	—	MHz/V
RF2 VCO Pushing			—	0.65	—	MHz/V
IF VCO Pushing			—	0.10	—	MHz/V
RF1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	0.250	—	MHz p-p
RF2 VCO Pulling			—	0.100	—	MHz p-p
IF VCO Pulling			—	0.025	—	MHz p-p
RF1 Phase Noise		1 MHz offset	—	–130	—	dBc/Hz
RF1 Integrated Phase Error		100 Hz to 100 kHz	—	1.2	—	degrees rms
RF2 Phase Noise		1 MHz offset	—	–131	—	dBc/Hz
RF2 Integrated Phase Error		100 Hz to 100 kHz	—	1.0	—	degrees rms
IF Phase Noise at 800 MHz		100 kHz offset	—	–104	—	dBc/Hz
IF Integrated Phase Error		100 Hz to 100 kHz	—	0.4	—	degrees rms

Notes:

1. f_ϕ(RF) = 1 MHz, f_ϕ(IF) = 1 MHz, RF1 = 2.4 GHz, RF2 = 2.1 GHz, IFOUT = 800 MHz, LPWR = 0, for all parameters unless otherwise noted.
2. RF VCO tuning range limits are fixed by inductance of internally bonded wires.
3. From powerup request ($\overline{PWDN}\uparrow$ or $\overline{SEN}\uparrow$ during a write of 1 to bits PDIB and PDRB in Register 2) to RF and IF synthesizers ready (settled to within 0.1 ppm frequency error).
4. From powerdown request ($\overline{PWDN}\downarrow$, or $\overline{SEN}\uparrow$ during a write of 0 to bits PDIB and PDRB in Register 2) to supply current equal to I_{PWDN}.

Table 5. RF and IF Synthesizer Characteristics (Continued)
(V_{DD} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 Harmonic Suppression		Second Harmonic	—	–28	–20	dBc
RF2 Harmonic Suppression			—	–23	–20	dBc
IF Harmonic Suppression			—	–26	–20	dBc
RFOUT Power Level		Z_L = 50 Ω, RF1 active	–7	–3.5	–0.5	dBm
RFOUT Power Level		Z_L = 50 Ω, RF2 active	–7	–3.5	–0.5	dBm
IFOUT Power Level		Z_L = 50 Ω	–7	–4	0	dBm
RF1 Output Reference Spurs		Offset = 1 MHz	—	–63	—	dBc
		Offset = 2 MHz	—	–68	—	dBc
		Offset = 3 MHz	—	–70	—	dBc
RF2 Output Reference Spurs		Offset = 1 MHz	—	–63	—	dBc
		Offset = 2 MHz	—	–68	—	dBc
		Offset = 3 MHz	—	–70	—	dBc
Powerup Request to Synthesizer Ready[3] Time	t_{pup}	Figures 4, 5 f_ϕ > 500 kHz	—	80	100	µs
Powerup Request to Synthesizer Ready[3] Time	t_{pup}	Figures 4, 5 $f_\phi \leq$ 500 kHz	—	$40/f_\phi$	$50/f_\phi$	
Powerdown Request to Synthesizer OffTime[4]	t_{pdn}	Figures 4, 5	—	—	100	ns

Notes:
1. f_ϕ(RF) = 1 MHz, f_ϕ(IF) = 1 MHz, RF1 = 2.4 GHz, RF2 = 2.1 GHz, IFOUT = 800 MHz, LPWR = 0, for all parameters unless otherwise noted.
2. RF VCO tuning range limits are fixed by inductance of internally bonded wires.
3. From powerup request ($\overline{PWDN}\uparrow$ or $\overline{SEN}\uparrow$ during a write of 1 to bits PDIB and PDRB in Register 2) to RF and IF synthesizers ready (settled to within 0.1 ppm frequency error).
4. From powerdown request ($\overline{PWDN}\downarrow$, or $\overline{SEN}\uparrow$ during a write of 0 to bits PDIB and PDRB in Register 2) to supply current equal to I_{PWDN}.

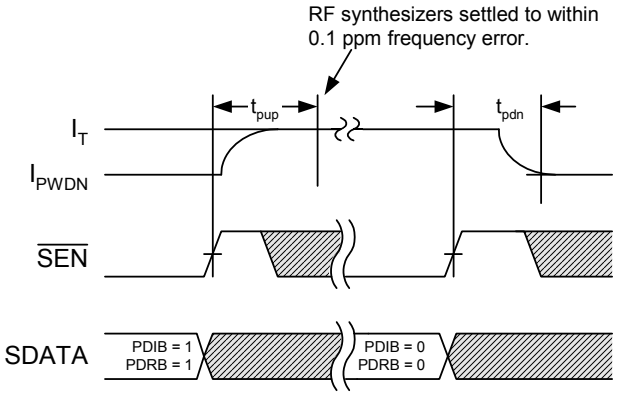


Figure 4. Software Power Management Timing Diagram

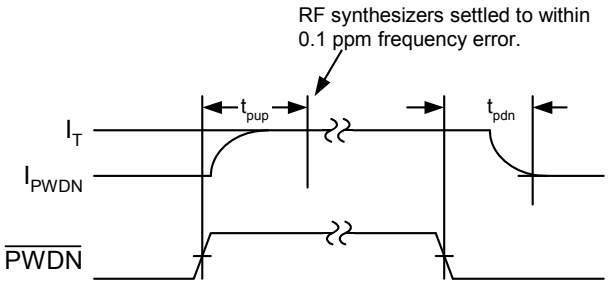


Figure 5. Hardware Power Management Timing Diagram

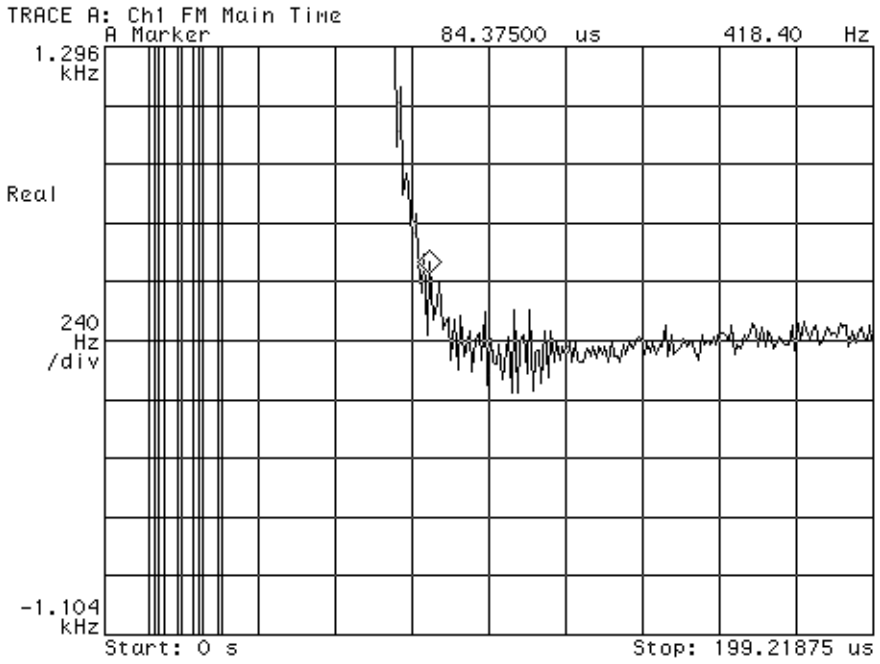
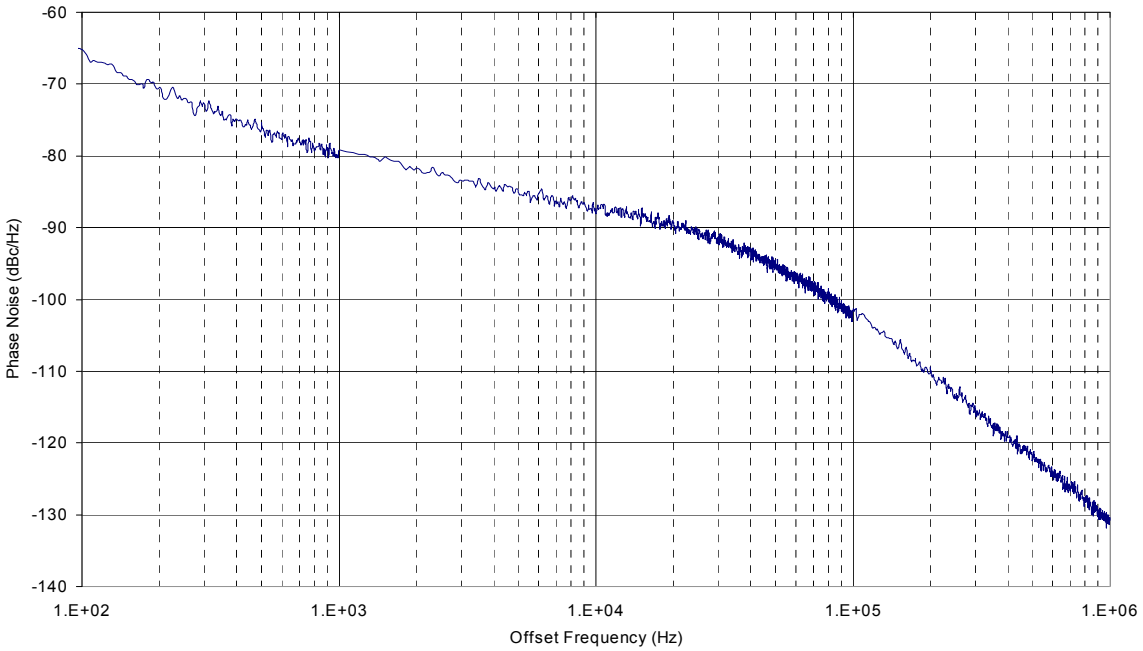


Figure 6. Typical Transient Response RF1 at 2.4 GHz with 1 MHz Phase Detector Update Frequency



Typical RF1 Phase Noise at 2.4 GHz

Figure 7. Typical RF1 Phase Noise at 2.4 GHz with 1 MHz Phase Detector Update Frequency

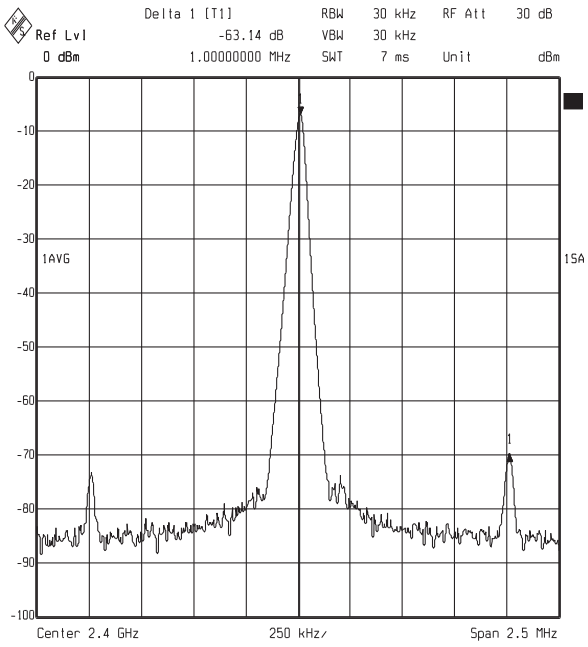
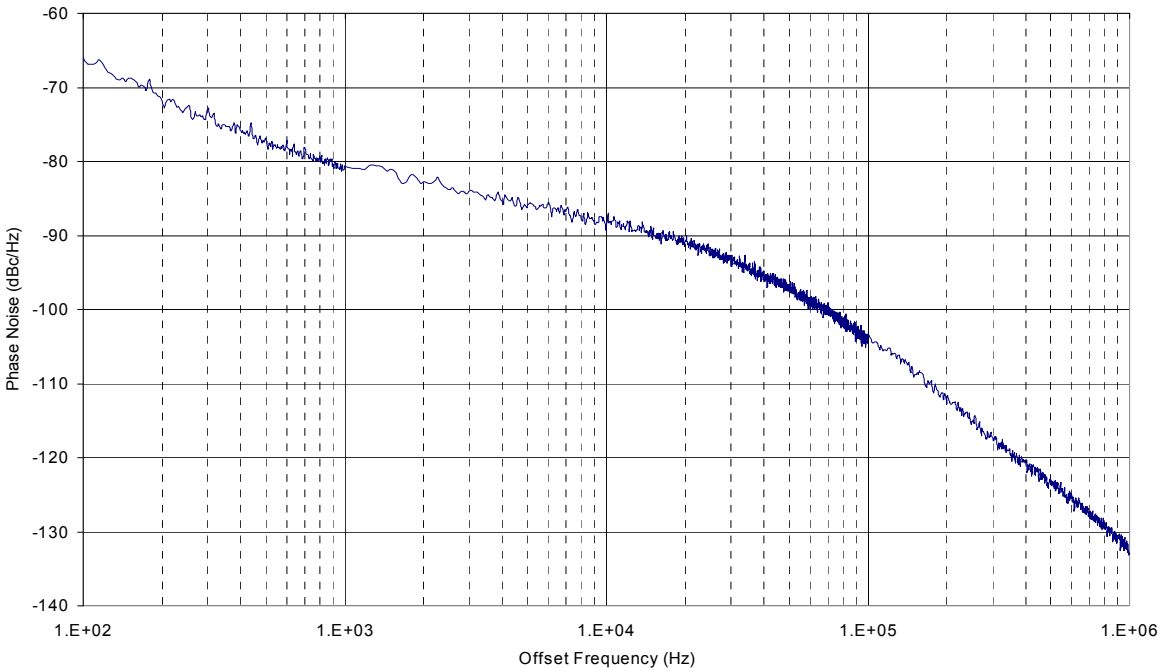


Figure 8. Typical RF1 Spurious Response at 2.4 GHz with 1 MHz Phase Detector Update Frequency

s



Typical RF2 Phase Noise at 2.1 GHz

Figure 9. Typical RF2 Phase Noise at 2.1 GHz with 1 MHz Phase Detector Update Frequency

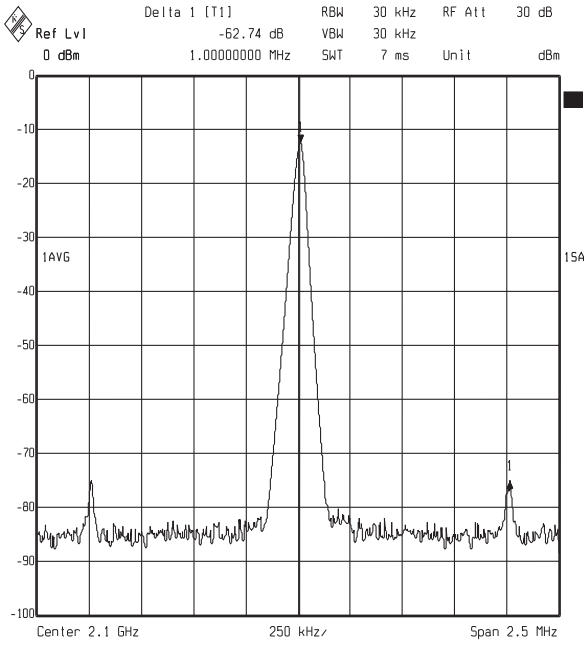
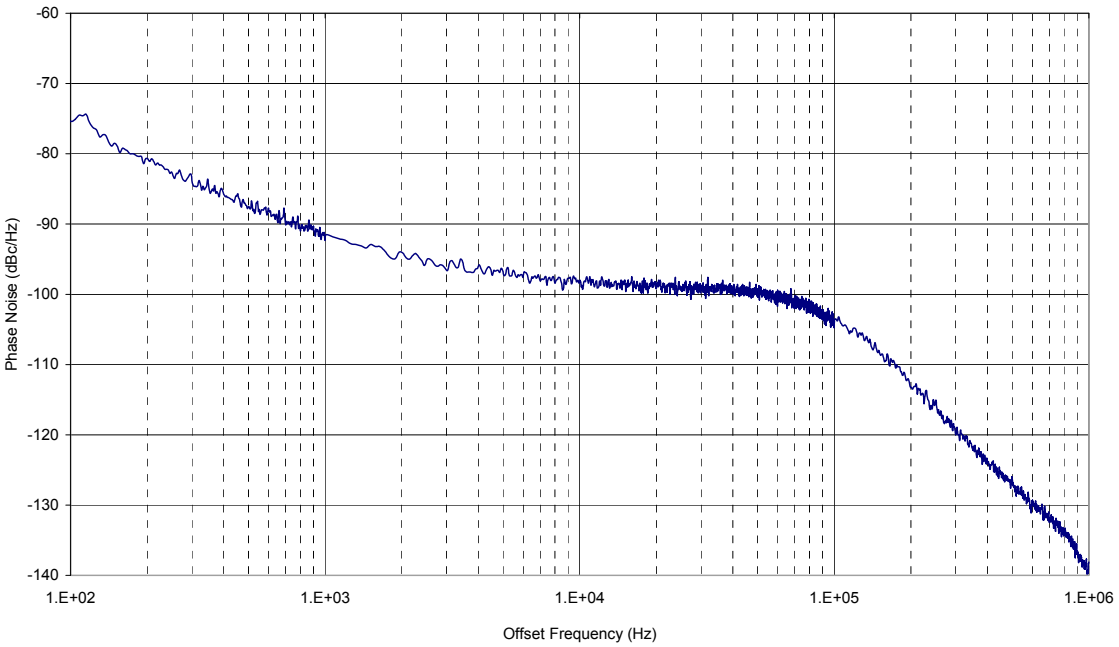


Figure 10. Typical RF2 Spurious Response at 2.1 GHz with 1 MHz Phase Detector Update Frequency



Typical IF Phase Noise at 800 MHz

Figure 11. Typical IF Phase Noise at 800 MHz with 1 MHz Phase Detector Update Frequency

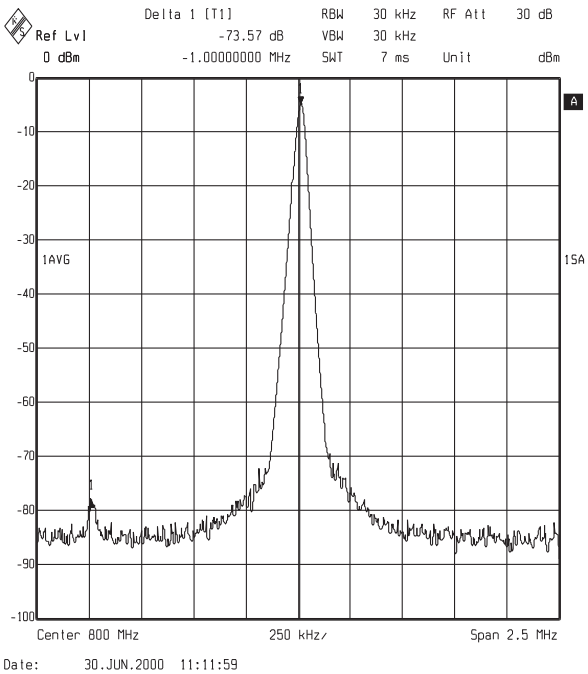
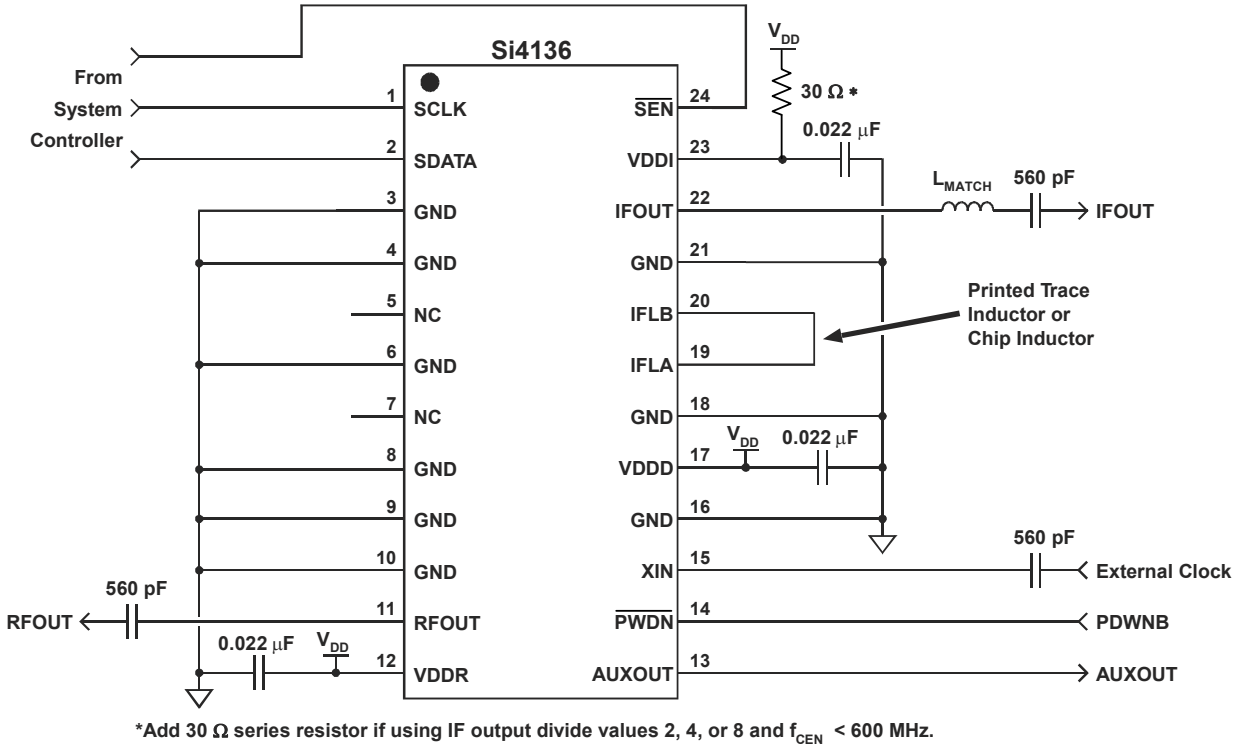


Figure 12. IF Spurious Response at 800 MHz with 1 MHz Phase Detector Update Frequency



*Add 30 Ω series resistor if using IF output divide values 2, 4, or 8 and f_{CEN} < 600 MHz.

Figure 13. Typical Application Circuit: Si4136-GT

2. Functional Description

The Si4136 is a monolithic integrated circuit that performs IF and dual-band RF synthesis for many wireless communications applications. This integrated circuit (IC), along with a minimum number of external components, is all that is necessary to implement the frequency synthesis function in applications like W-LAN using the IEEE 802.11 standard.

The Si4136 has three complete phase-locked loops (PLLs), with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4136 suitable for use in demanding wireless communications applications. Also integrated are phase detectors, loop filters, and reference and output frequency dividers. The IC is programmed through a three-wire serial interface.

Two PLLs are provided for RF synthesis. These RF PLLs are multiplexed so that only one PLL is active at a given time (as determined by the setting of an internal register). The active PLL is the last one written. The center frequency of the VCO in each PLL is set by the internal bond wire inductance within the package. Inaccuracies in these inductances are compensated for by the self-tuning algorithm. The algorithm is run following power-up or following a change in the programmed output frequency.

The RF PLLs contain a divide-by-2 circuit before the N-divider. As a result, the phase detector frequency ($f\phi$) is equal to half the desired channel spacing. For example, for a 200 kHz channel spacing, $f\phi$ would equal 100 kHz. The IF PLL does not contain the divide-by-2 circuit before the N-divider. In this case, $f\phi$ is equal to the desired channel spacing. Each RF VCO is optimized for a particular frequency range. The RF1 VCO is optimized to operate from 2.3 GHz to 2.5 GHz, while the RF2 VCO is optimized to operate between 2.025 GHz and 2.3 GHz.

One PLL is provided for IF synthesis. The center frequency of this circuit's VCO is set by an external inductance. The PLL can adjust the IF output frequency by ±5% of the VCO center frequency. Inaccuracies in the value of the external inductance are compensated for by the Si4136's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered-up (by either the $\overline{\text{PWDN}}$ pin or by software) and/or each time a new output frequency is programmed. The IF VCO can have its center frequency set as low as 526 MHz and as high as 952 MHz. An IF output divider is provided to divide down the IF output frequencies, if needed. The divider is programmable, capable of dividing by 1, 2, 4, or 8.

In order to accommodate designs running at XIN frequencies greater than 25 MHz, the Si4136 includes a programmable divide-by-2 option (XINDIV2 in Register 0, D6) on the XIN input. By enabling this option, the Si4136 can accept a range of TCXO frequencies from 25 MHz to 50 MHz. This feature makes the Si4136 ideal for W-LAN radio designs operating at an XIN of 44 MHz.

The unique PLL architecture used in the Si4136 produces settling (lock) times that are comparable in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

2.1. Serial Interface

A timing diagram for the serial interface is shown in Figure 2 on page 7. Figure 3 on page 7 shows the format of the serial word.

The Si4136 is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when $\overline{\text{SEN}}$ is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of $\overline{\text{SEN}}$ into the internal data register addressed in the address field. The serial interface is disabled when $\overline{\text{SEN}}$ is high.

Table 11 on page 21 summarizes the data register functions and addresses. It is not necessary (although it is permissible) to clock into the internal shift register any leading bits that are "don't cares."

2.2. Setting the IF VCO Center Frequencies

The IF PLL can adjust its output frequency ±5% from the center frequency as established by the value of an external inductance connected to the VCO. The RF1 and RF2 PLLs have fixed operating ranges due to the inductance set by the internal bond wires. Each center frequency is established by the value of the total inductance (internal and/or external) connected to the respective VCO. Manufacturing tolerance of ±10% for the external inductor is acceptable for the IF VCO. The Si4136 will compensate for inaccuracies by executing a self-tuning algorithm following PLL power-up or following a change in the programmed output frequency.

Because the total tank inductance is in the low nH range, the inductance of the package needs to be considered in determining the correct external inductance. The total inductance (L_{TOT}) presented to the IF VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). The IF VCO has a nominal capacitance (C_{NOM}) in parallel with the total inductance, and the center frequency is as follows:

$$f_{CEN} = \frac{1}{2\pi\sqrt{L_{TOT} \cdot C_{NOM}}} = \frac{1}{2\pi\sqrt{(L_{PKG} + L_{EXT}) \cdot C_{NOM}}}$$

Table 6 summarizes the characteristics of the IF VCO.

Table 6. Si4136-GT VCO Characteristics

VCO	Fcen Range (MHz)		Cnom (pF)	Lpkg (nH)	Lext Range (nH)	
	Min	Max			Min	Max
IF	526	952	6.5	2.1	2.2	12.0

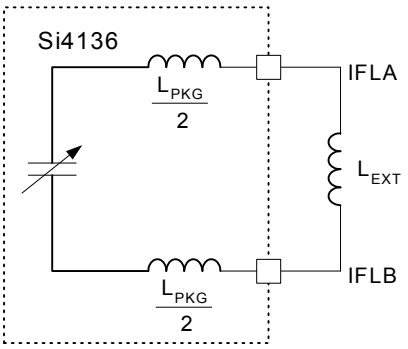


Figure 14. Example of IF External Inductor

As a design example, suppose synthesizing frequencies in a 30 MHz band between 735 MHz and 765 MHz is desired. The center frequency should be defined as midway between the two extremes, or 750 MHz. The PLL will be able to adjust the VCO output frequency ±5% of the center frequency, or ±37.5 MHz of 750 MHz (i.e., from approximately 713 MHz to 788 MHz). The IF VCO has a C_{NOM} of 6.5 pF, and a 6.9 nH inductance (correct to two digits) in parallel with this capacitance will yield the desired center frequency. An external inductance of 4.8 nH should be connected between IFLA and IFLB, as shown in Figure 14. This, in addition to 2.1 nH of package inductance, will present the correct total inductance to the VCO. In manufacturing, the external inductance can vary ±10% of its nominal value and the Si4136 will correct for the variation with the self-tuning algorithm.

For more information on designing the external trace inductor, please refer to Application Note 31.

2.3. Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following power-up of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the desired output frequency. In so doing, the algorithm will compensate for manufacturing tolerance errors in the value of the external inductance connected to the IF VCO. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the PLL controls the VCO oscillation frequency. The PLL will complete frequency locking, eliminating any remaining frequency error. Thereafter, it will maintain frequency-lock, compensating for effects caused by temperature and supply voltage variations.

The Si4136's self-tuning algorithm will compensate for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur *after* self-tuning is limited. For external inductances with temperature coefficients around ±150 ppm/°C, the PLL will be able to maintain lock for changes in temperature of approximately ±30°C.

Applications where the PLL is regularly powered-down or the frequency is periodically reprogrammed minimize or eliminate the potential effects of temperature drift because the VCO is re-tuned in either case. In applications where the ambient temperature can drift substantially after self-tuning, it may be necessary to monitor the lock-detect bar (LDETB) signal on the AUXOUT pin to determine whether a PLL is about to run out of locking capability. (See "2.9. Auxiliary Output (AUXOUT)" for how to select LDETB.) The LDETB signal will be low after self-tuning has completed but will rise when either the IF or RF PLL nears the limit of its compensation range. (LDETB will also be high when either PLL is executing the self-tuning algorithm.) The output frequency will still be locked when LDETB goes high, but the PLL will eventually lose lock if the temperature continues to drift in the same direction. Therefore, if LDETB goes high both the IF and RF PLLs should promptly be re-tuned by initiating the self-tuning algorithm.

2.4. Output Frequencies

The IF and RF output frequencies are set by programming the R- and N-Divider registers. Each PLL has its own R and N registers so that each can be

programmed independently. Programming either the R- or N-Divider register for RF1 or RF2 automatically selects the associated output.

When XINDIV2 = 0, the reference frequency on the XIN pin is divided by R and this signal is the input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by 2N for the RF PLLs or N for the IF PLL. After an initial transient

Equation 1. $f_{OUT} = (2N/R) \bullet f_{REF}$ (for the RF PLLs)

Equation 2. $f_{OUT} = (N/R) \bullet f_{REF}$ (for the IF PLL).

The integers R are set by programming the RF1 R-Divider register (Register 6), the RF2 R-Divider register (Register 7) and the IF R-Divider register (Register 8).

The integers N are set by programming the RF1 N-Divider register (register 3), the RF2 N-Divider register (Register 4), and the IF N-Divider register (Register 5).

If the optional divide-by-2 circuit on the XIN pin is enabled (XINDIV2 = 1) then after an initial transient

$f_{OUT} = (N/R) \bullet f_{REF}$ (for the RF PLLs)

$f_{OUT} = (N/2R) \bullet f_{REF}$ (for the IF PLL).

Each N-Divider is implemented as a conventional high speed divider. That is, it consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter. However, the control of these sub-circuits is handled automatically. Only the appropriate N value should be programmed.

2.5. PLL Loop Dynamics

The transient response for each PLL is determined by its phase detector update rate f_ϕ (equal to f_{REF}/R) and the phase detector gain programmed for each RF1, RF2, or IF synthesizer. (See Register 1.) Four different settings for the phase detector gain are available for each PLL. The highest gain is programmed by setting the two phase detector gain bits to 00, and the lowest by setting the bits to 11. The values of the available gains, relative to the highest gain, are listed in Table 7.

Table 7. Gain Values (Register 1)

K_P Bits	Relative P.D. Gain
00	1
01	1/2
10	1/4
11	1/8

In general, a higher phase detector gain will decrease in-band phase noise and increase the speed of the PLL transient until the point at which stability begins to be compromised. The optimal gain depends on N. Table 8 lists recommended settings for different values of N.

Table 8. Optimal K_P Settings

N	RF1 K_{P1}<1:0>	RF2 K_{P2}<1:0>	IF K_{PI}<1:0>
≤2047	00	00	00
2048 to 4095	00	01	01
4096 to 8191	01	10	10
8192 to 16383	10	11	11
≥16384	11	11	11

The VCO gain and loop filter characteristics are not programmable.

The settling time for each PLL is directly proportional to its phase detector update period T_ϕ (T_ϕ equals $1/f_\phi$). During the first 13 update periods the Si4136 executes the self-tuning algorithm. Thereafter the PLL controls the output frequency. Because of the unique architecture of the Si4136 PLLs, the time required to settle the output frequency to 0.1 ppm error is only about 25 update periods. Thus, the total time after power-up or a change in programmed frequency until the synthesized frequency is well settled—including time for self-tuning—is around 40 update periods.

Note: This settling time analysis holds for $f_\phi \leq 500$ kHz. For $f_\phi > 500$ kHz, the settling time can be a maximum of 100 µs as specified in Table 5.

2.6. RF and IF Outputs (RFOUT and IFOUT)

The RFOUT and IFOUT pins are driven by amplifiers that buffer the RF VCOs and IF VCO, respectively. The RF output amplifier receives its input from either the RF1 or RF2 VCO, depending upon which R- or N-Divider register was last written. For example, programming the N-Divider register for RF1 automatically selects the RF1 VCO output.

Figure 13 on page 15 shows an application diagram for the Si4136. The RF output signal must be AC coupled to its load through a capacitor.

The IFOUT pin must also be AC coupled to its load through a capacitor. The IF output level is dependent upon the load. Figure 17 displays the output level versus load resistance. For resistive loads greater than 500 Ω the output level saturates and the bias currents in the IF output amplifier are higher than they need to be. The LPWR bit in the Main Configuration register

(Register 0) can be set to 1 to reduce the bias currents and therefore reduce the power dissipated by the IF amplifier. For loads less than 500 Ω, LPWR should be set to 0 to maximize the output level.

For IF frequencies greater than 500 MHz, a matching network is required in order to drive a 50 Ω load. See Figure 15 below. The value of L_{MATCH} can be determined by Table 9.

Typical values range between 8 nH and 40 nH.

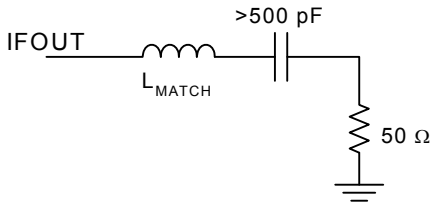


Figure 15. IF Frequencies > 500 MHz

Table 9. L_{MATCH} Values

Frequency	L_{MATCH}
500–600 MHz	40 nH
600–800 MHz	27 nH
800–1 GHz	18 nH

For frequencies less than 500 MHz, the IF output buffer can directly drive a 200 Ω resistive load or higher. For resistive loads greater than 500 Ω (f < 500 MHz) the LPWR bit can be set to reduce the power consumed by the IF output buffer. See Figure 16 below.

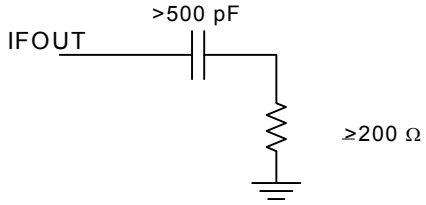


Figure 16. IF Frequencies < 500 MHz

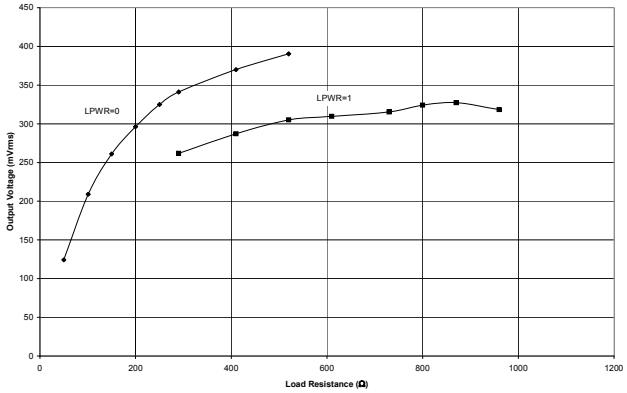


Figure 17. Typical IF Output Voltage vs. Load Resistance at 550 MHz

2.7. Reference Frequency Amplifier

The Si4136 provides a reference frequency amplifier. If the driving signal has CMOS levels, it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be AC coupled to the XIN pin through a 560 pF capacitor.

2.8. Powerdown Modes

Table 10 summarizes the powerdown functionality. The Si4136 can be powered down by taking the PWDN pin low or by setting bits in the Powerdown register (Register 2). When the PWDN pin is low, the Si4136 will be powered down regardless of the Powerdown register settings. When the PWDN pin is high, power management is under control of the Powerdown register bits.

The IF and RF sections of the Si4136 circuitry can be individually powered down by setting the Powerdown register bits PDIB and PDRB low. The reference frequency amplifier will also be powered up if either the PDRB and PDIB bits are high. Also, setting the AUTOPDB bit to 1 in the Main Configuration register (Register 0) is equivalent to setting both bits in the Powerdown register to 1.

The serial interface remains available and can be written in all power-down modes.

2.9. Auxiliary Output (AUXOUT)

The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration register (Register 0).

The LDETB signal can be selected by setting the AUXSEL bits to 011. This signal can be used to indicate that the IF or RF PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned.

Table 10. Powerdown Configuration

$\overline{\text{PWDN}}$ Pin	AUTOPDB	PDIB	PDRB	IF Circuitry	RF Circuitry
$\overline{\text{PWDN}}$ = 0	x	x	x	OFF	OFF
$\overline{\text{PWDN}}$ = 1	0	0	0	OFF	OFF
	0	0	1	OFF	ON
	0	1	0	ON	OFF
	0	1	1	ON	ON
	1	x	x	ON	ON

Note: x = don't care.

3. Control Registers

Table 11. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	0	0	0	0	AUXSEL		IFDIV		0	0	0	XIN DIV2	LPWR	0	AUTO PDB	0	0	0
1	Phase Detector Gain	0	0	0	0	0	0	0	0	0	0	0	0	K_{PI}		K_{P2}		K_{P1}	
2	Powerdown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB
3	RF1 N Divider	N_{RF1}																	
4	RF2 N Divider	0	N_{RF2}																
5	IF N Divider	0	0	N_{IF}															
6	RF1 R Divider	0	0	0	0	0	R_{RF1}												
7	RF2 R Divider	0	0	0	0	0	R_{RF2}												
8	IF R Divider	0	0	0	0	0	R_{IF}												
9	Reserved																		
. . .																			
15	Reserved																		

Note: Registers 9–15 are reserved. Writes to these registers may result in unpredictable behavior.

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	AUXSEL		IFDIV		0	0	0	XIN DIV2	LPWR	0	AUTO PDB	0	0	0

Bit	Name	Function
17:14	Reserved	Program to zero.
13:12	AUXSEL	**Auxiliary Output Pin Definition.** 00 = Reserved. 01 = Force output low. 11 = Lock Detect (LDETB).
11:10	IFDIV	**IF Output Divider** 00 = IFOUT = IFVCO Frequency 01 = IFOUT = IFVCO Frequency/2 10 = IFOUT = IFVCO Frequency/4 11 = IFOUT = IFVCO Frequency/8
9:7	Reserved	Program to zero.
6	XINDIV2	**XIN Divide-By-2 Mode.** 0 = XIN not divided by 2. 1 = XIN divided by 2.
5	LPWR	**Output Power-Level Settings for IF Synthesizer Circuit.** 0 = $R_{LOAD} < 500\ \Omega$—normal power mode. 1 = $R_{LOAD} \geq 500\ \Omega$—low power mode.
4	Reserved	Program to zero.
3	AUTOPDB	**Auto Powerdown** 0 = Software powerdown is controlled by Register 2. 1 = Equivalent to setting all bits in Register 2 = 1.
2:0	Reserved	Program to zero.

Register 1. Phase Detector Gain Address Field (A[3:0]) = 0001

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	K_{PI}		K_{P2}		K_{P1}	

Bit	Name	Function
17:6	Reserved	Program to zero.
5:4	K_{PI}	**IF Phase Detector Gain Constant.** N Value K_{PI} <2048 = 00 2048–4095 = 01 4096–8191 = 10 >8191 = 11
3:2	K_{P2}	**RF2 Phase Detector Gain Constant.** N Value K_{P2} <2048 = 00 2048–4095 = 01 4096–8191 = 10 >8191 = 11
1:0	K_{P1}	**RF1 Phase Detector Gain Constant.** N Value K_{P1} <4096 = 00 4096–8191 = 01 8192–16383 = 10 >16383 = 11

Register 2. Powerdown Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB

Bit	Name	Function
17:2	Reserved	Program to zero.
1	PDIB	**Powerdown IF Synthesizer.** 0 = IF synthesizer powered down. 1 = IF synthesizer on.
0	PDRB	**Powerdown RF Synthesizer.** 0 = RF synthesizer powered down. 1 = RF synthesizer on.

Register 3. RF1 N Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_{RF1}																	

Bit	Name	Function
17:0	N_{RF1}	**N Divider for RF1 Synthesizer.** $N_{RF1} \geq 992$.

Register 4. RF2 N Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	N_{RF2}																

Bit	Name	Function
17	Reserved	Program to zero.
16:0	N_{RF2}	**N Divider for RF2 Synthesizer.** $N_{RF2} \geq 240$.

Register 5. IF N Divider Address Field (A[3:0]) = 0101

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	N_{IF}															

Bit	Name	Function
17:16	Reserved	Program to zero.
15:0	N_{IF}	**N Divider for IF Synthesizer.** $N_{IF} \geq 56$.

Register 6. RF1 R Divider Address Field (A[3:0]) = 0110

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	R_{RF1}												

	Name	Function
17:13	Reserved	Program to zero.
12:0	R_{RF1}	**R Divider for RF1 Synthesizer.** R_{RF1} can be any value from 7 to 8189 if K_{P1} = 00 8 to 8189 if K_{P1} = 01 10 to 8189 if K_{P1} = 10 14 to 8189 if K_{P1} = 11

Register 7. RF2 R Divider Address Field (A[3:0]) = 0111

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	R_{RF2}												

Bit	Name	Function
17:13	Reserved	Program to zero.
12:0	R_{RF2}	**R Divider for RF2 Synthesizer.** R_{RF2} can be any value from 7 to 8189 if K_{P2} = 00 8 to 8189 if K_{P2} = 01 10 to 8189 if K_{P2} = 10 14 to 8189 if K_{P2} = 11