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AERO™+ TRANSCEIVER FOR GSM AND GPRS WIRELESS COMMUNICATIONS

Features

- Low-IF receiver:
  - Dual or triple-band LNA
  - Image-reject down-converter
- Universal baseband interface:
  - Digital IF to baseband converter
  - Channel filter and gain control
  - Analog or digital I/Q interface
- Offset-PLL transmitter:
  - Integrated TX VCO and loop filter
- Dual RF synthesizer:
  - Integrated RF and IF VCOs, loop filters, varactors, and resonators
- Integrated reference oscillator:
  - 13 or 26 MHz operation
- Quad-band support:
  - GSM 850 Class 4, small MS
  - E-GSM 900 Class 4, small MS
  - DCS 1800 Class 1
  - PCS 1900 Class 1
- GPRS Class 12 compliant
- CMOS process technology
- Low profile packages:
  - Si4200: 5 x 5 mm MLP32
  - Si4201: 4 x 4 mm MLP20
  - Si4134T: 5 x 5 mm MLP32
- 3-wire serial interface
- 2.7 V to 3.0 V operation

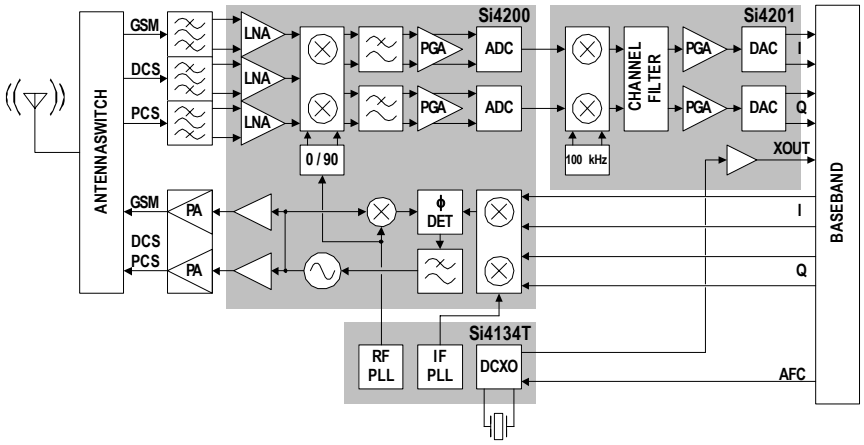
Applications

- Multi-band GSM/GPRS digital cellular handsets
- Multi-band GPRS data modems and terminals

Description

The Aero™+ transceiver is a complete RF front end for multi-band GSM and GPRS wireless communications. No external IF SAW filter or VCO modules are required as all functions are completely implemented on-chip, resulting in a dramatic reduction of board area and component count. The Aero+ transceiver includes a digitally-controlled crystal oscillator (DCXO) that completely integrates the reference oscillator and varactor.

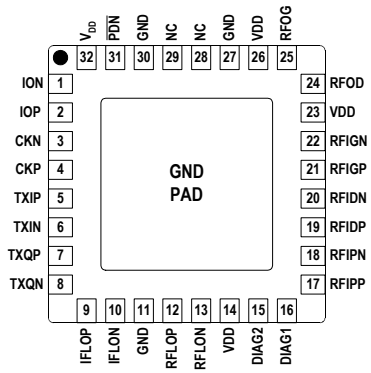
Functional Block Diagram



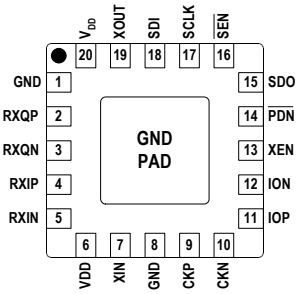
Pin Assignments (Top View)

Si4200-BM

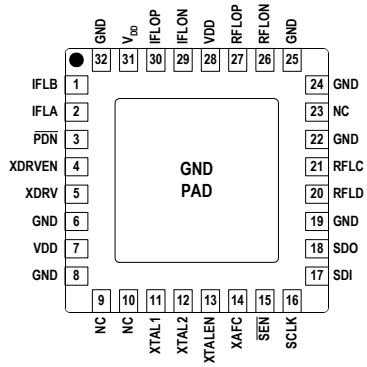
(Si4200DB-BM see page 39)



Si4201-BM



Si4134T-BM



Ordering Information: See page 42.

Patents pending

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Section **Page**

Electrical Specifications

Table 1. Recommended Operating Conditions[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–20	25	85	°C
Supply Voltage	V_{DD}		2.7	2.85	3.0	V
Supply Voltages Difference	V_Δ		–0.3	—	0.3	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at 2.85 V and an operating temperature of 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
2. Supply voltage difference specification applies to power supply pins per IC.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.3	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		10	dBm

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **The Si4200 and Si4134T devices are high-performance RF integrated circuits with an ESD rating of < 2 kV. Handling and assembly of these devices should only be done at ESD-protected workstations.**
3. For signals SCLK, SDI, $\overline{SEN}$, $\overline{PDN}$, XIN, XEN, XTALEN, and XDRVEN.
4. At SAW filter output for all bands.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si4200 Supply Current	I_{RX0}	Receive mode	—	55	80	mA
	I_{TX0}	Transmit mode	—	60	80	mA
	I_{PDN0}	$\overline{PDN}$ = 0	—	1	50	µA
Si4201 Supply Current[1]	I_{RX1}	Receive mode	—	9	12	mA
	I_{PDN1}	$\overline{PDN}$ = 0, XEN = 0, XBUF = 0, XPD1 = 1	—	1	50	µA
	I_{XOUT1}	$\overline{PDN}$ = 0, XEN = 1	—	1	2	mA
Si4134T Supply Current[2]	I_{RX3}	Receive mode	—	18	22	mA
	I_{TX3}	Transmit mode	—	24	30	mA
	I_{PDN3}	$\overline{PDN}$ = 0, XTALEN = 0	—	1	50	µA
	I_{XTAL13}	$\overline{PDN}$ = 0, XTALEN = 1, f_{REF} = 13 MHz	—	2.5	3.5	mA
	I_{XTAL26}	$\overline{PDN}$ = 0, XTALEN = 1, f_{REF} = 26 MHz	—	3.0	4.0	mA
Total Chipset Supply Current	I_{RX}	Receive mode	—	83	—	mA
	I_{TX}	Transmit mode	—	85	—	mA
High Level Input Voltage[3]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[3]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[3]	I_{IH}	V_{IH} = V_{DD} = 3.0 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IL} = 0 V, V_{DD} = 3.0 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OL} = 500 µA	—	—	0.4	V
High Level Output Voltage[5]	V_{OH}	I_{OH} = –10 mA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[5]	V_{OL}	I_{OL} = 10 mA	—	—	0.4	V

Notes:
1. Measured with load on XOUT pin of 10 pF and f_{REF} = 13 MHz. Limits with XEN = 1 guaranteed by characterization.
2. RF1 VCO is used for receive mode, RF2 and IF VCOs are used for transmit mode. Center frequencies for each VCO are as follows: RF1 = 1.9 GHz, RF2 = 1.35 GHz, IF = 825 MHz, f_{REF} = 13 MHz.
3. For pins SCLK, SDI, SEN, XEN, PDN, XDRVEN, and XTALEN.
4. For pins SDO and XOUT.
5. For pins DIAG1 and DIAG2.

Table 4. AC Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{CLK}	Figure 1, Figure 3	35	—	—	ns
SCLK Rise Time	t_R	Figure 1, Figure 3	—	—	50	ns
SCLK Fall Time	t_F	Figure 1, Figure 3	—	—	50	ns
SCLK High Time	t_{HI}	Figure 1, Figure 3	10	—	—	ns
SCLK Low Time	t_{LO}	Figure 1, Figure 3	10	—	—	ns
$\overline{\text{PDN}}$ Rise Time	t_{PR}	Figure 2	—	—	10	ns
$\overline{\text{PDN}}$ Fall Time	t_{PF}	Figure 2	—	—	10	ns
SDI Setup Time to SCLK↑	t_{SU}	Figure 3	15	—	—	ns
SDI Hold Time from SCLK↑	t_{HOLD}	Figure 3	10	—	—	ns
$\overline{\text{SEN}}$↓ to SCLK↑ Delay Time	t_{EN1}	Figure 3	10	—	—	ns
SCLK↑ to $\overline{\text{SEN}}$↑ Delay Time	t_{EN2}	Figure 3, Figure 4	12	—	—	ns
$\overline{\text{SEN}}$↑ to SCLK↑ Delay Time	t_{EN3}	Figure 3, Figure 4	12	—	—	ns
$\overline{\text{SEN}}$ Pulse Width	t_W	Figure 3, Figure 4	10	—	—	ns
SCLK↓ to SDO Time	t_{CA}	Figure 4	—	—	27	ns
Digital Input Pin Capacitance[1]			—	—	5	pF
Allowable Board Capacitance[2]			—	—	1	pF

Notes:
1. For pins SCLK, SDI, $\overline{\text{SEN}}$, XEN, $\overline{\text{PDN}}$, XDRVEN, and XTALEN.
2. For pins CKN, CKP, ION, and IOP.

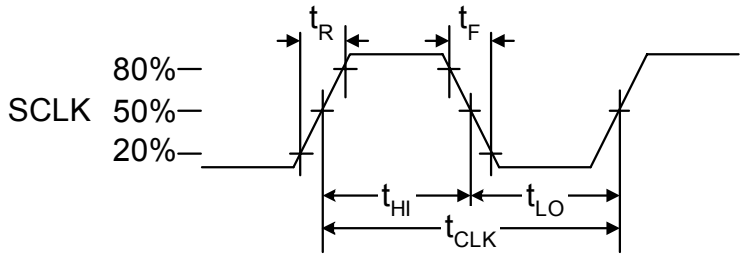


Figure 1. SCLK Timing Diagram

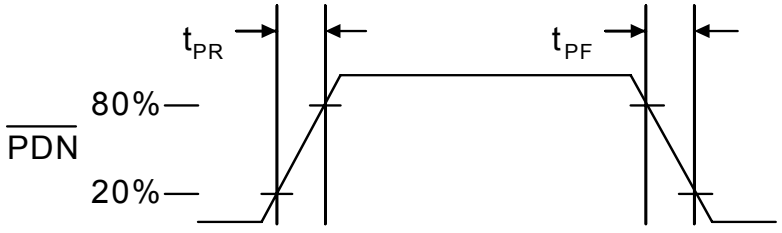


Figure 2. $\overline{\text{PDN}}$ Timing Diagram

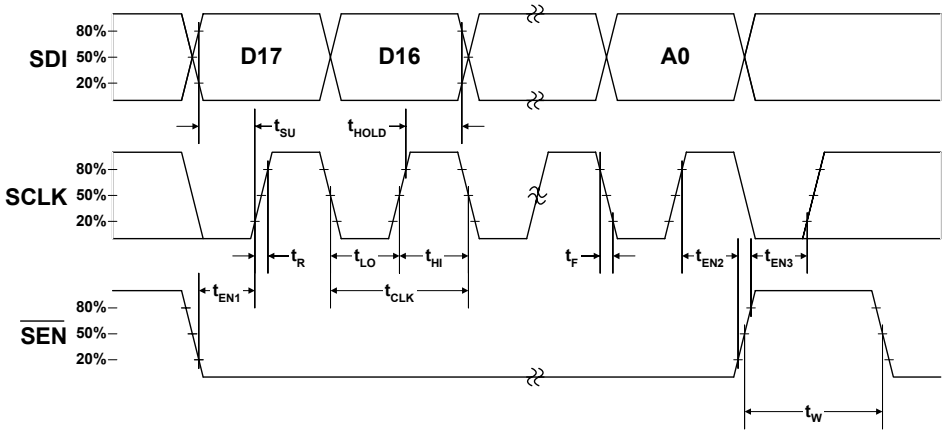


Figure 3. Serial Interface Write Timing Diagram

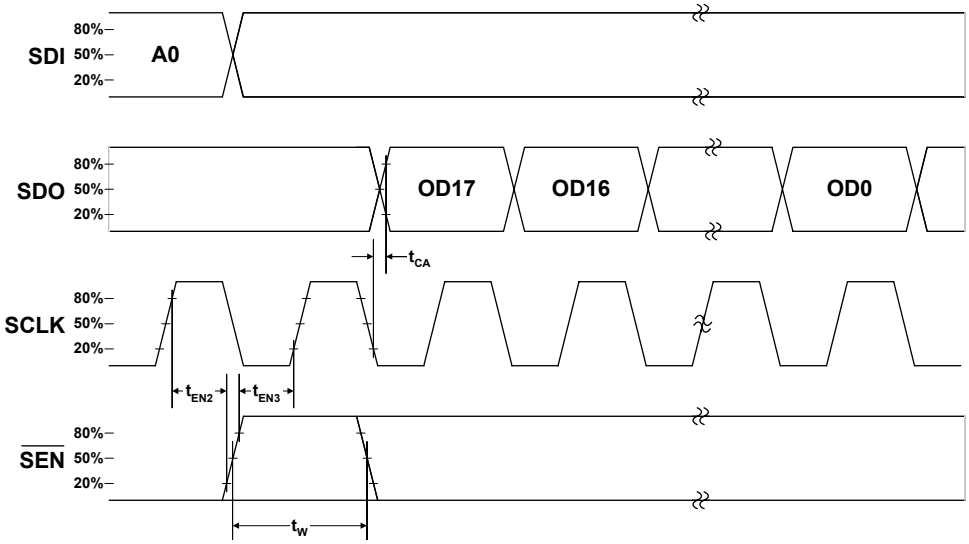


Figure 4. Serial Interface Read Timing Diagram

Table 5. Receiver Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GSM Input Frequency[1]	F_{IN}	GSM 850 band	869	—	894	MHz
		E-GSM 900 band	925	—	960	MHz
DCS or PCS Input Frequency[1]		DCS 1800 band	1805	—	1880	MHz
		PCS 1900 band	1930	—	1990	MHz
Noise Figure at 25 °C[2,3]	NF_{25}	GSM 850 band	—	2.6	3.3	dB
		E-GSM 900 band	—	2.7	3.4	dB
		DCS 1800 band	—	3.2	3.9	dB
		PCS 1900 band	—	3.6	4.3	dB
Noise Figure at 75 °C[2,3]	NF_{75}	GSM 850 band	—	3.3	4.0	dB
		E-GSM 900 band	—	3.4	4.1	dB
		DCS 1800 band	—	4.1	4.8	dB
		PCS 1900 band	—	4.8	5.5	dB
Noise Figure at 85 °C[2,3]	NF_{85}	GSM 850 band	—	3.4	4.1	dB
		E-GSM 900 band	—	3.5	4.2	dB
		DCS 1800 band	—	4.5	5.2	dB
		PCS 1900 band	—	5.1	5.8	dB
3 MHz Input Desensitization[2,3,4]	DES_3	GSM input	–25	–21	—	dBm
		DCS/PCS inputs	–28	–25	—	dBm
20 MHz Input Desensitization[2,3,4]	DES_{20}	GSM input	–20	–16	—	dBm
		DCS/PCS inputs	–19	–15	—	dBm
Input IP2[2]	IP2	$\lvert f_{1,2} - f_0 \rvert \geq 6$ MHz, $\lvert f_2 - f_1 \rvert = 100$ kHz	29	40	—	dBm
Input IP3[2]	IP3	$\lvert f_2 - f_1 \rvert \geq 800$ kHz, $f_0 = 2f_1 - f_2$	–18	–12	—	dBm
Image Rejection[2,4]	IR	GSM Input	28	35	—	dB
		DCS/PCS Inputs	28	40	—	dB
1 dB Input Compression[2,5]	CP_{MAX}	GSM Input	–28	–23	—	dBm
		DCS/PCS inputs	–27	–22	—	dBm
1 dB Input Compression[2,6]	CP_{MIN}	GSM Input	–23	–18	—	dBm
		DCS/PCS inputs	–23	–18	—	dBm
Minimum Voltage Gain[2,6,7]	G_{MIN}	GSM input	4.5	8.5	12.5	dB
		DCS/PCS inputs	11.5	15.5	19.5	dB
Maximum Voltage Gain[2,7]	G_{MAX}	GSM input	100	104	108	dB
		DCS/PCS inputs	96	102	106	dB
LNA Voltage Gain[3,8]	G_{LNA}	GSM input	—	17	—	dB
		DCS/PCS inputs	—	15	—	dB

Table 5. Receiver Characteristics (Continued)
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LNA Gain Control Range	ΔG_{LNA}	GSM input	13	17	21	dB
		DCS/PCS inputs	4	8	12	dB
Analog PGA Control Range	ΔG_{APGA}		13	16	19	dB
Analog PGA Step Size			3.2	4.0	4.8	dB
Digital PGA Control Range	ΔG_{DPGA}		—	63	—	dB
Digital PGA Step Size			—	1	—	dB
Maximum Differential Output Voltage[9]		DACFS[1:0] = 00	0.8	1.0	1.2	V_{PPD}
		DACFS[1:0] = 01	1.6	2.0	2.4	V_{PPD}
		DACFS[1:0] = 10	2.8	3.5	4.2	V_{PPD}
Output Common Mode Voltage[9]		DACCM[1:0] = 00	0.8	1.0	1.2	V
		DACCM[1:0] = 01	1.05	1.25	1.45	V
		DACCM[1:0] = 10	1.15	1.35	1.55	V
Differential Output Offset Voltage[9,10]			—	—	50	mV
Baseband Gain Error[9,10]			—	—	1	%
Baseband Phase Error[9,10]			—	—	1	deg
Output Load Resistance[9]	R_L	Single-ended	10	—	—	kΩ
Output Load Capacitance[9]	C_L	Single-ended	—	—	10	pF
Group Delay[11]		CSEL = 0	—	—	22	µs
		CSEL = 1	—	—	16	µs
Differential Group Delay[11]		CSEL = 0	—	—	1.5	µs
		CSEL = 1	—	—	1	µs
Powerup Settling Time[3,12]		From powerdown	—	200	220	µs

Notes:
1. GSM input pins RFIGP and RFIGN. DCS input pins RFIDP and RFIDN. PCS input pins RFIPP and RFIPN. On the Si4200DB, the PCS input should be used for either PCS 1900 or DCS 1800 bands.
2. Measurement is performed with a 2:1 balun (50 Ω input, 200 Ω balanced output) and includes matching network and PCB losses. Measured at max gain (AGAIN[2:0] =100b, LNAG[1:0] = 01b, LNAC[1:0] = 01b) unless otherwise noted. Noise figure measurements are referred to 290 °K. Insertion loss of the balun is removed.
3. Specifications guaranteed by characterization.
4. Input signal at balun is –102 dBm. SNR at baseband output is 9 dB.
5. AGAIN[2:0]=000b, LNAG[1:0] = 01b, LNAC[1:0] = 01b.
6. AGAIN[2:0]=000b, LNAG[1:0] = 00b, LNAC[1:0] = 00b.
7. Voltage gain is defined as the differential rms voltage at the RXIP/RXIN pins or RXQP/RXQN pins divided by the rms voltage at the balun input with DACFS[1:0] = 01 and CSEL = 1. Gain is 1.5 dB higher with CSEL = 0. Minimum and maximum values do not include the variation in the Si4201 DAC full scale voltage (also see Maximum Differential Output Voltage specification).
8. Voltage gain is defined as the differential rms voltage at the LNA output divided by the rms voltage at the balun output.
9. Output pins RXIP, RXIN, RXQP, RXQN.
10. The baseband signal path is entirely digital. Gain, phase, and offset errors at the baseband outputs are because of the Si4201 D/A converters. Offsets can be measured and calibrated out. See ZERODEL[2:0] in the register description.
11. Group delay is measured from antenna input to baseband outputs. Differential group delay is measured in-band.
12. Includes settling time of the Si4134T frequency synthesizer with 13 MHz DCXO output settled. Settling to 5 degrees phase error measured at RXIP, RXIN, RXQP, and RXQN pins.

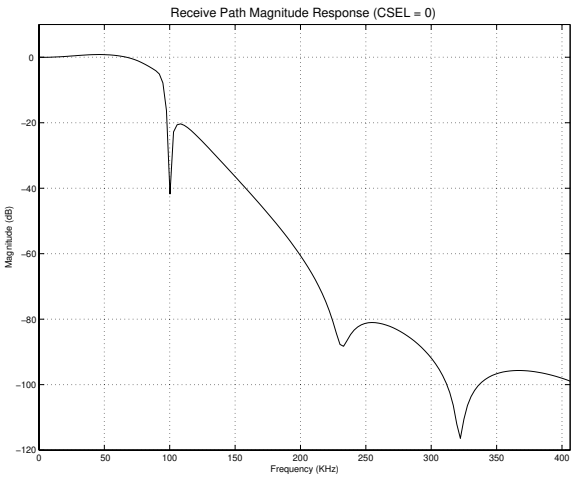


Figure 5. Receive Path Magnitude Response (CSEL = 0)

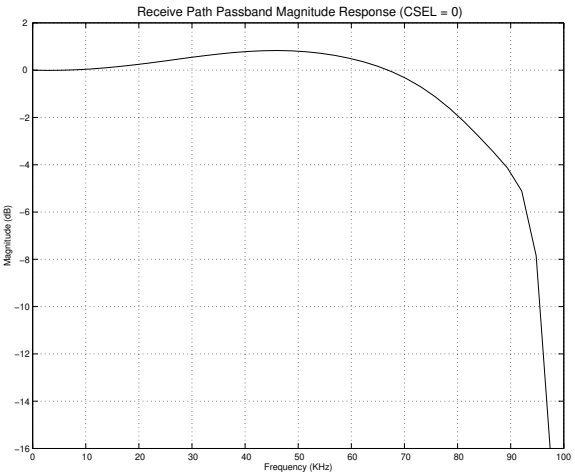


Figure 6. Receive Path Passband Magnitude Response (CSEL = 0)

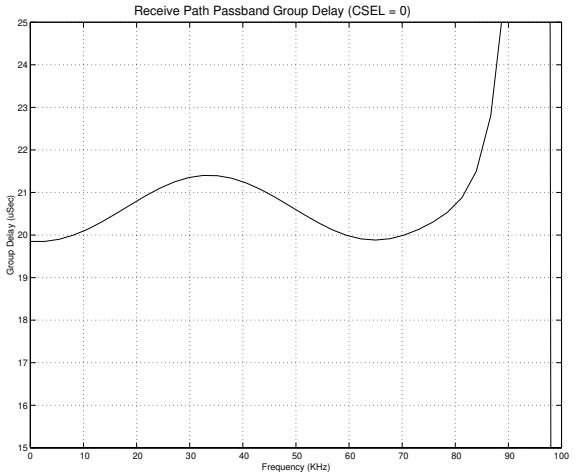


Figure 7. Receive Path Passband Group Delay (CSEL = 0)

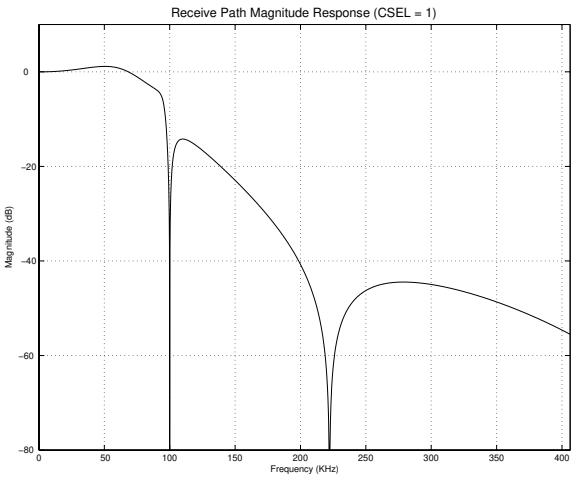


Figure 8. Receive Path Magnitude Response (CSEL = 1)

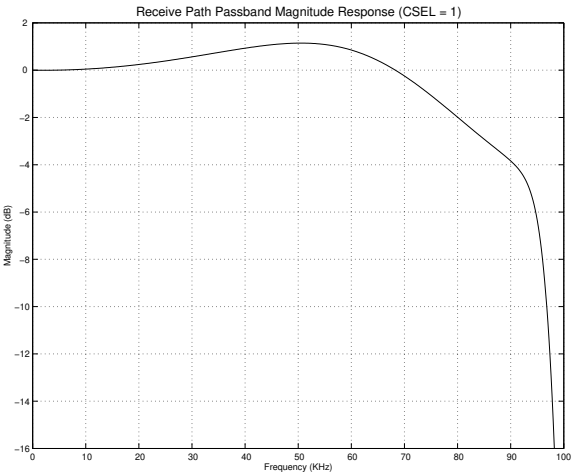


Figure 9. Receive Path Passband Magnitude Response (CSEL = 1)

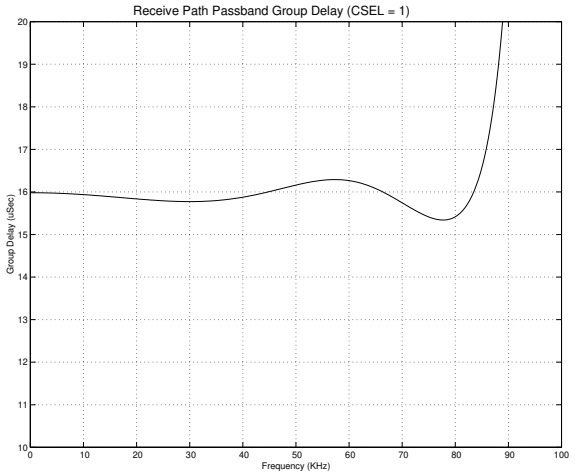


Figure 10. Receive Path Passband Group Delay (CSEL = 1)

Table 6. Transmitter Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RFOG Output Frequency[1]		GSM 850 band	824	—	849	MHz
		E-GSM 900 band	880	—	915	MHz
RFOD Output Frequency[2]		DCS 1800 band	1710	—	1785	MHz
		PCS 1900 band	1850	—	1910	MHz
I/Q Differential Input Swing[3,4]			0.88	—	2.2	V_{PPD}
I/Q Input Common-Mode[3]			1.1	—	1.4	V
I/Q Differential Input Resistance[3,4]		BBG[1:0] = 11b	26	30	35	kΩ
		BBG[1:0] = 00b	22	25	29	kΩ
		BBG[1:0] = 01b	17	20	23	kΩ
		Powered down	—	Hi-Z	—	kΩ
I/Q Input Capacitance[3,5]			—	—	5	pF
I/Q Input Bias Current[3]			13	16	19	μA
Sideband Suppression		67.7 kHz sinusoid	—	–46	–34	dBc
Carrier Suppression		67.7 kHz sinusoid	—	–48	–33	dBc
IM3 Suppression		67.7 kHz sinusoid	—	–57	–50	dBc
Phase Error[5]			—	1.9	3.0	$^{o}_{rms}$
			—	5	10	$^{o}_{PEAK}$
TXVCO Pushing[1,2]		Open loop	—	100	—	kHz/V
TXVCO Pulling[1,2]		VSWR 2:1, all phases open loop	—	200	—	kHz_{PP}
RFOG Output Modulation Spectrum[1,6]		400 kHz offset	—	–65	–63	dBc
		1.8 MHz offset	—	–70	–68	dBc
RFOD Output Modulation Spectrum[2,6]		400 kHz offset	—	–65	–63	dBc
		1.8 MHz offset	—	–70	–65	dBc
RFOG Output Phase Noise[1,5,7]		10 MHz offset	—	–160	–155	dBc/Hz
		20 MHz offset	—	–166	–164	dBc/Hz
RFOD Output Phase Noise[2,5,7]		20 MHz offset	—	–163	–157	dBc/Hz
RFOG Output Power Level[1]		Z_L = 50 Ω	7	9	11	dBm
RFOD Output Power Level[2]		Z_L = 50 Ω	6	8	10	dBm

Table 6. Transmitter Characteristics (Continued)
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Output Harmonic Suppression[1,2]		2nd harmonic	—	—	–20	dBc
		3rd harmonic	—	—	–10	dBc
Powerup Settling Time[5,8]		From powerdown	—	—	150	μs

Notes:
1. Measured at RFOG pin.
2. Measured at RFOD pin.
3. Input pins TXIP, TXIN, TXQP, and TXQN.
4. Differential Input Swing is programmable with the BBG[1:0] bits in Register 04h. Program these bits to the closest appropriate value. The I/Q Input Resistance scales inversely with the BBG[1:0] setting.
5. Specifications are guaranteed by characterization.
6. Measured with pseudo-random pattern. Carrier power and noise power < 1.8 MHz measured with 30 kHz RBW. Noise power ≥ 1.8 MHz measured with 100 kHz RBW.
7. Measured with all 1s pattern.
8. Including settling time of the Si4134T frequency synthesizer with 13 MHz DCXO output settled. Settling time measured at the RFOD and RFOG pins to 0.1 ppm frequency error.

Table 7. Frequency Synthesizer Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 VCO Frequency[1]	f_{RF1}	GSM 850 band	1737.8	—	1787.8	MHz
		E-GSM 900 band	1849.8	—	1919.8	MHz
		DCS 1800 band	1804.9	—	1879.9	MHz
		PCS 1900 band	1929.9	—	1989.9	MHz
RF2 VCO Frequency[1]	f_{RF2}	GSM 850 band	1272	—	1297	MHz
		E-GSM 900	1279	—	1314	MHz
		DCS 1800 band	1327	—	1402	MHz
		PCS 1900 band	1423	—	1483	MHz
IF VCO Frequency[1]	f_{IF}	GSM 850 band	—	896	—	MHz
		E-GSM 900 band 880–895 MHz 900–915 MHz	—	798	—	MHz
		E-GSM 900 band 895–900 MHz	—	790	—	MHz
		DCS 1800 band	—	766	—	MHz
		PCS 1900 band	—	854	—	MHz
RF1 PLL Phase Detector Update Frequency	f_ϕ	GSM input, RFUP = 0	—	200	—	kHz
		DCS/PCS inputs, RFUP = 1	—	100	—	kHz
IF and RF2 PLL Phase Detector Update Frequency	f_ϕ		—	200	—	kHz
RF2 VCO Nominal Capacitance[2,3]	C_{NOM}		—	4.8	—	pF
IF VCO Nominal Capacitance[2,3]			—	6.5	—	pF
RF2 VCO Package Inductance[2,3]	L_{PKG}		—	2.0	—	nH
IF VCO Package Inductance[2,3]			—	1.6	—	nH
RF1 VCO Pushing[3]		Open Loop	—	500	—	kHz/V
RF2 VCO Pushing[3]			—	400	—	kHz/V
IF VCO Pushing[3]			—	300	—	kHz/V
RF1 VCO Pulling[3]		VSWR = 2:1, all phases, open loop	—	400	—	kHz_{PP}
RF2 VCO Pulling[3]			—	100	—	kHz_{PP}
IF VCO Pulling[3]			—	100	—	kHz_{PP}
RF1 PLL Phase Noise[3]		3 MHz offset	—	–144	–138	dBc/Hz
RF2 PLL Phase Noise[3]		400 kHz offset	—	–126	–121	dBc/Hz
IF PLL Phase Noise[3]		400 kHz offset	—	–128	–123	dBc/Hz

Table 7. Frequency Synthesizer Characteristics (Continued)
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 PLL Spurious[3]		3 MHz offset	—	–95	–83	dBc
RF2 PLL Spurious[3]		400 kHz offset	—	–80	–75	dBc
IF PLL Spurious[3]		400 kHz offset	—	–80	–70	dBc

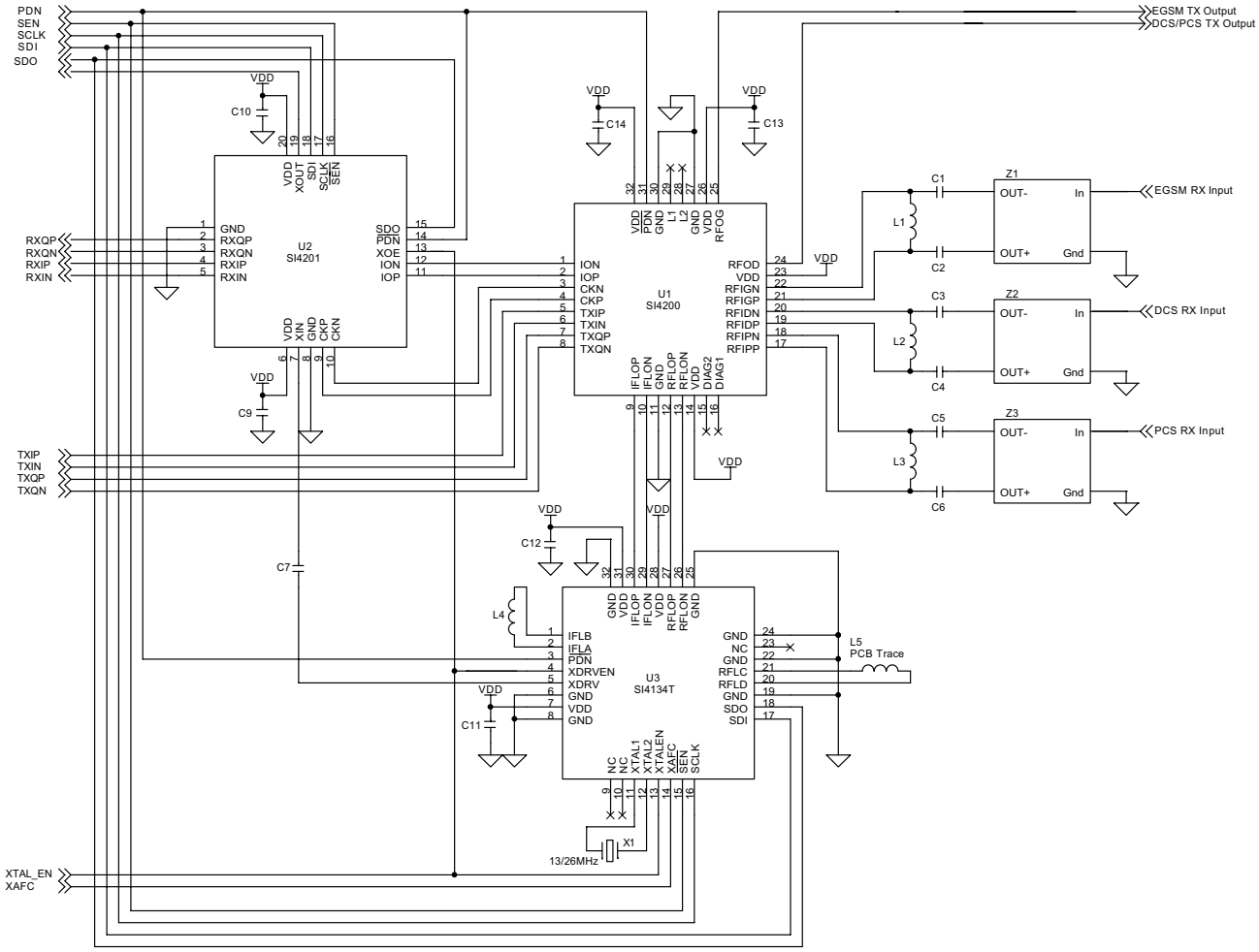
Notes:
1. For the GSM input, the RF1 VCO is divided by two on the Si4200. During transmit, the IF VCO is divided by two on the Si4200. These tuning ranges are guaranteed provided the VCOs on the Si4134T are properly centered during the PC board design phase. See “AN49: Aero Transceiver PCB Layout Guidelines” for more information.
2. See "VCO Inductor Design" on page 22.
3. Specifications are guaranteed by characterization.

Table 8. Reference Oscillator (DCXO) Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XDRV Board Capacitance	C_{XDRV}		—	—	2	pF
XTAL1 Trace Capacitance[1]	C_{XTAL1}		—	0.90	—	pF
XTAL2 Trace Capacitance[1]	C_{XTAL2}		—	0.63	—	pF
Crystal Oscillation Frequency	f_{REF}	XSEL = 0, DIV2 = 0	—	13	—	MHz
		XSEL = 1, DIV2 = 1	—	26	—	MHz
Crystal Load Capacitance	C_L		—	8	—	pF
Crystal Sensitivity[2]	S		—	22.5	—	ppm/pF
Initial Crystal Frequency Offset	Δf_{OFF}	T_A = 25 °C	–10	—	10	ppm
Crystal Frequency Tolerance[3]	Δf_{TOL}		–10	—	10	ppm
CDAC Range[4]	Δf_{CDAC}		20	—	—	ppm
CDAC Step Size[4,5]			—	1.0	1.5	ppm
CVAR Input Voltage	V_{XAFC}		0	—	2.5	V
CVAR Range[4]	Δf_{CVAR}	V_{CTL} = 0 to 2.5 V	20	30	60	ppm
Powerup Settling Time	t_{DCXO}	V_{CTL} = 1.25 V	—	1.0	—	ms

Notes:
1. See “AN49: Aero Transceiver PCB Layout Guidelines” for suggested layout.
2. Allowable manufacturing tolerance of ±10% from typical value.
3. Crystal accuracy over temperature range.
4. Specifications guaranteed when using a crystal that conforms to f_{REF} = 13 MHz, C_L = 8 pF, S = 22.5 ppm/pF, Δf_{OFF} = ±10 ppm, and Δf_{TOL} = ±10 ppm.
5. Average step size over CDAC codes 0 to 63.

Typical Triple-Band Application Schematic



Notes:

1. Connect GND pad on bottom of U1–U3 to GND.
2. All V_{DD} pins may be fed from a single supply or regulator.
3. For dual-band designs, the DCS LNA input pins (U1 pins 19–20) should be grounded. For a complete pinout, see "Pin Descriptions: Si4200DB-BM" on page 39.
4. See “AN49: Aero Transceiver PCB Layout Guidelines” for details on the following:
   - LNA matching network (C1–C6, L1–L3). Values should be custom tuned for a specific PCB layout and SAW filter to optimize performance.
   - Differential traces between the SAW filters (Z1–Z3) and transceiver (U1) pins 17–22.
   - Detailed SAW filter (Z1–Z3) requirements.
   - L4 and PCB inductor trace L5 for frequency synthesizer (U3) pins 1–2 and 20–21.
   - CKP/CKN and IOP/ION differential traces between transceiver (U1) pins 1–4 and baseband interface (U2) pins 9–12.
   - X1 connection to U3 pins 11–12.
5. XEN, XDRVEN, and XTALEN are recommended to be tied together and controlled simultaneously.

Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1–C2	1.2 pF, ±0.1 pF, C0G (GSM 850 and E-GSM 900)	Murata GRM36C0G series Venkel C0402C0G500 series
C3–C4	1.0 pF, ±0.1 pF, C0G (DCS 1800)	Murata GRM36C0G series Venkel C0402C0G500 series
C5–C6	1.0 pF, ±0.1 pF, C0G (PCS 1900)	Murata GRM36C0G series Venkel C0402C0G500 series
C7	100pF, ±5%, C0G	Venkel C0402C0G500 series
C9–C10, C13–C14	22 nF, ±20%, Z5U	
C11–C12	10 pF, ±20%, C0G	
L1	24 nH, ±5%	Murata LQW18AN series (0603 size) Murata LQW15A series (0402 size)
L2	7.5 nH, ±0.5 nH	Murata LQW18AN series (0603 size) Murata LQW15A series (0402 size)
L3	6.8 nH, ±0.2 nH	Murata LQW18AN series (0603 size) Murata LQW15A series (0402 size)
L4	3.9 nH, ±5%	Multi-layer (0402 or 0603 size)
L5	Inductor for RF2 VCO	PCB Trace
R1	100 Ω, ±5%	
U1	GSM Transceiver	Silicon Laboratories Si4200-BM
U2	Universal Baseband Interface	Silicon Laboratories Si4201-BM
U3	RF Synthesizer	Silicon Laboratories Si4134T-BM
X1	13 or 26 MHz Crystal, C_L = 8.0 pF	KDS BR13000AA0E KSS CX96FFFBQAJ13
Z1	GSM 850 RX SAW Filter (150 or 200 Ω balanced output)	EPCOS B39881-B7719-C610 (6-pin, 2.0x2.5 mm) EPCOS B39881-B9001-C710 (5-pin, 1.4x2.0 mm) Murata SAFSD881MFL0T00R00 (6-pin, 2.0x2.5 mm) Murata SAFEK881MFL0T00R00 (6-pin, 1.6x2.0 mm)
	E-GSM 900 RX SAW Filter (150 or 200 Ω balanced output)	EPCOS B39941-B7721-C910 (6-pin, 2.0x2.5 mm) EPCOS B39941-B7820-C710 (5-pin, 1.4x2.0 mm) Murata SAFSD942MFM0T00R00 (6-pin, 2.0x2.5 mm) Murata SAFEK942MFM0T00R00 (6-pin, 1.6x2.0 mm)
Z2	DCS 1800 RX SAW Filter (150 or 200 Ω balanced output)	EPCOS B39182-B7749-C910 (6-pin, 2.0x2.5 mm) EPCOS B39182-B7821-C710 (5-pin, 1.4x2.0 mm) Murata SAFSD1G84FA0T00R00 (6-pin, 2.0x2.5 mm) Murata SAFEK1G84FA0T00R00 (6-pin, 1.6x2.0 mm)
Z3	PCS 1900 RX SAW Filter (150 or 200 Ω balanced output)	EPCOS B39202-B7741-C910 (6-pin, 2.0x2.5 mm) EPCOS B39202-B7825-C710 (5-pin, 1.4x2.0 mm) Murata SAFSD1G96FB0T00R00 (6-pin, 2.0x2.5 mm) Murata SAFEK1G96FA0T00R00 (6-pin, 1.6x2.0 mm)

Functional Description

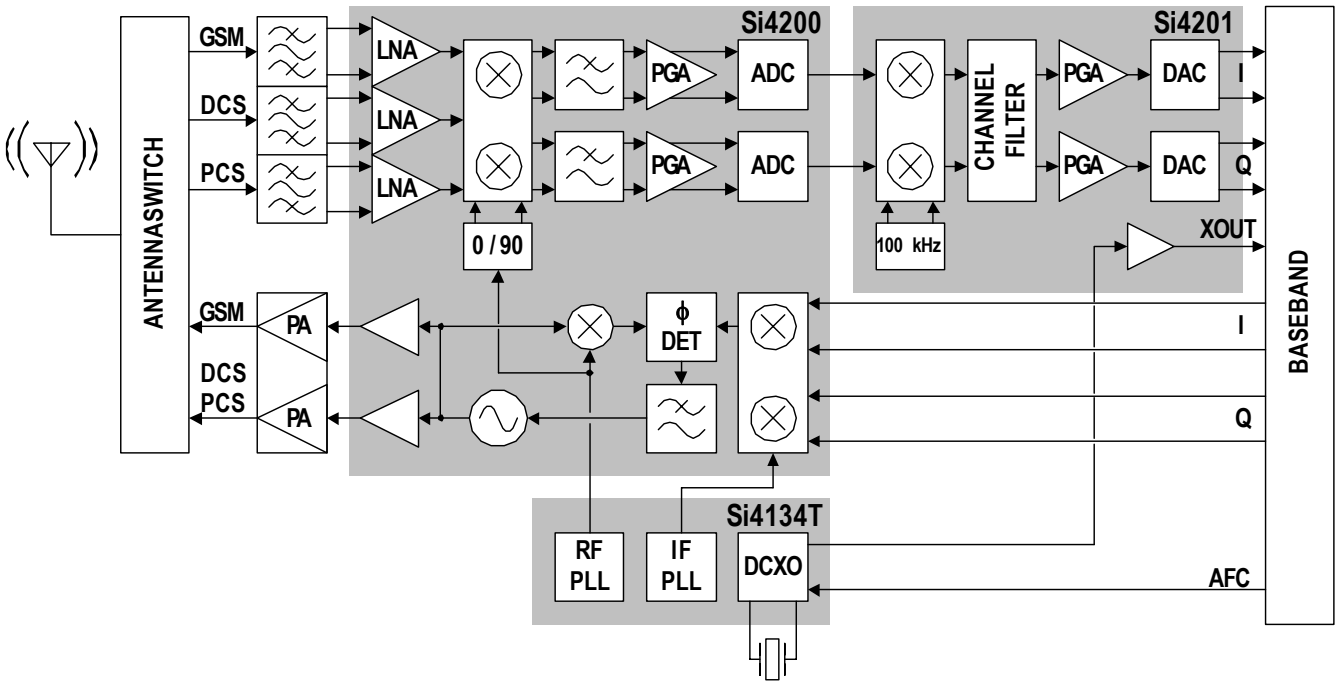


Figure 11. Aero+ Transceiver Block Diagram

The Aero+ transceiver is the industry's most integrated RF front end for multi-band GSM/GPRS digital cellular handsets and wireless data modems. The chipset consists of the Si4200 GSM transceiver, Si4201 universal baseband interface, and Si4134T dual RF synthesizer with an integrated digitally-controlled crystal oscillator (DCXO). The highly integrated solution eliminates the IF SAW filter, external low noise amplifiers (LNAs) for three bands, transmit and RF voltage-controlled oscillator (VCO) modules, and more than 60 other discrete components found in conventional designs.

The high level of integration combined with micro leadframe package (MLP) technology and fine line CMOS process technology results in a solution with 50% less area and 80% fewer components than competing solutions. A triple-band GSM transceiver using the Aero+ chipset can be implemented with 19 components in less than 2 cm^2 of board area. This level of integration is an enabling force in lowering the cost, simplifying the design and manufacturing, and shrinking the form factor in next-generation GSM/GPRS voice and data terminals.

The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduced complexity. The universal baseband interface is compatible with any supplier's baseband subsystem.

The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifier, and uses an offset phase-locked loop (PLL) with a fully integrated transmit VCO. The frequency synthesizer uses Silicon Laboratories' proven technology that includes integrated RF and IF VCOs, varactors, and loop filters.

The unique integer-N PLL architecture used in the Si4134T produces a transient response superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. This fast transient response makes the Aero+ chipset well suited to GPRS multi-slot applications where channel switching and settling times are critical.

While conventional solutions use BiCMOS or other bipolar process technologies, the Aero+ chipset is the industry's first cellular transceiver to be implemented in a 100% CMOS process. This brings the cost savings and extensive manufacturing capacity of CMOS to the GSM market.

Receive Section

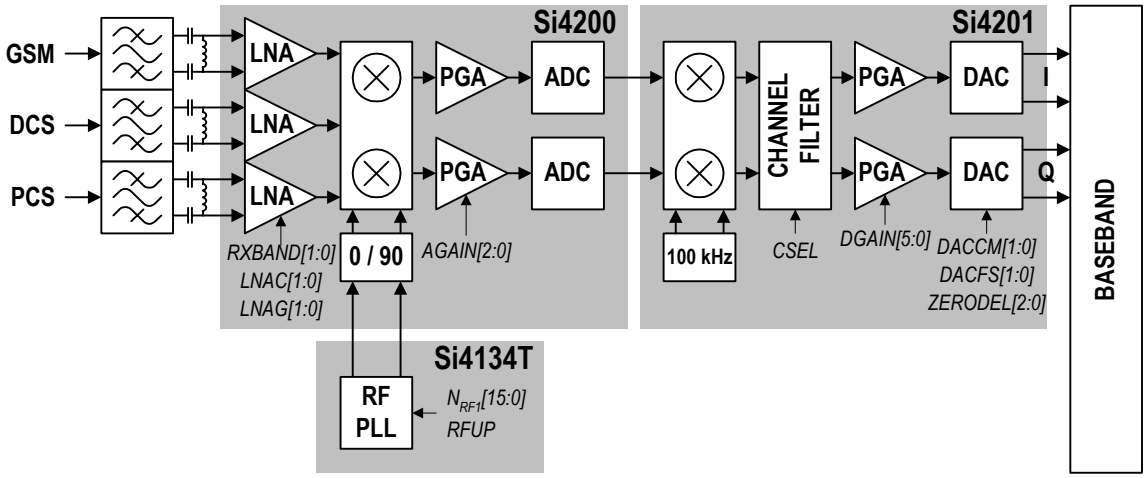


Figure 12. Receiver Block Diagram

The Aero+ transceiver uses a low-IF receiver architecture that allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF SAW filter required in conventional superheterodyne architectures. Compared to a direct-conversion architecture, the low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, 2nd-order distortion of blockers, and device 1/f noise. This relaxes the common-mode balance requirements on the input SAW filters and simplifies PC board design and manufacturing.

The Si4200 integrates three differential-input LNAs. The GSM input supports the GSM 850 (869–894 MHz) or E-GSM 900 (925–960 MHz) bands. The DCS input supports the DCS 1800 (1805–1880 MHz) band. The PCS input supports the PCS 1900 (1930–1990 MHz) band. For quad-band designs, SAW filters for the GSM 850 and E-GSM 900 bands should be connected to a balanced combiner which drives the GSM input for both bands. For dual-band designs using the Si4200DB-BM, the PCS input should be used for either DCS 1800 or PCS 1900 bands.

The LNA inputs are matched to the 200 Ω balanced-output SAW filters through external LC matching networks. See "AN49: Aero Transceiver PCB Layout Guidelines" for details. The LNA gain is controlled with the LNAG[1:0] and LNAC[1:0] bits in register 05h.

A quadrature image-reject mixer downconverts the RF signal to a 100 kHz intermediate frequency (IF) with the RFLO from the Si4134T frequency synthesizer. The RFLO frequency is between 1737.8 and 1989.9 MHz, and is divided by two in the Si4200 for GSM 850 and E-GSM 900 modes. The mixer output is amplified with an analog programmable gain amplifier (PGA), which is controlled with the AGAIN[2:0] bits in register 05h. The quadrature IF signal is digitized with high resolution A/D converters (ADCs).

The Si4201 downconverts the ADC output to baseband with a digital 100 kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. The response of the IIR filter is programmable to a high selectivity setting (CSEL = 0) or a low selectivity setting (CSEL = 1). The low selectivity filter has a flatter group delay response that may be desirable where the final channelization filter is in the baseband chip. After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN[5:0] bits in register 05h.

The LNAG[1:0], LNAC[1:0], AGAIN[2:0] and DGAIN[5:0] bits must be set to provide a constant amplitude signal to the baseband receive inputs. See "AN51: Aero Transceiver AGC Strategy" for more details.

DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, and RXQN pins to interface to standard analog-input baseband ICs. No special processing is required in the baseband for offset compensation or extended dynamic range. The receive and transmit baseband I/Q pins can be multiplexed together into a 4-wire interface. The common mode level at the receive I and Q outputs is programmable with the DACCM[1:0] bits, and the full scale level is programmable with the DACFS[1:0] bits in register 12h.

Transmit Section

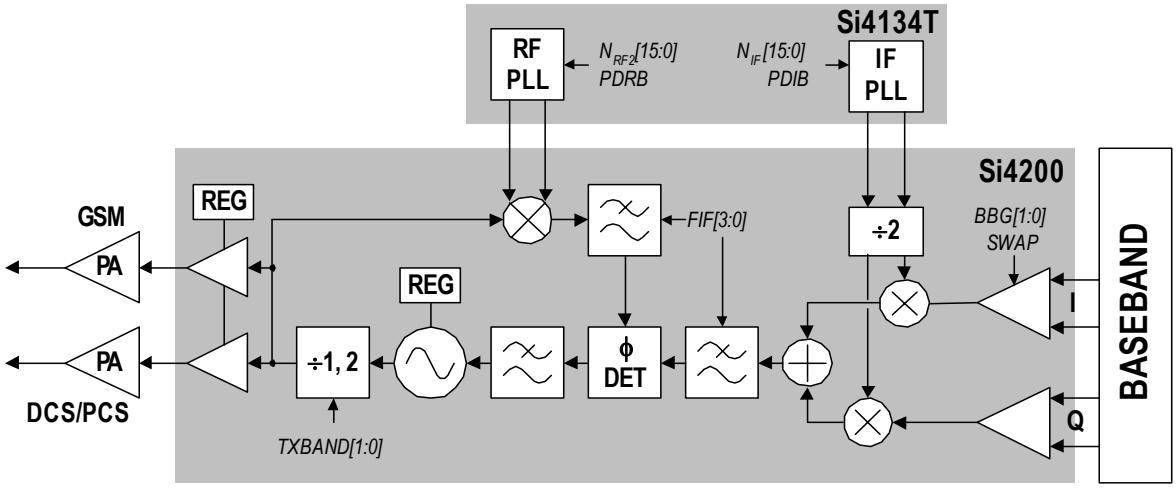


Figure 13. Transmitter Block Diagram

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two output buffers that can drive external power amplifiers (PA): one for the GSM 850 (824 to 849 MHz) and E-GSM 900 (880 to 915 MHz) bands and one for the DCS 1800 (1710 to 1785 MHz) and PCS 1900 (1850 to 1910 MHz) bands. The OPLL requires no external filtering to attenuate transmitter noise or spurious signals in the receive band, saving both cost and power. Additionally, the output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA.

A quadrature mixer upconverts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate a SSB IF signal that is filtered and used as the reference input to the OPLL. The Si4134T generates the IFLO frequency between 766 and 896 MHz. The IFLO is divided by two to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz. For the E-GSM 900 band, two different IFLO frequencies are required for spur management. Therefore, the IF PLL must be programmed per channel in the E-GSM 900 band. The IFLO frequencies are defined in Table 6 on page 12.

The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the DCS 1800 and PCS 1900 bands, and its output is divided by two for the GSM 850 and E-GSM 900 bands. The Si4134T generates the RFLO frequency between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the GSM 850 and E-GSM 900 bands, and low-side injection is used for the DCS 1800 and PCS 1900 bands. The I and Q signals are automatically swapped within the Si4200 when switching bands. Additionally, the SWAP bit in register 03h can be used to manually exchange the I and Q signals.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. The cutoff frequency of the filters is programmable with the FIF[3:0] bits in register 04h and should be set to the recommended settings detailed in the register description.

Frequency Synthesizer

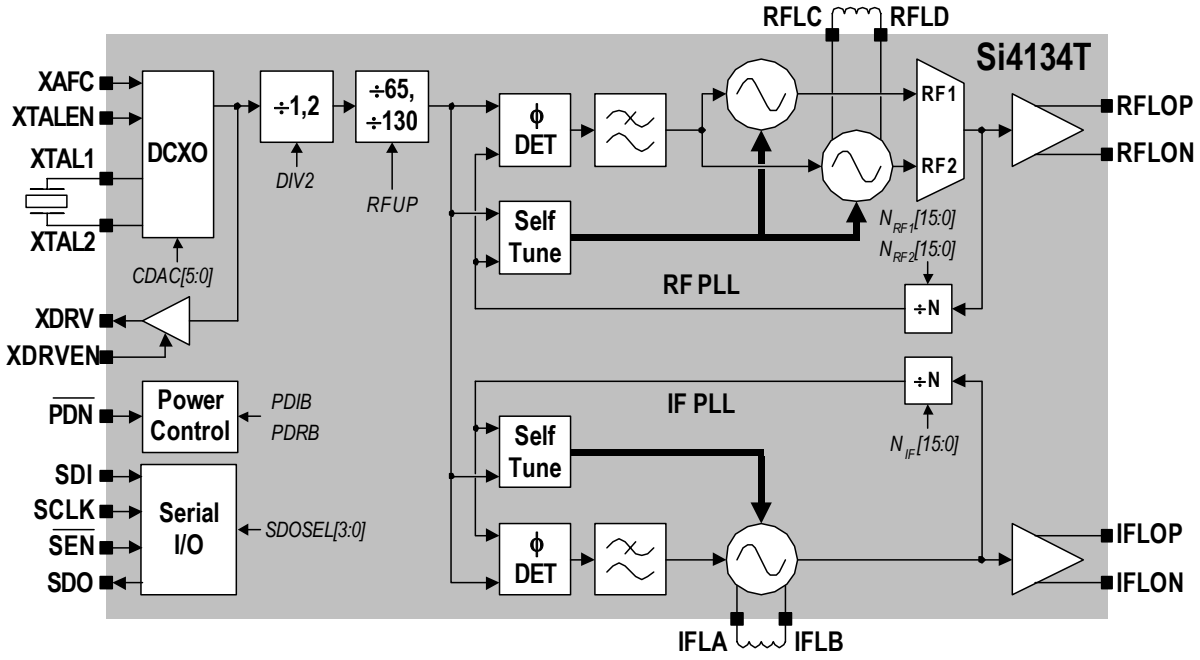


Figure 14. Si4134T Frequency Synthesizer Block Diagram

The Si4134T dual frequency synthesizer is a monolithic CMOS integrated circuit that performs IF and RF synthesis. An integrated digitally-controlled crystal oscillator (DCXO) is provided to generate the reference clock. The DCXO allows the use of a standard crystal resonator, avoiding the need for a crystal oscillator module.

Two complete PLLs are integrated including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. Differential outputs for the IF and RF PLLs are provided for direct connection to the Si4200 transceiver IC. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and the RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode and uses a single VCO.

The IF and RF output frequencies are set by programming the N-Divider registers, N_{RF1}, N_{RF2}, and N_{IF}. Programming the N-Divider register for either RF1 or RF2 automatically selects the proper VCO. The output frequency of each PLL is as follows:

$$f_{OUT} = N \times f_{\phi}$$

A programmable divider in the input stage allows either a 13 or 26 MHz reference frequency depending on the choice of crystal. When configured for 26 MHz operation using a TCXO, the DIV2 bit in Register 31h should be set appropriately. The RF PLL phase detector update rate (f_{ϕ}) can be programmed with the RFUP bit in Register 31h to either f_{ϕ} = 100 kHz or f_{ϕ} = 200 kHz. Receive mode should use f_{ϕ} = 100 kHz in DCS 1800 and PCS 1900 bands, and f_{ϕ} = 200 kHz in the GSM 850 and E-GSM 900 bands. For transmit modes, the RF2 and IF PLL phase detector update rates should always be configured for f_{ϕ} = 200 kHz.

VCO Inductor Design

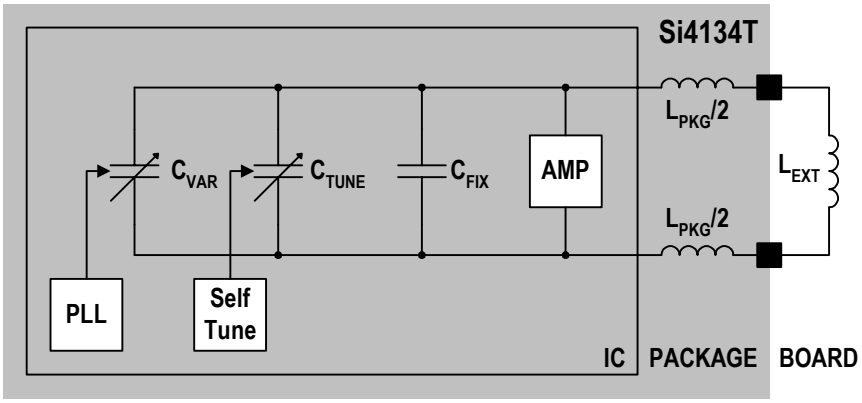


Figure 15. VCO Block Diagram

Determining L_{EXT}

The center frequencies for the RF2, and IF VCOs in the Si4134T are set using an external inductance (L_{EXT}). It is very important that L_{EXT} be properly designed to ensure maximum manufacturing margin for the desired VCO frequency tuning ranges. Because the total tank inductance is in the low nH range, the inductance of the package (L_{PKG}) must be considered in determining the correct external inductance.

Figure 15 shows the detailed configuration of the integrated VCOs. The total inductance (L_{TOT}) of each VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). The total capacitance (C_{TOT}) of each VCO is the sum of the self tuning capacitance (C_{TUNE}), the PLL varactor capacitance (C_{VAR}), and the fixed capacitance (C_{FIX}). The nominal capacitance (C_{NOM}) of each VCO is calculated with C_{TUNE} and C_{VAR} at their center values. C_{NOM} and L_{PKG} values are defined in Table 7 on page 14.

The center frequency is calculated as follows:

$$f_{CEN} = \frac{1}{2\pi\sqrt{C_{NOM}(L_{PKG} + L_{EXT})}}$$

The value for the external inductor is determined by the following:

$$L_{EXT} = \frac{1}{(2\pi f_{CEN})^2 C_{NOM}} - L_{PKG}$$

where f_{CEN} = desired center frequency of VCO.
C_{NOM} = nominal capacitance from Table 7.
L_{PKG} = package inductance from Table 7.
L_{EXT} = external inductance required.

Table 9. VCO f_{CEN} Values (MHz)

Supported Bands	RF1* VCO	RF2 VCO	IF VCO
European Dual-Band (900/1800)	1862	1341	782
Triple-Band (900/1800/1900)	1897	1381	810
Quad-Band (850/900/1800/1900) or North American Dual Band (850/1900)	1864	1378	831
***Note:** L_{EXT} is set internally.			

Table 10. VCO L_{EXT} Values (nH)

Supported Bands	RF2 VCO	IF VCO
European Dual-Band (900/1800)	0.91	4.77
Triple-Band (900/1800/1900)	0.75	4.34
Quad-Band (850/900/1800/1900) or North American Dual Band (850/1900)	0.76	4.04

For example, the RF2 VCO for a triple-band design requires f_{CEN} = 1381 MHz. Table 7 on page 14 shows C_{NOM} = 4.8 pF and L_{PKG} = 2.02 nH for the RF2 VCO. The previous equation shows L_{EXT} = 0.75 nH should be connected between the RFLC and RFLD pins.

See "AN49: Aero Transceiver PCB Layout Guidelines" for details on how to implement and verify the proper value of L_{EXT}.

DCXO Overview

The Si4134T integrates the DCXO circuitry required to generate a precise system reference clock using only an external crystal resonator. (See Figure 16.) An internal digitally programmable capacitor array (CDAC) provides a coarse method of adjusting the reference frequency in discrete steps. An integrated analog varactor (CVAR) allows for a fine and continuous adjustment of the reference frequency by an external control voltage (XAFC). This control voltage is supplied by the AFC DAC on the baseband IC. The complete DCXO solution effectively replaces the TCVCXO module typically required to provide a 13 or 26 MHz reference clock for the system. The Si4134T generates a single-ended 13 or 26 MHz output (XDRV) to drive the Si4201, and the Si4201 then buffers a 13 or 26 MHz reference clock (XOUT) to be sent to other system components such as the baseband. The complete circuit is shown in the "Typical Triple-Band Application Schematic" on page 16.

DCXO Tuning

The DCXO uses the CDAC and the CVAR to correct for both static and dynamic frequency errors, respectively. To compensate for crystal systematic offset error, the CDAC ensures a minimum of ±10 ppm frequency adjustment capability. The CDAC is programmed using register 28h.

The CDAC[5:0] register (register 28) may be programmed during powerup or after an initial calibration. Periodic adjustments to compensate for aging may also be performed over time to ensure accuracy.

The baseband determines the appropriate frequency adjustment based on the receipt of the FCCH burst. The baseband then adjusts the XAFC voltage using the baseband AFC DAC (12 or 13-bit), which controls the varactor on the Si4134T.

The baseband AFC DAC can adjust CVAR to correct for frequency variations caused by temperature drift. The step size per bit depends on the resolution of the AFC DAC and its output voltage range.

DCXO Crystal Selection

The tuning range specifications listed in Table 8 on page 15 for CDAC and CVAR assume that Aero+ is used with a crystal that conforms to the crystal parameters listed in the same table. Other crystals may be used with Aero+ for cost and/or performance reasons. For example, using a higher sensitivity crystal extends the CVAR and the CDAC frequency compensation range. However, care must be taken when using a more sensitive crystal because other system parameters are affected. Contact Silicon Laboratories' applications support for assistance in specifying other crystals.

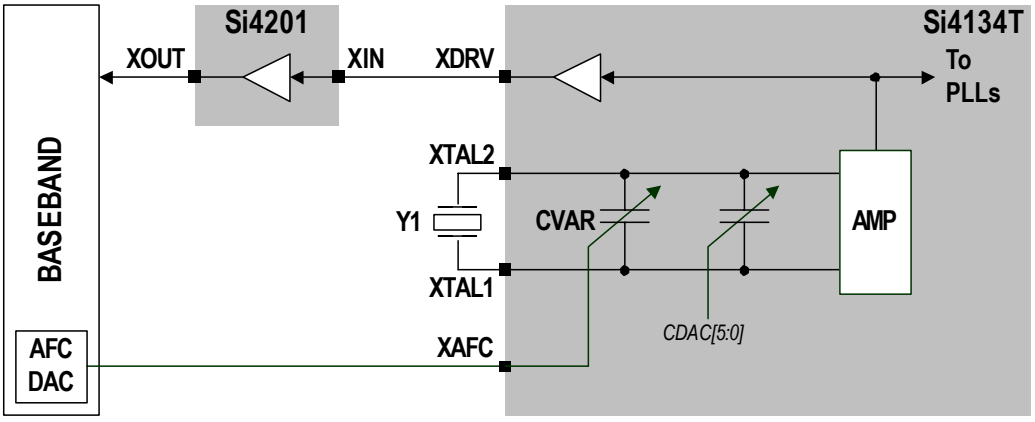


Figure 16. DCXO System Signal Routing Diagram

Serial Interface

A three-wire serial interface is provided to allow an external system controller to write the control registers for dividers, receive path gain, powerdown settings, and other controls. The serial control word is 24 bits in length, comprised of an 18-bit data field and a 6-bit address field as shown in Figure 17. A single logical register space is shared among the three chips, which is summarized in Table 11 on page 25.

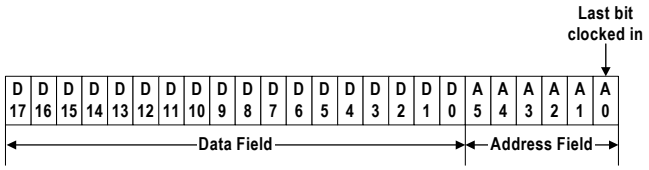


Figure 17. Serial Interface Format

The serial interface pins are intended to be connected in parallel to both the Si4201 and the Si4134T. Serial control is relayed from the Si4201 to the Si4200 over the signal interface (IOP/ION and CKP/CKN pins). All registers must be written when the $\overline{PDN}$ pin is asserted (low), except for Register 22h. All serial interface pins should be held at a constant level during receive and transmit bursts to minimize spurious emissions. This includes stopping the SCLK clock. A timing diagram for the serial interface is shown in Figure 3 on page 7.

When the serial interface is enabled (i.e., when $\overline{SEN}$ is low), data and address bits on the SDI pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of $\overline{SEN}$ into the internal data register addressed in the address field. The internal shift register ignores any leading bits before the 24 required bits. The serial interface is disabled when $\overline{SEN}$ is high.

Optionally, registers can be read as illustrated in Figure 4 on page 7. The serial output data appears on the SDO pin after writing the revision register with the address to be read. SDO is enabled when $\overline{PDN}$ = 0 on the Si4201 and when $\overline{PDN}$ = 1 on the Si4134T, allowing the SDO pin to be shared. Writing to any of the registers causes the function of SDO to revert to its previously programmed function.

XDRV Buffer

To supply a frequency adjusted reference clock to the Si4201, the XDRVEN pin on the Si4134T must be high. When held low, the Si4134T is fully operational, but no reference signal (either 13 or 26 MHz) is sourced from the XDRV pin.

The XTALEN signal controls the powerup state of the DCXO and must be enabled (XTALEN = 1) before the XDRV signal can be sourced.

XOUT Buffer

The Si4201 contains a reference clock buffer to drive the baseband input. The clock signal from the Si4134T is capacitively coupled to the XIN pin on the Si4201. To achieve complete powerdown during sleep, the XEN pin must be set low, the XBUF bit in Register 12 must be set to 0, and the XPD1 bit in Register 11 must be set to 1. During normal operation, these bits should set to their default values.

The XOUT buffer is a CMOS driver stage with approximately 250 Ω of series resistance. This buffer is enabled when the XEN hardware control (pin 13 on the Si4201) is set high, independent of the $\overline{PDN}$ control pin.

Control Registers

Table 11. Register Summary

	Reg	Name	Bit																	
			D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	00h	Si4200 Revision/Read	0	0	0	0	0	0	0	0	0	0	REV0[7:0]							
	01h	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET
	02h	Mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTO	MODE[1:0]	
	03h	Config	0	0	0	0	DIAG[1:0]		SWAP	0	0	0	TXBAND[1:0]		RXBAND[1:0]		0	0	1	0
	04h	Transmit	0	0	0	0	0	0	0	1	BBG[1:0]		FIF[3:0]				0	0	0	0
	05h	Receive	0	0	0	0	DGAIN[5:0]						0	AGAIN[2:0]			LNAC[1:0]		LNAG[1:0]	
	10h	Si4201 Revision/Read	0	0	0	0	0	0	0	0	0	0	REV1[7:0]							
	11h	Config	0	0	0	0	DPDS[2:0]			XPD1	1	XSEL	0	1	0	1	0	0	0	CSEL
	12h	DAC Config	0	0	0	0	0	0	0	1	XBUF‘	0	ZDBS	ZERODEL[2:0]			DACCM[1:0]		DACFS[1:0]	
	19h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Master Registers	20h	RX Master #1	RXBAND[1:0]	N_{RF1}[15:0]																
	21h	RX Master #2	0	DPDS[2:0]			LNAC[1:0]		LNAG[1:0]		AGAIN[2:0]		0	DGAIN[5:0]						
	22h	RX Master #3	0	0	0	0	0	0	0	0	0	0	0	0	DGAIN[5:0]					
	23h	TX Master #1	TXBAND[1:0]	N_{RF2}[15:0]																
	24h	TX Master #2	FIF[3:0]	N_{IF}[13:0]																
	28h	CDAC	0	0	0	0	0	0	0	0	0	0	0	0	CDAC[5:0]					
	30h	Si4134T Revision/Read	0	0	0	0	0	0	0	0	0	0	REV3[7:0]							
	31h	Config	0	0	0	SDOSEL[3:0]				0	0	0	0	0	0	RFUP	DIV2	0	0	0
	32h	Powerdown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB
	33h	RF1 N Divider	0	0	N_{RF1}[15:0]															
	34h	RF2 N Divider	0	0	N_{RF2}[15:0]															
	35h	IF N Divider	0	0	N_{IF}[15:0]															

Notes:

1. Any register not listed here is reserved and should not be written. Writing to reserved registers may result in unpredictable behavior.
2. Master registers 20h to 24h simplify programming the Aero+ transceiver to support initiation of receive (RX) and transmit (TX) operations with only two register writes.
3. See “AN50: Aero Transceiver Programming Guide” for detailed instructions on register programming.