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Dual N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)
25	0.0195 at V _{GS} = 4.5 V	8	11
	0.026 at V _{GS} = 2.5 V	8	

FEATURES

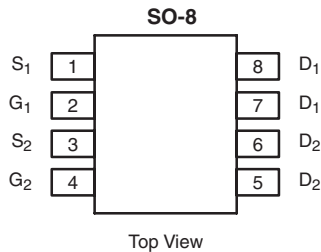
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested



RoHS
COMPLIANT
HALOGEN
FREE
Available

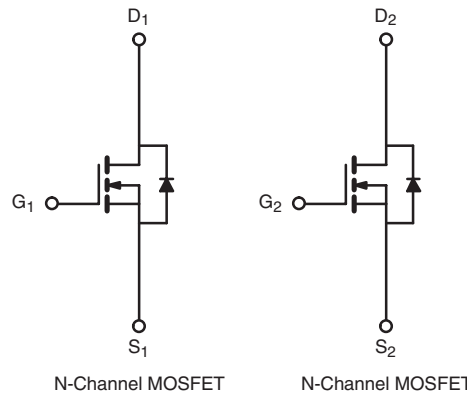
APPLICATIONS

- Synchronous Buck Converter



Top View

Ordering Information: Si4226DY-T1-E3 (Lead (Pb)-free)
Si4226DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	25	V
Gate-Source Voltage	V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	30	A
Source-Drain Current Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	1.7 ^{b, c}
Pulsed Source-Drain Current	I _{SM}	30	mJ
Single Pulse Avalanche Current	I _{AS}	10	
Single Pulse Avalanche Energy	E _{AS}	5	
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	50	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	30	38	

Notes:

- a. Based on T_C = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 110 °C/W.
- e. Package limited.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		26		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		2.0	V
Gate Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		0.0155	0.0195	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 5\text{ A}$		0.020	0.026	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 7\text{ A}$		40		S
Dynamic^a						
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1255		pF
Output Capacitance	C_{oss}			185		
Reverse Transfer Capacitance	C_{rss}			90		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		24	36	nC
		N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		11	17	
Q_{gs}			2			
Q_{gd}			2.5			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.3	1.4	2.8	Ω
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		8	16	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			24	40	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		14	25	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	50	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			2.6	A
Pulse Diode Forward Current ^a	I_{SM}				30	
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}$		0.73	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	28	nC
Reverse Recovery Fall Time	t_a			12		ns
Reverse Recovery Rise Time	t_b			13		

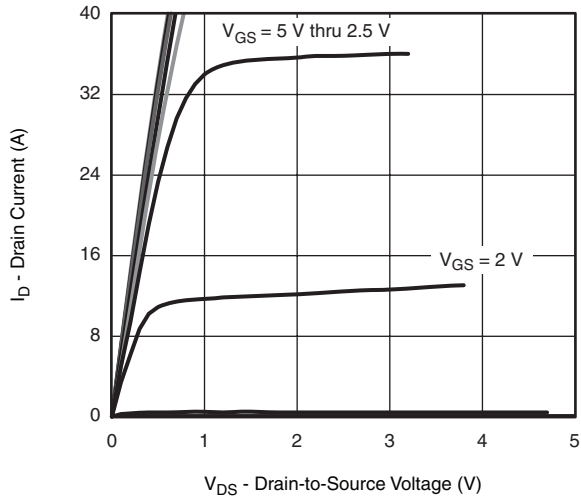
Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

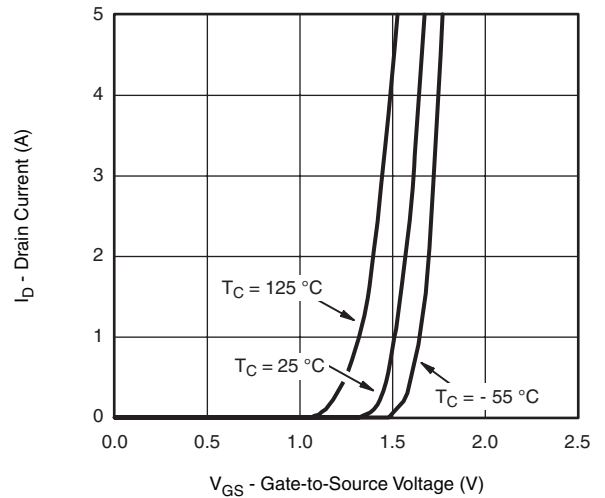
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



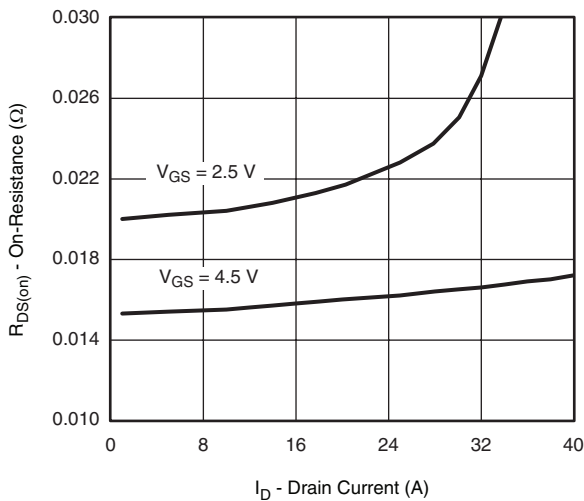
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



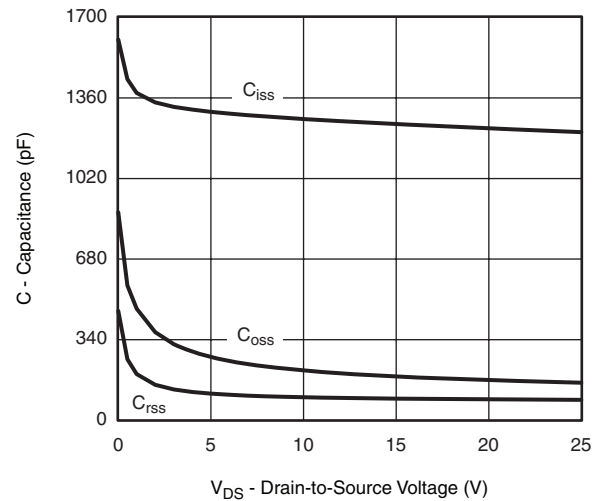
Output Characteristics



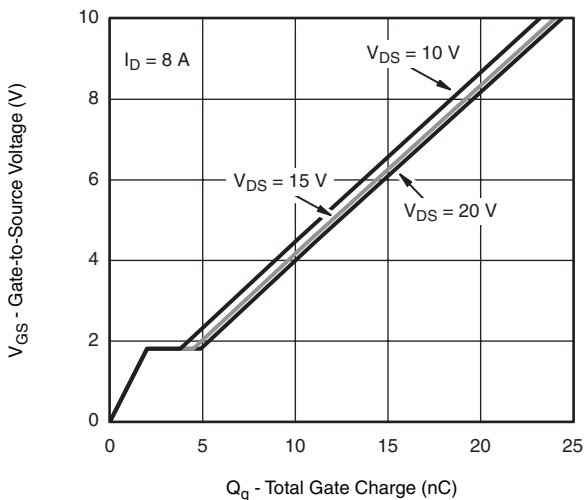
Transfer Characteristics



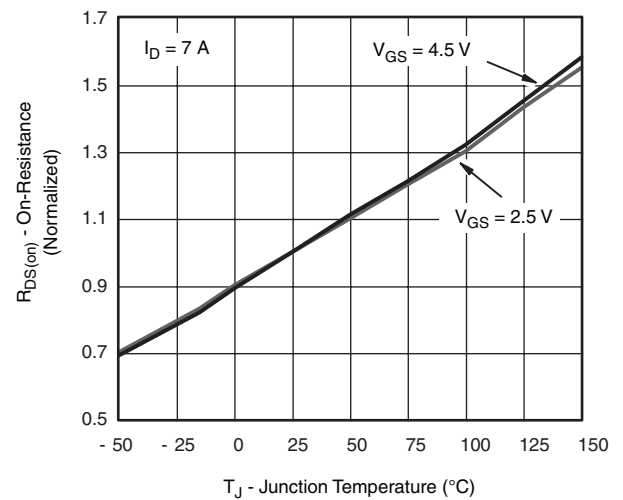
On-Resistance vs. Drain Current



Capacitance



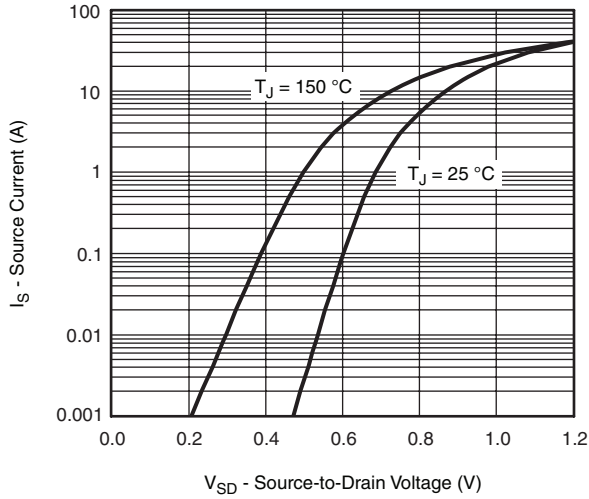
Gate Charge



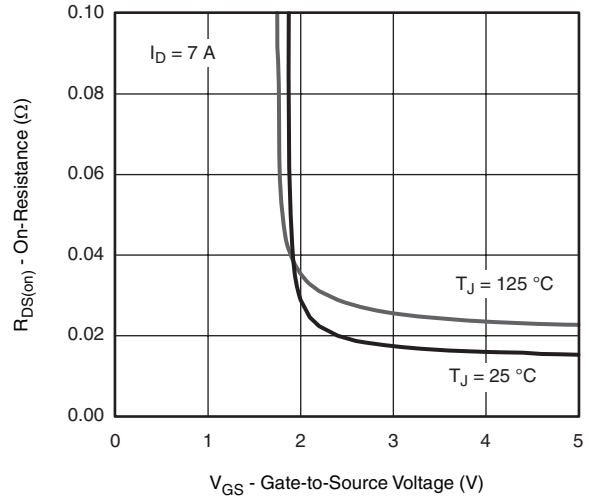
On-Resistance vs. Junction Temperature



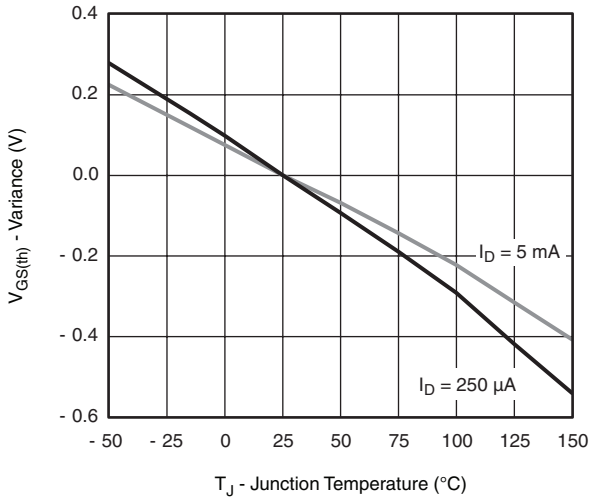
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



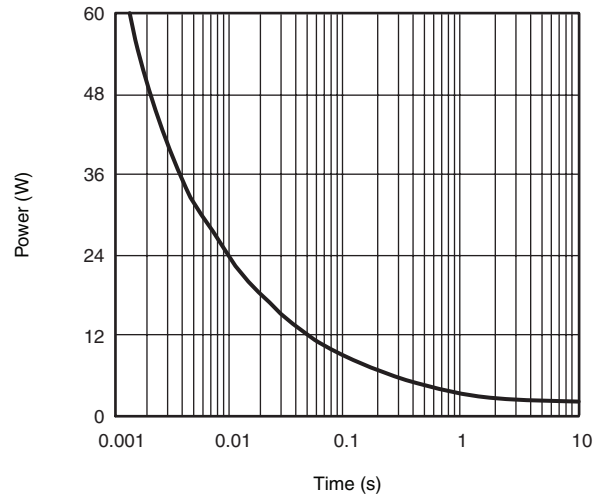
Source-Drain Diode Forward Voltage



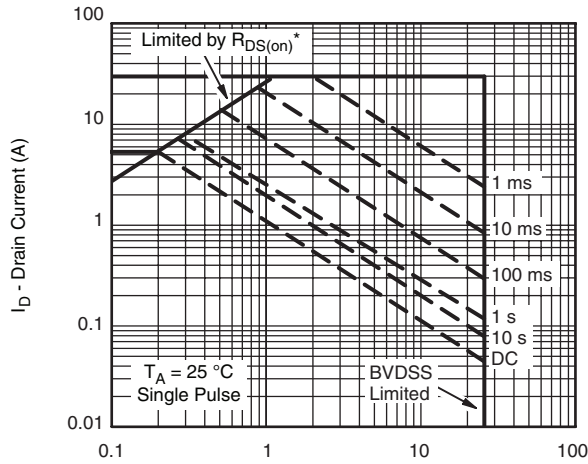
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

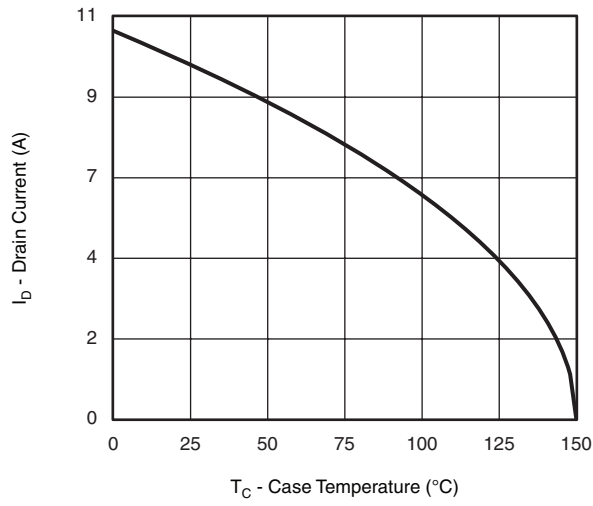


* $V_{DS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

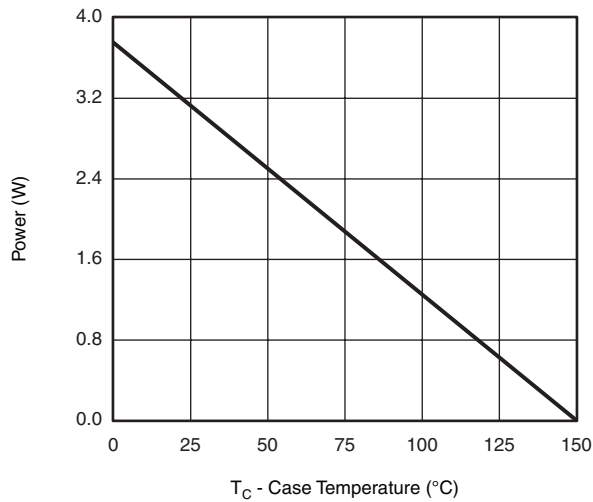
Safe Operating Area



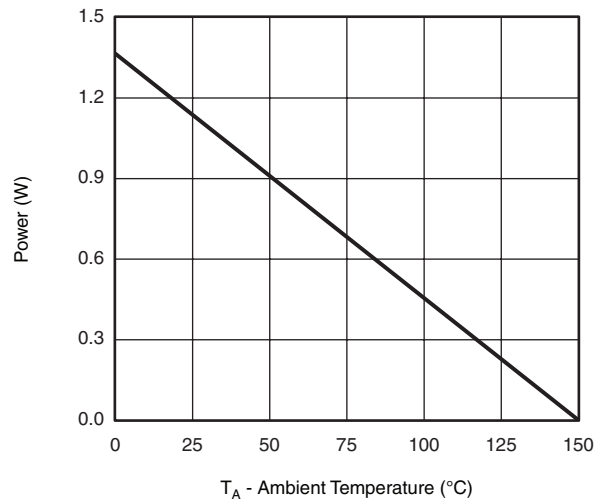
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Foot

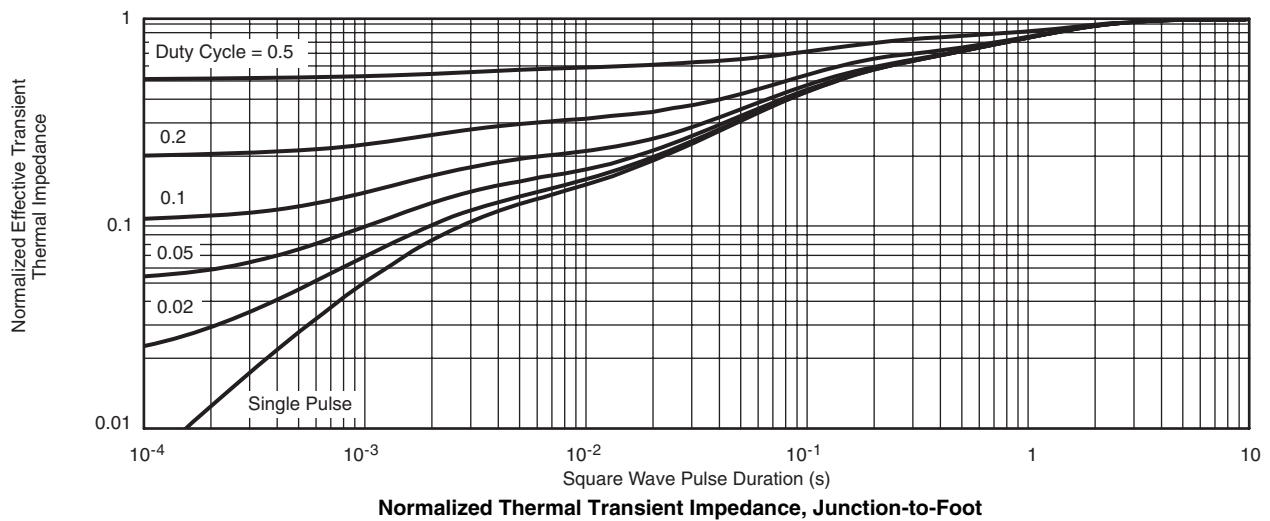
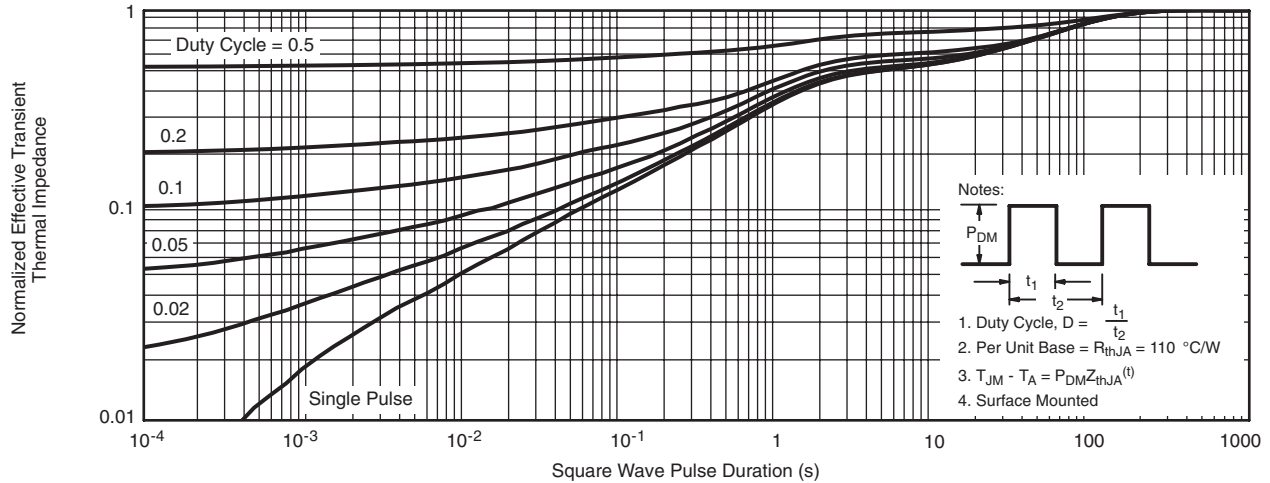


Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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