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Si4313-B1

Si4313 Low-Cost ISM Receiver

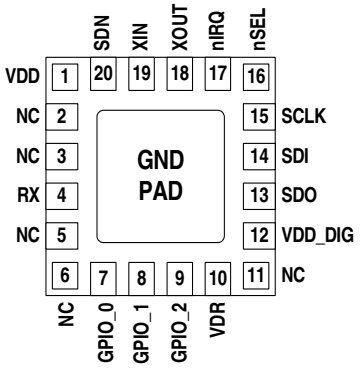
Features

- Frequency range = 240–960 MHz
- Sensitivity = –118 dBm
- Low power consumption
- Data rate = 0.2 to 128 kbps
- FSK, GFSK, and OOK modulation schemes
- Power supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Digital RSSI
- Wake-up timer
- Auto frequency calibration (AFC)
- Clear channel assessment
- Programmable RX BW 2.6–620 kHz
- Preamble detector
- RX 64 byte FIFO
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-pin QFN package
- Low BOM
- Single capacitor matching network
- Power-On-Reset (POR)
- Single-ended antenna configuration

Ordering Information:
See page 44.

Pin Assignments

Si4313



Patents pending

Applications

- Remote control
- Weather station
- Personal data logging
- Health monitors

Description

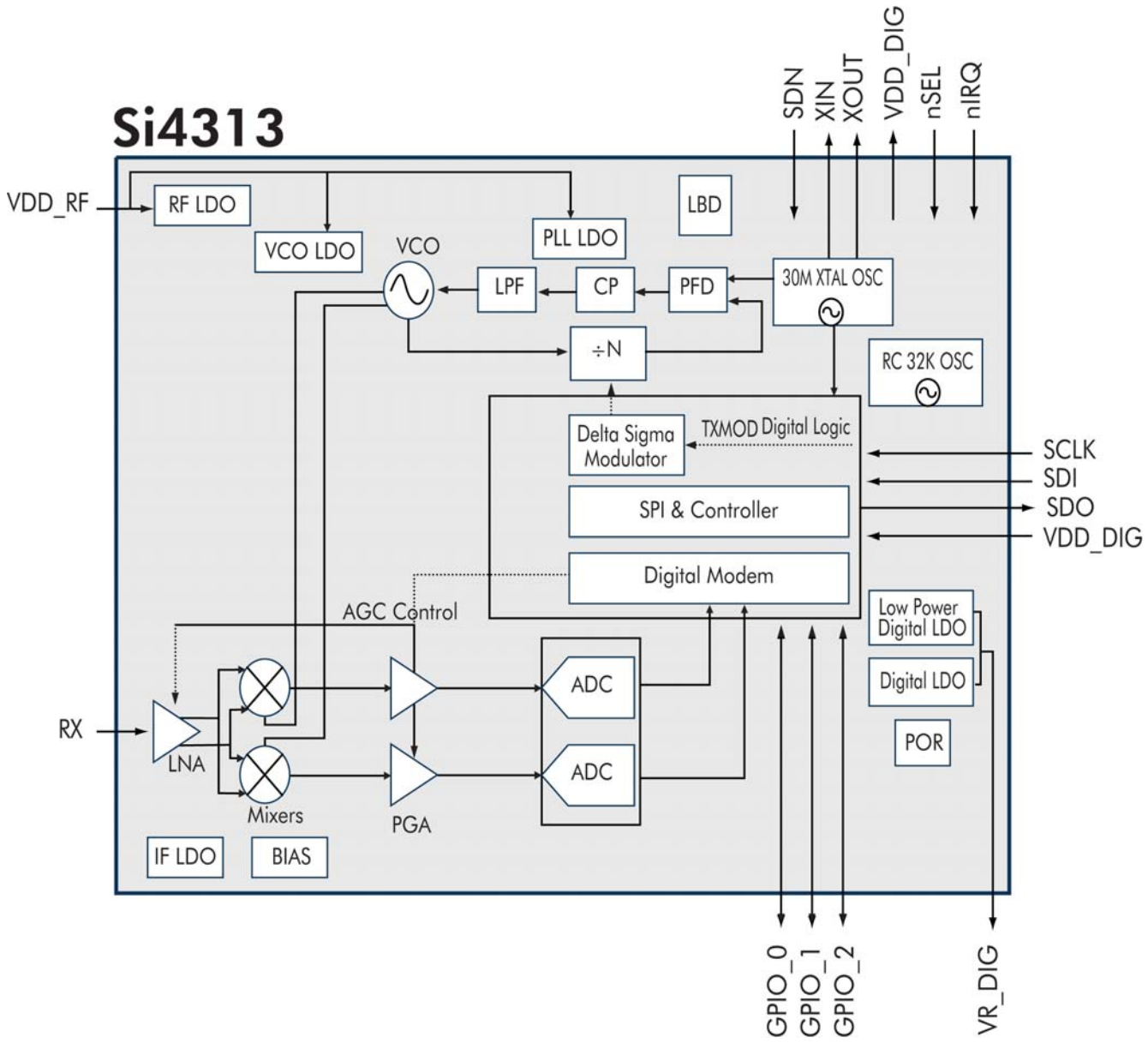
The Si4313 is a single-ended universal ISM receiver for cost-sensitive applications featuring technology developed for the EZRadioPRO® product family.

The Si4313 offers a simple, single-ended radio implementation over the 240–960 MHz frequency range. A receive sensitivity of up to –118 dBm allows for the creation of communication links with an extended range. The Si4313 offers excellent receiver performance in cost-sensitive radio applications.

The Si4313 provides designers with advanced features to enable low system power consumption by offloading a number of RF-related activities from the system MCU allowing for extended MCU sleep periods. Additional features, such as an automatic wake-up timer, 64-byte RX FIFO, and a preamble detection circuit, are available.

The Si4313's digital receive architecture features an ADC and DSP based modem that performs the radio demodulation and filtering for increased performance.

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{DD}		1.8	3.0	3.6	V
Power Saving Modes	$I_{SHUTDOWN}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF[2]	—	15	50	nA
	$I_{STANDBY}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF	—	450	800	nA
	I_{SLEEP}	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF	—	1	—	µA
	$I_{SENSOR-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	$I_{SENSOR-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	I_{READY}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled	—	800	—	µA
Tune Mode Current	I_{TUNE}	Synthesizer and regulators enabled	—	8.5	—	mA
RX Mode Current	I_{RX}		—	18.5	—	mA

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	$F_{SYNTH-LB}$	Low Band	240	—	480	MHz
	$F_{SYNTH-HB}$	High Band	480	—	960	MHz
Synthesizer Frequency Resolution[2]	F_{RES-LB}	Low Band	—	156.25	—	Hz
	F_{RES-HB}	High Band	—	312.5	—	Hz
Reference Frequency Input Level[2]	f_{REF_LV}	When using external reference signal driving XOUT pin, instead of using crystal. Measured peak-to-peak (V_{PP})	0.7	—	1.6	V
Synthesizer Settling Time[2]	t_{LOCK}	Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration	—	200	—	µs

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

Table 3. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	F_{RX}		240	—	960	MHz
RX Sensitivity	P_{RX_2}	(BER < 0.1%) (2 kbps, GFSK, BT = 0.5, Δf = ±5 kHz)[2]	—	–118	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)[2]	—	–105	—	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)[2]	—	–101	—	dBm
	P_{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, Δf = ±62.5 kHz)[1]	—	–98	—	dBm
	P_{RX_OOK}	(BER < 0.1%) (4.8 kbps, 350 kHz BW, OOK)[2]	—	–107	—	dBm
		(BER < 0.1%) (40 kbps, 400 kHz BW, OOK)[1]	—	–99	—	dBm
RX Bandwidth[2]	BW		2.6	—	620	kHz
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[2]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER <0.1%. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5, channel spacing = 150 kHz	—	–31	—	dB
±2-Ch Offset Selectivity[2]	$C/I_{2\text{-}CH}$		—	–35	—	dB
≥±3-Ch Offset Selectivity[2]	C/I3-CH		—	–40	—	dB
Blocking at 1 MHz offset[2]	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5	—	–52	—	dB
Blocking at 4 MHz offset [2]	$4M_{BLOCK}$		—	–56	—	dB
Blocking at 8 MHz offset [2]	$8M_{BLOCK}$		—	–63	—	dB
Image Rejection[2]	Im_{REJ}	IF = 937 kHz	—	–30	—	dB
Spurious Emissions[2]	P_{OB_RX1}		—	—	–54	dBm

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

Table 4. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low Battery Detector Resolution[2]	LBD_{RES}		—	50	—	mV
Low Battery Detector Conversion Time[2]	LBD_{CT}		—	250	—	µs
Microcontroller Clock Output Frequency	F_{MC}	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768 k	—	30 M	Hz
30 MHz XTAL Start-Up time	t_{30M}		—	600	—	µs
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	97	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	6	—	sec
32 kHz Accuracy using Internal RC Oscillator[2]	$32KRC_{RES}$		—	1000	—	ppm
32 kHz RC Oscillator Start-Up	t_{32kRC}		—	500	—	µs
POR Reset Time	t_{POR}		—	16	—	ms
Software Reset Time[2]	t_{soft}		—	100	—	µs

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

Table 5. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time[2]	T_{RISE}	0.1 x VDD to 0.9 x V_{DD}, C_L = 5 pF	—	—	8	ns
Fall Time[2]	T_{FALL}	0.9 x VDD to 0.1 x V_{DD}, C_L = 5 pF	—	—	8	ns
Input Capacitance[2]	C_{IN}		—	—	1	pF
Logic High Level Input Voltage[2]	V_{IH}		V_{DD}–0.6	—	—	V
Logic Low Level Input Voltage[2]	V_{IL}		—	—	0.6	V
Input Current[2]	I_{IN}	0<VIN< V_{DD}	–100	—	100	nA
Logic High Level Output Voltage[2]	V_{OH}	I_{OH}<1 mA source, V_{DD} = 1.8 V	V_{DD}–0.6	—	—	V
Logic Low Level Output Voltage[2]	V_{OL}	I_{OL}<1 mA sink, V_{DD} = 1.8 V	—	—	0.6	V

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

Table 6. GPIO Specifications (GPIO_0, GPIO_1 and GPIO_2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time[2]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = HH	—	—	8	ns
Fall Time[2]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = HH	—	—	8	ns
Input Capacitance[2]	C_{IN}		—	—	1	pF
Logic High Level Input Voltage[2]	V_{IH}		V_{DD}–0.6	—	—	V
Logic Low Level Input Voltage[2]	V_{IL}		—	—	0.6	V
Input Current[2]	I_{IN}	0<V_{IN}< V_{DD}	–100	—	100	nA
Input Current if pull-up activated[2]	I_{INP}	V_{IL} = 0 V	5	—	25	µA
Maximum Output Current[2]	I_{OMAXLL}	DRV<1:0> = LL	0.1	0.5	0.8	mA
	I_{OMAXLH}	DRV<1:0> = HL	0.9	2.3	3.5	mA
	I_{OMAXHL}	DRV<1:0> = HL	1.5	3.1	4.8	mA
	I_{OMAXHH}	DRV<1:0> = HH	1.8	3.6	5.4	mA
Logic High Level Output Voltage[2]	V_{OH}	I_{OH}< I_{Omax} source, V_{DD} = 1.8 V	V_{DD}–0.6	—	—	V
Logic Low Level Output Voltage[2]	V_{OL}	I_{OL}< I_{Omax} sink, V_{DD} = 1.8 V	—	—	0.6	V

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
Voltage on Digital Control Inputs	–0.3, V_{DD} +0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} +0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature T_A	–40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

***Note:** Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. *This is an ESD-sensitive device*.

1.1. Test Condition Definitions

1.1.1. Production Test Conditions

- TA = +25 °C
- VDD = +3.3 VDC
- Sensitivity measured at 919 MHz.
- External reference signal (XOUT) = 1.0 VPP at 30 MHz, centered around 0.8 VDC.
- Production test schematic (unless noted otherwise).
- All RF input levels refer to the pins of the Si4313 (not the RF module).

1.1.2. Qualification Test Conditions

- TA = –40 to +85 °C.
- VDD = +1.8 to +3.6 VDC.
- Based upon standard reference design test cards.
- All RF input levels refer to the pins of the Si4313 (not the RF module).

2. Functional Description

The Si4313 is an ISM wireless single-ended receiver with continuous frequency coverage over the entire 240–960 MHz band. The wide operating voltage range of 1.8–3.6 V and low current consumption make the Si4313 an ideal solution for low-cost, battery-powered applications.

The Si4313 receiver uses a low IF architecture with a digital modem that performs the signal demodulation. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A local oscillator (LO) is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency, frequency deviation, and Gaussian filtering at any frequency between 240–960 MHz.

The Si4313 is designed to work with a microcontroller, crystal, and a few passives to create a very low-cost system. Voltage regulators are integrated on-chip, which allows for a wide range of operating supply voltage conditions from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with the microcontroller. Three configurable general-purpose I/Os are also available. Minimal antenna matching is required allowing the use of a single ac coupling capacitor which simplifies the system design and lowers the solution cost.

2.1. Application Example

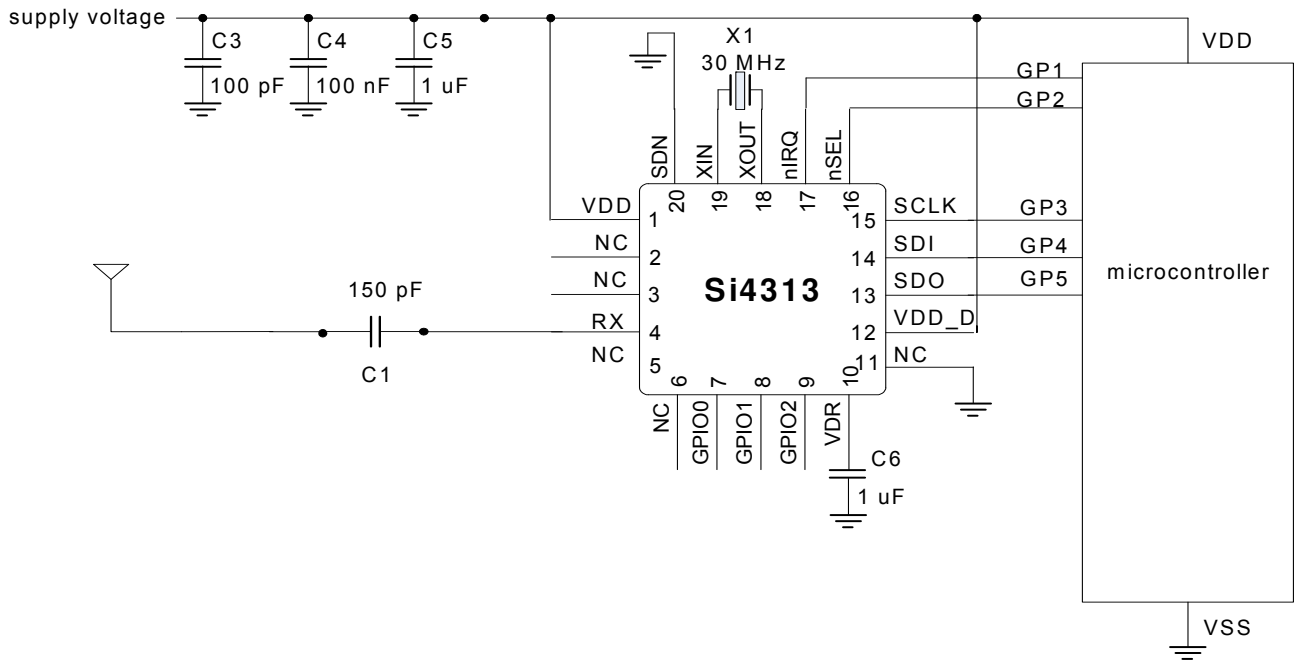


Figure 1. Application Example

2.2. Operating Modes

The Si4313 provides several operating modes, which can be used to optimize the power consumption of the receive application. Depending upon the system communication protocol, an optimal trade-off between radio wake time and power consumption can be achieved.

In general, any given operating mode may be classified as an Active mode or a Power Saving mode. Table 8 indicates which blocks are enabled (active) in each corresponding mode. With the exception of the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI. An "X" in any table cell means that the block can be independently programmed to be either ON or OFF (in that given operating mode) without noticeably impacting current consumption. The SPI block includes the SPI interface hardware and the register space. The 32 kHz OSC circuit block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor and low-battery detector.

Table 8. Operating Modes

Mode Name	Circuit Blocks							
	Digital LDC	SPI	32 kHz OSC	AUX	30 MHz XTAL	PLL	RX	I_{VDD}
Shutdown	OFF register contents lost	OFF	OFF	OFF	OFF	OFF	OFF	15 nA
Standby	ON register contents retained	OFF	OFF	OFF	OFF	OFF	OFF	450 nA
Sleep		ON	ON	X	OFF	OFF	OFF	1 µA
Sensor		ON	X	ON	OFF	OFF	OFF	1 µA
Ready		ON	X	X	ON	OFF	OFF	800 µA
Tuning		ON	X	X	ON	ON	OFF	8.5 mA
Receive		ON	X	X	ON	ON	ON	18.5 mA

3. Controller Interface

3.1. Serial Peripheral Interface

The Si4313 communicates with the host MCU over a standard three-wire SPI interface: SCLK, SDI, and nSEL. The host MCU can read data from the device on the SDO output pin. An SPI transaction is a 16-bit sequence which consists of a Read-Write (R/W) select bit followed by a 7-bit address field (ADDR) and an 8-bit data field (DATA). The 7-bit address field supports reading from or writing to one of the 128 8-bit control registers. The R/W select bit determines whether the SPI transaction is a read or write transaction. If R/W = 1, it signifies a WRITE transaction, while R/W = 0 signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4313 every eight clock cycles. Timing parameters are shown in Table 9. The SCLK rate is flexible with a maximum rate of 10 MHz.

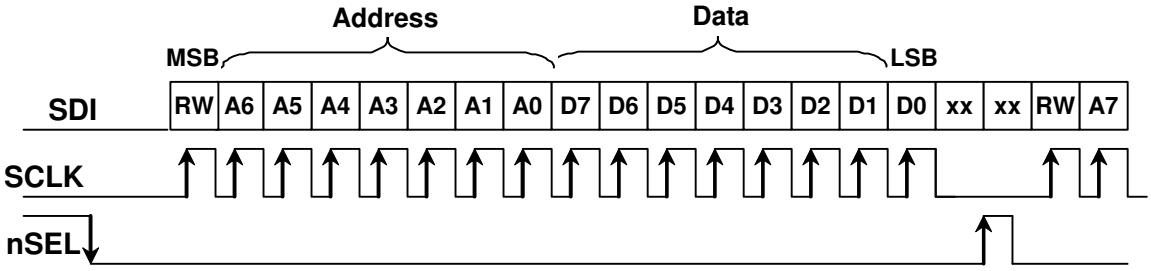
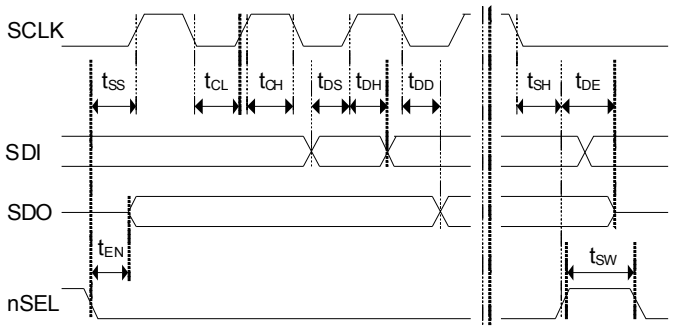


Figure 2. SPI Timing

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (nsec)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

To read back data from the Si4313, the R/W bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored on the SDI pin when R/W = 0. The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 3. After the READ function is completed, the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high, the SDO output pin will be pulled high by internal pull-up.

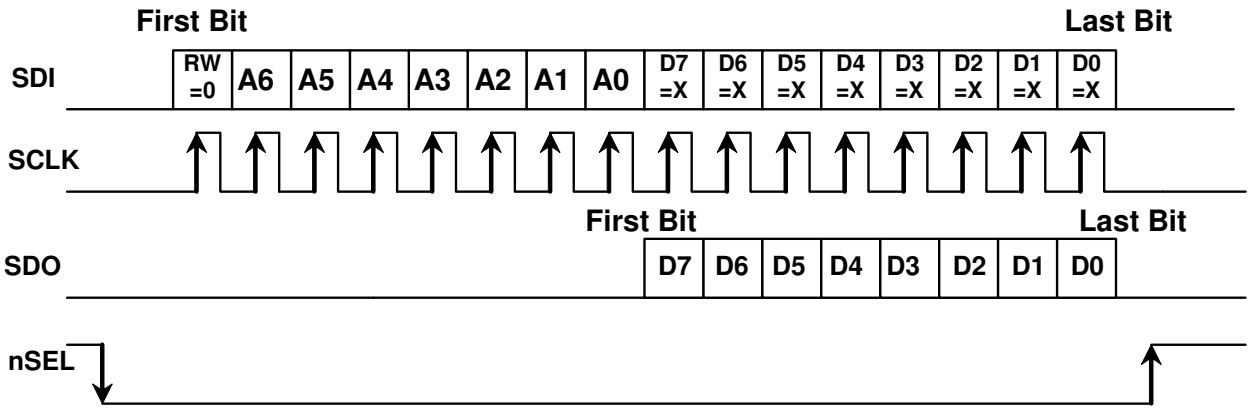


Figure 3. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode, which allows for reading/writing sequential registers without having to resend the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An example burst write transaction is shown in Figure 4, and a burst read is shown in Figure 5. As long as nSEL is held low, input data will be latched into the Si4313 every eight SCLK cycles.

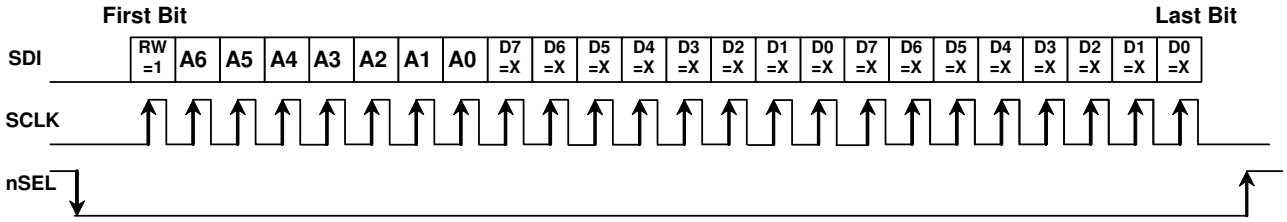


Figure 4. SPI timing—Burst Write Mode

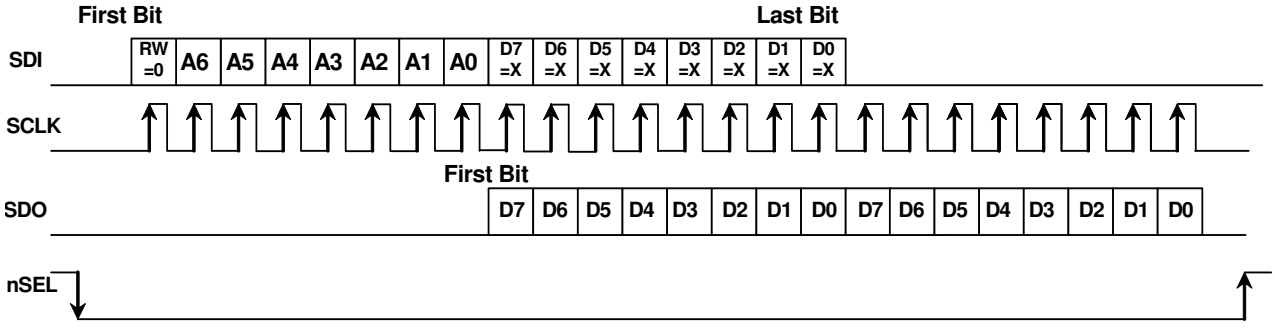


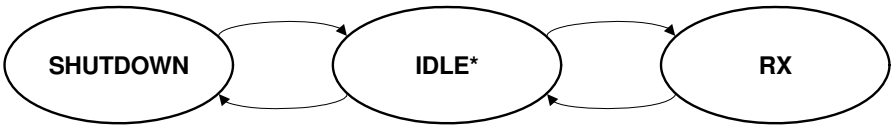
Figure 5. SPI timing—Burst Read Mode

3.2. Operating Mode Control

There are three primary states in the Si4313 radio state machine: SHUTDOWN, IDLE, and RECEIVE. The SHUTDOWN state is designed to completely shut down the radio to minimize current consumption. There are five different configurations/options for the IDLE state that can be selected to optimize the Si4313 for the application requirements.

"Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected. The RX state may be reached automatically from any of the IDLE states by setting the rxon bit in "Register 07h. Operating Mode and Function Control 1". Table 10 shows each of the operating modes with the time required to reach RX mode as well as the current consumption of each mode.

The Si4313 includes a low-power digital regulated supply (LPLDO), which is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the digital modem, crystal oscillator, SPI, and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.



*Five different options for IDLE

Figure 6. State Machine Diagram

Table 10. Operating Modes Response Time

State Mode	Response Time to RX	Current in State/Mode (µA)
Shut Down State	16.8 ms	15 nA
Idle States		
Standby Mode	800 µs	450 nA
Sleep Mode	800 µs	1 µA
Sensor Mode	800 µs	1 µA
Ready Mode	200 µs	800 µA
Tune Mode	200 µs	8.5 mA
RX State	N/A	18.5 mA

3.2.1. SHUTDOWN State

The SHUTDOWN state is the lowest current consumption state of the device with nominally less than 15 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

3.2.2. IDLE State

There are fivefour different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX/RX mode. This tradeoff is shown in Table 10. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption of the five IDLE states with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The STANDBY mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "8.4. Wake-Up Timer and 32 kHz Clock Source" on page 36 for more information on the Wake-Up-Timer. SLEEP mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.3. SENSOR Mode

In SENSOR mode the Low Battery Detector may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 in "Register 07h. Operating Mode and Function Control 1". See "8.3. Low Battery Detector" on page 34 for more information on this feature. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TXRX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time. READY mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled in “Register 62h. Crystal Oscillator Control and Test.” To exit READY mode, bufovr (bit 1) of this register must be set back to 0.

3.2.2.5. TUNE Mode

In TUNE mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TXRX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for frequency hopping spread spectrum systems (FHSS). TUNE mode is entered by setting pllon = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

3.2.3. RX State

The RX state may be entered from any of the Idle modes when the rxon bit is set to 1 in 'Register 07h. Operating Mode and Function Control 1'. A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the main digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by internal timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").
5. Wait until PLL settles to required receive frequency (controlled by internal timer).
6. Enable receive circuits: LNA, mixers, and ADC.
7. Calibrate ADC (RC calibration).
8. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

3.2.4. Device Status

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
02	R	Device Status	ffovfl	ffunfl	rxffem	Reserved	freqerr		cps[1]	cps[2]	—

The operational status of the Si4313 can be read from the Device Status register, 'Register 02h'

3.3. Interrupts

The Si4313 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h-04h) containing the active Interrupt Status bit. The nIRQ output signal will then be reset until the next change in status is detected. The interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h-06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event then it will not trigger the nIRQ pin, but the status may still be read at anytime in the Interrupt Status registers.

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
03	R	Interrupt Status 1	ifferr	Reserved	Reserved	irxffafull	iext	Reserved	Reserved	Reserved	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	Reserved	Reserved	enrxffafull	enext	Reserved	Reserved	Reserved	00h
06	R/W	Interrupt Enable 1	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h

3.4. System Timing

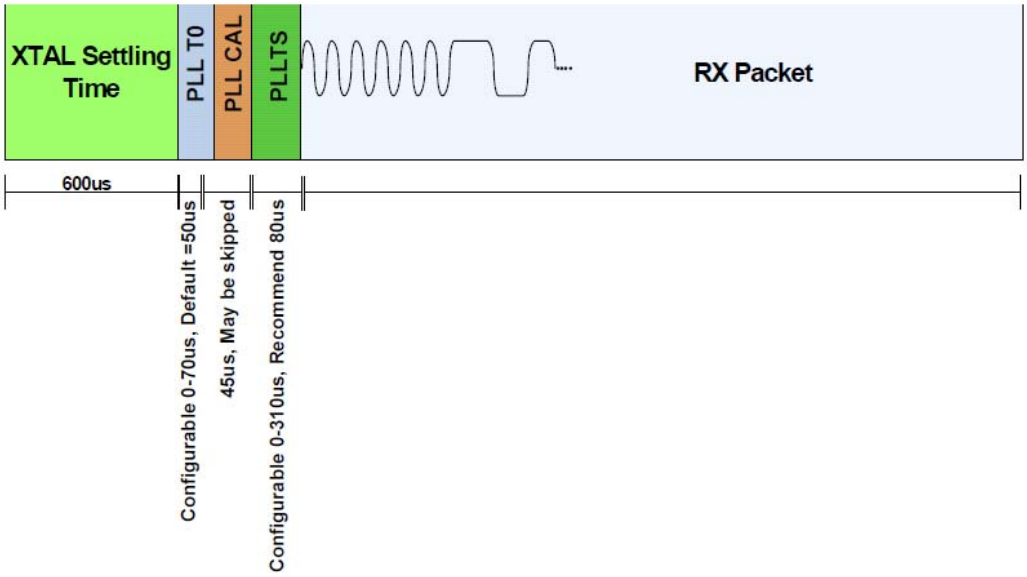


Figure 7. RX Timing

The VCO will automatically calibrate at every frequency change or power-up. The PLL T0 time is to allow for bias settling of the VCO. The PLL TS time is for the settling time of the PLL, which has a default setting of 100 µs. The total time for PLL T0, PLL CAL, and PLL TS under all conditions is 200 µs. In certain applications, the PLL T0 time and the PLL CAL may be skipped for faster turnaround time. Contact applications support if faster turnaround time is desired.

3.5. Frequency Control

To calculate the necessary frequency register settings, use the Silicon Labs' Wireless Design Suite (WDS) or Excel Calculator available from the product web page. These methods offer a simple, quick interface to determine the correct settings based on the application requirement.

Add	R/W	Function/Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
75	R/W	Frequency Band Select		sbsel	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h

3.5.1. Automatic State Transition for Frequency Change

If registers 79h or 7Ah are changed in RX mode, the state machine will automatically transition the chip back to tune and change the frequency. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System. In turn, this reduces microcontroller activity, thereby reducing current consumption.

3.5.2. Frequency Offset Adjustment

When the AFC is disabled, the frequency offset can be adjusted manually by fo[9:0] in registers 73h and 74h. The frequency offset adjustment and the AFC are both implemented by shifting the Synthesizer Local Oscillator frequency. This register is a signed register; so, in order to get a negative offset, it is necessary to take the twos

complement of the positive offset number. The offset can be calculated with the following formula:

$$\text{Desired Offset} = 156.25\ \text{Hz} \times (\text{hbsel} + 1) \times \text{fo}[9:0]$$

$$\text{fo}[9:0] = \frac{\text{Desired Offset}}{156.25\ \text{Hz} \times (\text{hbsel} + 1)}$$

The adjustment range is ±160 kHz in high band and ±80 kHz in low band. For example, to compute an offset of +50 kHz in high band mode, fo[9:0] should be set to 0A0h. For an offset of –50 kHz in high band mode, the fo[9:0] register should be set to 360h.

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
73	R/W	Frequency Offset	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	fo[9]	fo[8]	00h

3.5.3. Auto Frequency Control (AFC)

All AFC settings can be easily obtained from the excel settings calculator or by using the WDS Chip Configurator. This is the recommended method to program all AFC settings. This section is intended to describe the operation of the AFC in more detail to help understand the trade-offs of using AFC.The receiver supports automatic frequency control (AFC) to compensate for frequency differences between the transmitter and receiver reference frequencies. These differences can be caused by the absolute accuracy and temperature dependencies of the reference crystals. Due to frequency offset compensation in the modem, the receiver is tolerant to frequency offsets up to ±0.25 times the IF bandwidth when the AFC is disabled. When the AFC is enabled, the received signal will be centered in the pass-band of the IF filter, providing optimal sensitivity and selectivity over a wider range of frequency offsets up to ±0.35 times the IF bandwidth. The trade-off of receiver sensitivity (at 1% PER) versus carrier offset and the impact of AFC are illustrated in Figure 8.

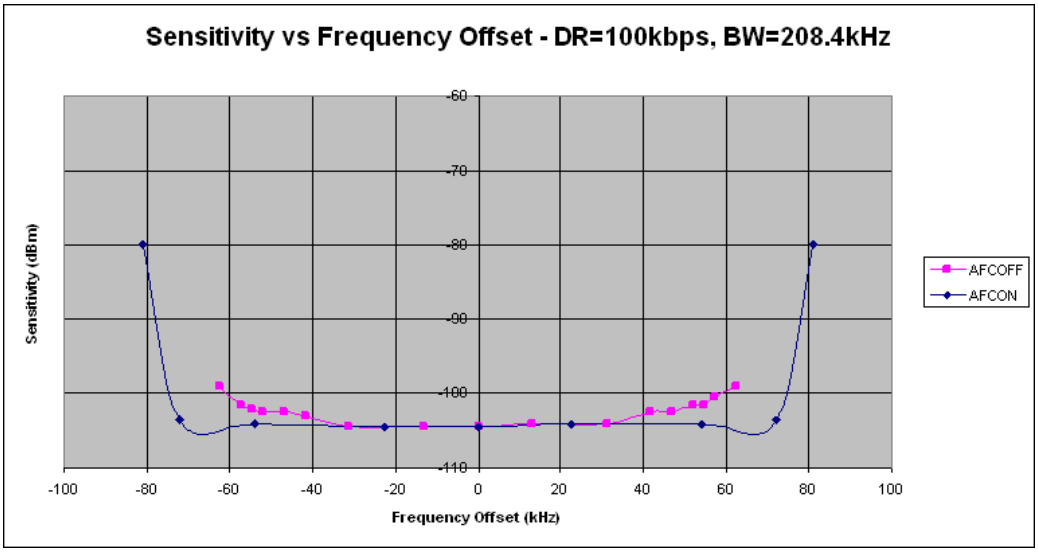


Figure 8. Sensitivity at 1% PER vs. Carrier Frequency Offset

When AFC is enabled, the preamble length needs to be long enough to settle the AFC. In general, one byte of preamble is sufficient to settle the AFC. Disabling the AFC allows the preamble to be shortened from 40 bits to 32 bits. Note that with the AFC disabled, the preamble length must still be long enough to settle the receiver and to detect the preamble (see "6.2. Preamble Length" on page 30). The AFC corrects the detected frequency offset by changing the frequency of the Fractional-N PLL. When the preamble is detected, the AFC will freeze for the remainder of the packet. The AFC loop includes a bandwidth limiting mechanism improving the rejection of out of band signals. When the AFC loop is enabled, its pull-in-range is determined by the bandwidth limiter value

(AFCLimiter) which is located in register 2Ah.

AFC_pull_in_range = ±AFCLimiter[7:0] x (hbsel+1) x 625 Hz

The AFC Limiter register is an unsigned register and its value can be obtained from the EZRadioPRO Register Calculator spreadsheet or from WDS.

The amount of error correction feedback to the Fractional-N PLL before the preamble is detected is controlled from afcgearh[2:0]. The default value 000 relates to a feedback of 100% from the measured frequency error and is advised for most applications. Every bit added will half the feedback but will require a longer preamble to settle.

The AFC operates as follows. The frequency error of the incoming signal is measured over a period of two bit times, after which it corrects the local oscillator via the Fractional-N PLL. After this correction, some time is allowed to settle the Fractional-N PLL to the new frequency before the next frequency error is measured. The duration of the AFC cycle before the preamble is detected can be programmed with shwait[2:0]. It is advised to use the default value 001, which sets the AFC cycle to 4 bit times (2 for measurement and 2 for settling).

The AFC correction value may be read from register 2Bh. The value read can be converted to kHz with the following formula:

AFC Correction = 156.25Hz x (hbsel +1) x afc_corr[7: 0]

	Frequency Correction	
	RX	**TX**
AFC disabled	Freq Offset Register	Freq Offset Register
AFC enabled	AFC	Freq Offset Register

4. Modulation Options

All modulation options are programmed in "Register 71h. Modulation Mode Control 2."

4.1. Modulation Type

The Si4313 can be configured to support three alternative modulation options: Gaussian Frequency Shift Keying (GFSK), Frequency Shift Keying (FSK), and On-Off Keying (OOK). The type of modulation is selected with the modtyp[1:0] bits in "Register 71h. Modulation Mode Control 2".

modtyp[1:0]	Modulation Source
00	Reserved
01	OOK
10	FSK
11	GFSK

4.2. FIFO Mode

In FIFO mode, the integrated FIFO is used to receive the data. The FIFO is accessed via "Register 7Fh. FIFO Access" with burst read capability. The FIFO may be configured specific to the application packet size, etc. (see "6. Data Handling" on page 29 for further information).

In RX mode, the preamble detection threshold and sync needs to be programmed so that the modem knows when to start filling data into the FIFO. When the FIFO is being used, the data being loaded into or out of the FIFO can still be observed by configuring the GPIO, which can be useful during development.

4.3. Direct Mode

In many system implementations, it may not be desirable to use a FIFO, and, for this scenario, a “Direct Mode”, which bypasses the FIFOs entirely, is provided. In Direct Mode, the RX data and RX clock are programmed directly to the GPIO and used by the microcontroller to process the data without using the FIFO. In direct mode, the preamble detection threshold (Reg 35h) still needs to be programmed. Once the preamble is detected, algorithms internal to the modem change. It is not required that the sync be programmed when direct mode is used for RX.

4.3.1. Direct Mode using SPI or nIRQ Pins

In certain applications, it may be desirable to minimize the connections to the microcontroller or to preserve the GPIOs for other uses. For these cases, it is possible to use the SPI pins and nIRQ as the modulation clock and data. The SDO pin can be configured to be the data clock by programming trclk = 10. If the nSEL pin is LOW, then the function of the pin will be SPI data output. If the pin is high and trclk is 10, then, during the RX mode, the data clock will be available on the SDO pin. If trclk[1:0] is set to 11 and no interrupts are enabled in registers 05 or 06h, the nIRQ pin can also be used as the RX data clock.

The SDI pin can be configured to be the data source for RX if dtmod = 01. Similarly, if nSEL is LOW, the pin will function as SPI data-in; if nSEL is HIGH, it will be the received demodulated data.