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Si4322

Si4322 UNIVERSAL ISM BAND FSK RECEIVER

Features

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input
- Programmable baseband bandwidth (135 to 400 kHz)
- Analog and digital RSSI
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery

- RX pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 64-bit RX data FIFO
- Autonomous low duty-cycle mode down to 0.006%
- Standard 10 MHz crystal reference
- Wake-up timer
- Low battery detector
- 2.2 to 3.8 V supply voltage
- Low power consumption
- Low standby current (typical 0.3 µA)

Pin Assignments

SDI	1	16 VDI
SCK	2	15 ARSSI
nSEL	3	14 VDD
SDO/FFIT	4	Si4322 13 IN1
nIRQ	5	12 IN2
DATA/nFFS	6	11 VSS
DCLK/FFIT/CFIL	7	10 nRES
CLK	8	9 XTL/REF

Patents pending

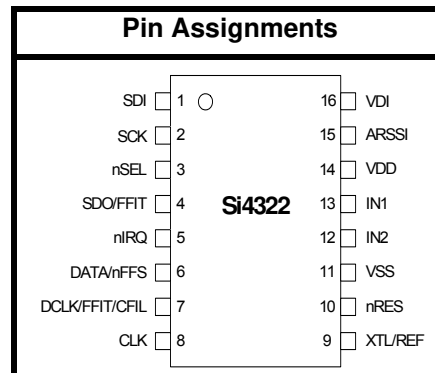This data sheet refers to version A1

Applications

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control

- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

Description

Silicon Labs' Si4322 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with Silicon Labs' FSK transmitters, the Si4322 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering capacitors are needed for operation.

The Si4322 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator. The receiver employs zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The Si4322 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

Si4322

Functional Block Diagram

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1. Electrical Specifications

Table 1. DC Characteristics

(Test conditions: T_{OP} = 25 °C; V_{DD} = 2.7 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{dd}		—	12	14	mA
Standby Current	I_{pd}	all blocks disabled	—	0.3	—	µA
Low Battery Voltage Detector and Wake-Up Timer Current[1]	I_{lb}		—	—	5	µA
Idle Current	I_x	crystal oscillator is on[1]	—	0.5	—	mA
Low Battery Detection Threshold	V_{lb}	programmable in 0.1 V steps	2.0		3.5	V
Low Battery Detection Accuracy	V_{lba}		—	±2.5	—	%
V_{dd} Threshold Required to Generate a POR	V_{POR}		—	1.5	—	V
POR Hysteresis	$V_{PORhyst}$	larger glitches on the V_{dd} generate a POR even above the threshold V_{POR}[2]	—	—	0.6	V
V_{DD} Slew Rate	SR_{Vdd}	for proper POR generation	0.1	—	—	V/ms
Digital Input Low Level	V_{il}		—	—	0.3 x V_{DD}	V
Digital Input High Level	V_{ih}		0.7 x V_{DD}	—	—	V
Digital Input Current	I_{il}	V_{IL} = 0 V	–1	—	1	µA
Digital Input Current	I_{ih}	V_{IH} = V_{DD}, V_{DD} = 3.8 V	–1	—	1	µA
Digital Output Low Level	V_{ol}	I_{OL} = 2 mA		—	0.4	V
Digital Output High Level	V_{oh}	I_{oh} = –2 mA	V_{DD} – 0.4	—	—	V

Notes:
1. Measured with disabled clock output buffer.
2. For detailed information see "13. Reset modes" on page 34.

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Table 2. AC Characteristics

(Test conditions: T_{OP} = 25 °C; V_{DD} = 2.7 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Receiver Frequency	f_{LO}	433 MHz band, 10 kHz resolution 868 MHz band, 20 kHz resolution 915 MHz band, 20 kHz resolution	400.96 801.92 881.92	— — —	439.03 878.06 958.06	MHz
Receiver Bandwidth	BW	Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	120 180 240 300 360	135 200 270 350 400	150 225 300 375 450	kHz
FSK Bit Rate	BR	With internal digital filters	—	—	115.2	kbps
FSK Bit Rate	BRA	With analog filter		—	256	kbps
Receiver Sensitivity	P_{min}	BER 10^{-3}, BW = 135 kHz, BR = 1.2 kbps, δf_{FSK} = 60 kHz	—	−109	—	dBm
AFC Locking Range	AFC_{range}	δf_{FSK}: FSK deviation in the received signal	—	0.8 x δf_{FSK}	—	
Input IP3	$IIP3_{inh}$	In band interferers	—	−21	—	dBm
Input IP3	$IIP3_{outh}$	Out of band interferers: f − f_{LO} > 4 MHz	—	−18	—	dBm
Co-Channel Rejection	CCR	BER = 10^{-2} with continuous wave interferer in the channel	—	−4	—	dB
Blocking Ratio with CW Interferer	BR_{2MHz}	BER = 10^{-2}, BW = 135 kHz, BR = 9.6 kbps, δf_{FSK} = 60 kHz, interferer offset 2 MHz	—	54	—	dB
	BR_{10MHz}	Same as above, interferer offset 10 MHz	—	59	—	dB
Maximum Input Power	P_{max}	LNA: maximum gain	0	—	—	dBm
RF Input Impedance Real Part (differential)[1]	R_{in}	LNA gain (0, −12 dB) LNA gain (−6, −18 dB)	— —	250 500	— —	Ω
RF Input Capacitance (differential)[1]	C_{in}		—	1	—	pF
RSSI Accuracy	RS_a		—	±5	—	dB
RSSI Range	RS_r		—	46	—	dB

Notes:
1. See matching circuit parameters and antenna design guide for information, and Application Notes available from http://www.silabs.com.
2. Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.
3. During the Power-On Reset period, commands are not accepted by the chip. In case of software reset, (see "13. Reset modes" on page 34) the reset timeout is 0.25 ms typical.
4. The crystal oscillator start up time strongly depends on the capacitance seen by the oscillator. Low capacitance and low ESR crystal is recommended with low parasitic PCB layout design.
5. Auto-calibration can be turned off.

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Table 2. AC Characteristics (Continued)
(Test conditions: T_{OP} = 25 °C; V_{DD} = 2.7 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Filter Capacitance for ARSSI	C_{ARSSI}		1	—	—	nF
DRSSI Programmable Level Steps	RS_{step}		—	6	—	dB
DRSSI Response Time	RS_{resp}	Until the DRSSI goes high after the input signal exceeds the pre-programmed limit, C_{ARRSI} = 5 nF	—	500	—	µs
PLL Reference Frequency	f_{ref}	Note 2	9	10	11	MHz
PLL Lock Time	t_{lock}	Frequency error < 1 kHz after 1 MHz step	—	30	—	µs
PLL Startup Time	t_{st1P}	Initial calibration after power-up with running crystal oscillator	—	—	500	µs
PLL Startup Time	t_{st2P}	Recalibration after receiver chain enable with running crystal oscillator	—	—	60	µs
Crystal Load Capacitance, see Crystal Selection Guide	C_{xl}	Programmable in 0.5 pF steps, tolerance ±10%	8.5	—	16	pF
Internal POR Pulse Width[3]	t_{POR}	After V_{DD} has reached 90% of final value	—	50	100	ms
Crystal Oscillator Startup Time	t_{sx}	Crystal ESR < 50 Ω, C_L = 16pF[4]	—	—	5	ms
Wake-Up Timer Clock Period	t_{PBt}	Calibrated every 30 seconds[5]	0.995	1	1.005	ms
Programmable Wake-Up Time	$t_{wake-up}$		1	—	8.4×10^6	ms
Digital Input Capacitance	C_{inD}		—	—	2	pF
Digital Output Rise/Fall Time	t_r, t_f	15 pF pure capacitive load	—	—	10	ns
Clock Output Rise/Fall Time	t_{rckout}, t_{fckout}	10 pF pure capacitive load	—	—	15	ns
Slow Clock Frequency	$f_{ckoutslow}$	Tolerance ± 1 kHz	—	32	—	kHz

Notes:
1. See matching circuit parameters and antenna design guide for information, and Application Notes available from http://www.silabs.com.
2. Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.
3. During the Power-On Reset period, commands are not accepted by the chip. In case of software reset, (see "13. Reset modes" on page 34) the reset timeout is 0.25 ms typical.
4. The crystal oscillator start up time strongly depends on the capacitance seen by the oscillator. Low capacitance and low ESR crystal is recommended with low parasitic PCB layout design.
5. Auto-calibration can be turned off.

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Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Supply Voltage	V_{DD}	2.2	—	3.8	V
Ambient Operating Temperature	T_{OP}	–40	—	+85	^{o}C

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Positive Supply Voltage	V_{DD}	–0.5	6.0	V
Voltage on Any Pin	V_{IN}	–0.5	V_{dd}+0.5	V
Input Current into Any Pin Except VDD and VSS	I_{IN}	–25	25	mA
Electrostatic Discharge with Human Body Model	ESD	—	1000	V
Storage Temperature	T_{ST}	–55	125	^{o}C
Lead Temperature (soldering, max 10 s)	T_{LD}	—	260	^{o}C

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2. Typical Application Schematic
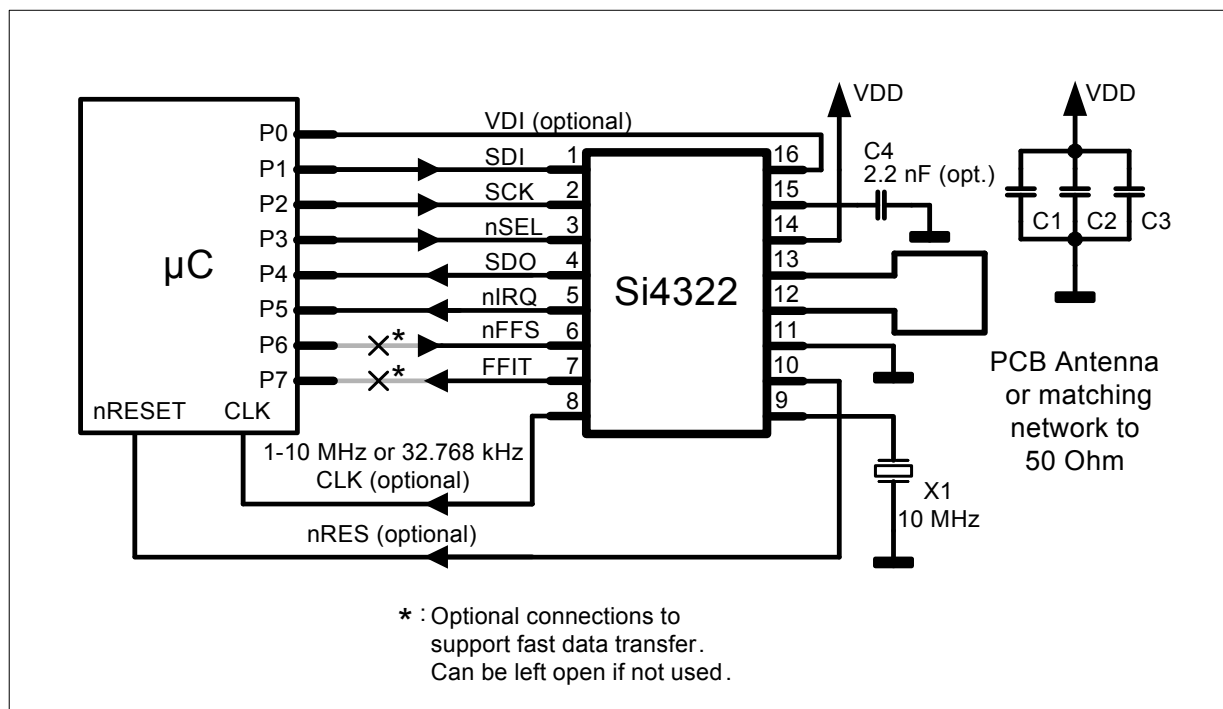
2.1. Recommended Supply Decoupling Capacitor Values

C2 and C3 should be 0603 size ceramic capacitors to achieve the best supply decoupling.

Band [MHz]	C1	C2	C3
433	2.2 µF	10 nF	220 pF
868	2.2 µF	10 nF	47 pF
915	2.2 µF	10 nF	33 pF

Property	C1	C2	C3
SMD size	A	0603	0603
Dielectric	Tantalum	Ceramic	Ceramic

Table 5. Pin Function vs. Operation Mode

Bit setting fe	Function	Pin 6	Pin 7
0	Receiver FIFO disabled	RX data output	RX data clock output
1	Receiver FIFO enabled	nFFS input (RX data FIFO can be accessed)	FFIT output
Note: The fe bit can be found in the "5.14. FIFO Settings Command" on page 25.			

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3. Internal Pin Connections

Pin	Name	Internal Connection
1	SDI	
2	SCK	
3	nSEL	
4	SDO / FFIT	
5	nIRQ	
6	DATA / nFFS	
7	DCLK / FFIT / CFIL	
8	CLK	

Pin	Name	Internal Connection
9	XTL / REF	
10	nRES	
11	VSS	
12	IN2	
13	IN1	
14	VDD	
15	ARSSI	
16	VDI	

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4. Functional Description

The Si4322 FSK receiver is the counterpart of Silicon Labs' Si4022 FSK transmitter. It covers the unlicensed frequency bands at 433, 868 and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The receiver employs zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The Si4322 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

4.1. PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

4.2. LNA

The LNA has 250 Ω input impedance, which suits to the recommended antennas. (See Application Notes available from www.silabs.com.)

If the RF input of the chip is connected to 50 Ω devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain can be selected (0, –6, –12, –18 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

4.3. Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements.

The filter structure is a 7th order Butterworth low-pass with 40 dB suppression at 2 x BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 15 kHz.
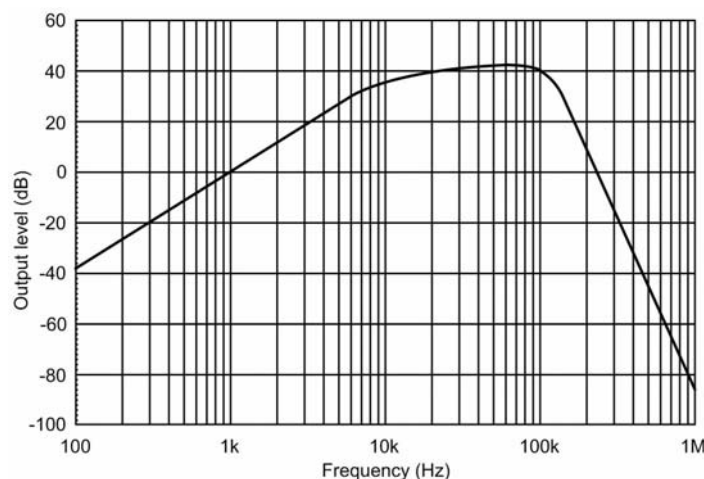
Figure 1. Full Baseband Amplifier Transfer Function, BW = 135 kHz

4.4. Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter followed by a Schmitt-trigger (St). The resistor (10k) and the Schmitt-trigger (St) are integrated on the chip. The filter capacitor should be connected externally, its value should be chosen according to the actual bit rate. In this mode, the receiver can handle up to 256 kbps data rate. When the analog filter is selected, the FIFO cannot be used and clock is not provided for the demodulated data.

Digital operation: The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode, there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock, the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, and then automatically switches to slow mode after locking.

Only the data filter and the clock recovery use the bit rate clock. Therefore, in analog mode, there is no need for setting the correct bit rate.

4.5. Data Validity Blocks

4.5.1. RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.
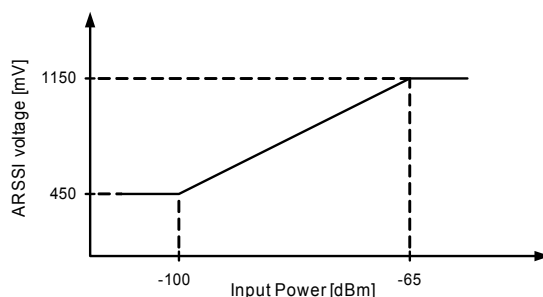

Figure 2. Typical Analog ARSSI Voltage vs. RF Input Power

4.5.2. DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive 0→1 and 1→0 transitions during a single bit period. The programmable DQD parameter defines a threshold for this counter. If the counter result exceeds this parameter, then DQD output indicates good FSK signal quality. Using this method, it is possible to "forecast" the probability of BER degradation. In cases when the deviation is close to the bit rate, there should be four transitions during a single one-bit period in the I/Q signals. As the bit rate decreases in comparison to the deviation, more and more transitions will happen during a bit period.

4.5.3. AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of the following:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e., increased sensitivity)
- higher data rate

4.6. Crystal Oscillator and Microcontroller Clock Output

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this data sheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. In normal operation, it is divided from the reference 10 MHz. During sleep mode, a low frequency (typical 32 kHz) output clock signal can be switched on, which is provided by a low-power RC oscillator.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the "5.3. Configuration Setting Command" on page 16, the chip provides a programmable number (default is 512) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode.

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4.7. Low Battery Voltage Detector

The low battery detector circuit periodically monitors (typ. 8 ms) the supply voltage and generates an interrupt if it falls below a programmable threshold level.

4.8. Wake-Up Timer

The wake-up timer has very low current consumption (5 µA max) and can be programmed from 1 ms to several hours.

It calibrates itself to the crystal oscillator at every startup and then at every 30 seconds with an accuracy of ±0.5%. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing. The periodic auto-calibration feature can be turned off.

4.9. Event Handling

In order to minimize current consumption, the receiver supports sleep mode. Active mode can be initiated by setting the *ex* or *en* bits (in "5.3. Configuration Setting Command" on page 16 or "5.5. Receiver Setting Command" on page 18).

The Si4322 generates an interrupt signal on several events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up). This signal can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

4.10. Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 64-bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the *fe* bit to 1 in the "5.14. FIFO Settings Command" on page 25. During FIFO read the crystal oscillator must be ON.

5. Control Interface

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g., bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. Special care must be taken when the microcontroller's built-in hardware serial port is used. If the port cannot be switched to 16-bit mode then a separate I/O line should be used to control the nSEL pin to ensure the low level during the whole duration of the command or a software serial control interface should be implemented. The Power On Reset (POR) circuit sets default values in all control registers.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

5.1. Timing Specification

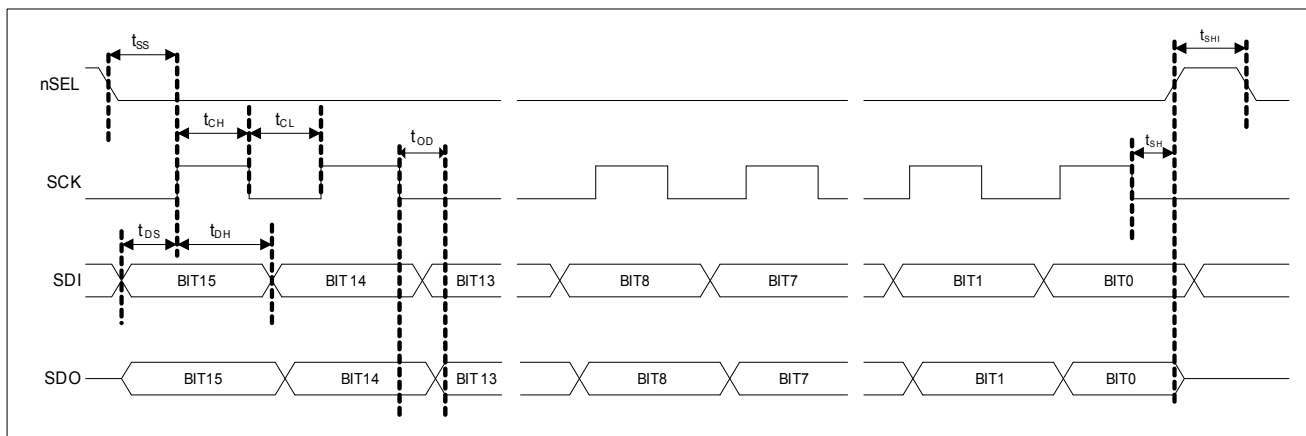| Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Figure 3. Timing Diagram

5.2. Control Commands

	Control Word	Related Parameters/Functions	Related Control Bits
1	Configuration Setting Command	Receiving band, low battery detector, wake-up timer, crystal oscillator, load capacitance, baseband filter bandwidth, clock output buffer	*b1* to *b0*, *eb*, *et*, *ex*, *x3* to *x0*, *i2* to *i0*, *dc*
2	Frequency Setting Command	Frequency of the local oscillator	*f11* to *f0*
3	Receiver Setting Command	VDI source, LNA gain, RSSI threshold, enable receiver	*d1* to *d0*, *g1* to *g0*, *r2* to *r0*, *en*
4	Synchron Pattern Command	Synchron pattern	*b7* to *b0*
5	Wake-up Timer Command	Wake-up time period	*r3* to *r0*, *m7* to *m0*
6	Extended Wake-up Timer Command	Wake-up time period extended adjustment	*c1* to *c0*, *m13* to *m8*
7	Low Duty-Cycle Command	Enable and set low duty-cycle mode	*d6* to *d0*, *enldc*
8	Low Battery Detector and Clock Divider Command	Microcontroller clock division ratio, low frequency oscillator enable, LBD threshold voltage	*cd2* to *cd0*, *elfc*, *t3* to *t0*
9	AFC Control Command	AFC parameters	*a1* to *a0*, *rl1* to *rl0*, *st*, *fi*, *oe*, *aen*
10	Data Filter Command	Clock recovery parameters, auto-sleep mode, data filter type, auto wake-up, DQD threshold	*al*, *ml*, *dsfi*, *sf*, *ewi*, *f2* to *f0*
11	Data Rate Command	Bit rate	*cs*, *r6* to *r0*
12	FIFO Settings Command	FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable	*f3* to *f0*, *s1* to *s0*, *ff*, *fe*
13	Extended Features Command	Clock tail, wake-up auto calibration, PLL bandwidth, long FIFO IT level	*ctls*, *dcal*, *bw1* to *bw0*, *f5* to *f4*
14	Status Read Command	Receiver status read	

Note: In the following tables the POR column shows the default values of the command registers after power-on.

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Table 6. Control Register Default Values

	Control Register	Power-On Reset Value
1	Configuration Setting Command	928Ah
2	Frequency Setting Command	AD57h
3	Receiver Setting Command	C080h
4	Synchron Pattern Command	C1D4h
5	Wake-up Timer Command	E196h
6	Extended Wake-up Timer Command	C300h
7	Low Duty-Cycle Command	CC0Eh
8	Low Battery Detector and Clock Divider Command	C213h
9	AFC Control Command	C687h
10	Data Filter Command	C462h
11	Data Rate Command	C813h
12	FIFO Settings Command	CE87h
13	Extended Features Command	B0CAh
14	Status Register Read Command	0000h

5.3. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	928Ah

Bit 12-11 <*b1* : *b0*>:Receiving band selection:

b1	b0	Frequency Band [MHz]
0	0	reserved
0	1	433
1	0	868
1	1	915

Bit 10 <*eb*>: Enables the low battery detector circuit

Bit 9 <*et*>: When set, enables the operation of the wake-up timer

Bit 8 <*ex*>: If *ex* is set the crystal oscillator remains turned on during the inactive periods of the chip

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Bit 7:4 <*x3* : *x0*>: Crystal load capacitance. Set according to the crystal's specified load capacitance.

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
……				….
1	1	1	0	15.5
1	1	1	1	16.0

Bit 3:1 <*i2* : *i0*>: Baseband filter bandwidth

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	Reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	135
1	1	0	Reserved
1	1	1	Reserved

Bit 0 <*dc*>: When *dc* bit is set it disables the clock output.

Note: The internal 32 kHz oscillator is turned on by setting the *elfc* bit in the "5.10. Low Battery Detector and Microcontroller Clock Divider Command" on page 21 or the *enldc* bit in the "5.9. Low Duty Cycle Command" on page 20 or by enabling the low battery detector using *eb* bit or by turning on the wake-up timer (*et* bit) in this command.
Clock tail feature: When the clock output (pin 8) used to provide clock signal for the microcontroller (*dc* bit is set to 0), it is possible to use the clock tail feature. This means that the crystal oscillator turn off is delayed, after issuing the command (clearing the *ex* bit) 512 more clock pulses are provided. This ensures that the microcontroller can switch itself to low power consumption mode. It is possible to decrease the clock tail length to 128 pulses by clearing the *ctls* bit in "5.15. Extended Features Command" on page 26.

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5.4. Frequency Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	AD57h

The 12-bit parameter F (bits *f11* to *f0*) should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as follows:

f_0 = 10 x N x (C + F/4000) [MHz]

The constants N and C are determined by the selected band:

Band [MHz]	N	C
433	4	10
868	8	10
915	8	11

Band	Min Frequency	Max Frequency	PLL Frequency Step
433 MHz	400.96 MHz	439.03 MHz	10 kHz
868 MHz	801.92 MHz	878.06 MHZ	20 kHz
915 MHz	881.92 MHz	958.06 MHz	20 kHz

5.5. Receiver Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C080h

Bit 7:6 *<d1 : d0>*: Select the VDI (valid data indicator) signal:

d1	d0	VDI output
0	0	Digital RSSI Out (DRSSI)
0	1	Data Quality Detector Output (DQD)
1	0	Clock Recovery Lock
1	1	Always High

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Bit 5:4 *<g1 : g0>*: Set the LNA gain:

g1	g0	G_{LNA} (dB relative to maximum gain)
0	0	0
0	1	−6
1	0	−12
1	1	−18

Bit 3:1 *<r2 : r0>*: Control the threshold of the RSSI detector:

r2	r1	r0	$RSSI_{setth}$ [dBm]
0	0	0	−103
0	0	1	−97
0	1	0	−91
0	1	1	−85
1	0	0	−79
1	0	1	−73
1	1	0	−67
1	1	1	−61

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th} = RSSI_{setth} + G_{LNA}$$

Bit 0 *<en>*: Enables the whole receiver chain and crystal oscillator when set. Enable/disable of the wake-up timer and the low battery detect or are not affected by this setting.

5.6. Synchron Pattern Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	1	b7	b6	b5	b4	b3	b2	b1	b0	C1D4h

The synchron pattern consists of two bytes. Byte 1 is fixed 2Dh, Byte 0 is programmable (default D4h) by B *<b7 : b0>*. For more details, see "5.14. FIFO Settings Command" on page 25.

5.7. Wake-Up Timer Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	0	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M *<m13 : m0>* , R *<r3 : r0>* and C *<c1 : c0>*:

$$T_{wake-up} = M \times 2^{R-C} \text{ ms}$$

The upper six bits of M *<m13 : m8>* and the C *<c1 : c0>* parameter can be found in the *Extended Wake-Up Timer Command*, see below.

Note: The wake-up timer generates interrupts continuously at the programmed interval while the *et* bit ("5.3. Configuration Setting Command" on page 16) is set.

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5.8. Extended Wake-Up Timer Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	1	c1	c0	m13	m12	m11	m10	m9	m8	C300h

These bits can be used to extend the range of the wake-up timer. The explanation of the bits can be found under the Wake-Up Timer Command description (see above).

5.9. Low Duty Cycle Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	enldc	CC0Eh

With this command, autonomous low duty cycle operation can be set up in order to decrease the average power consumption in receive mode.

Bit 7-1 <*d6* : *d0*>: The duty cycle can be calculated by using D <*d6* to *d0*> and M. (M is parameter in a *Wake-Up Timer Command*, see above). The time cycle is determined by the *Wake-Up Timer Command*.
duty cycle= (D x 2 +1) / M x 100%

Bit 0 <*enldc*>: Enables the low duty cycle mode. Wake-up timer interrupt is not generated in this mode.

Note: For this operating mode, bit *en* must be cleared in the "5.5. Receiver Setting Command" on page 18 and bit *et* must be set in the "5.3. Configuration Setting Command" on page 16.
In low duty cycle mode the receiver periodically wakes up for a short period of time and checks if there is a valid FSK transmission is in progress. FSK transmission is detected in the frequency range determined by "5.4. Frequency Setting Command" on page 18 plus and minus the baseband filter bandwidth set by the "5.3. Configuration Setting Command" on page 16. This on-time is automatically extended while DQD indicates good received signal condition.

When calculating the on-time take into account the crystal oscillator, the synthesizer, and the PLL need time to start, see the "Table 2. AC Characteristics" on page 6 depending on the DQD parameter, the chip needs to receive a few valid data bits before the DQD signal indicates good signal condition "5.12. Data Filter Command" on page 23. Choosing too short on-cycle can prevent the crystal oscillator from starting or the DQD signal may not go high even when the received signal has good quality.

There is an application proposal shown below. The Si4322 is configured to work in FIFO mode. The chip periodically wakes up and switches to receiving mode. If valid FSK data received, the chip sends an interrupt to the microcontroller and continues filling the RX FIFO. After the transmission is over and the FIFO is read out completely and all other interrupts are cleared, the chip goes back to low power consumption mode.
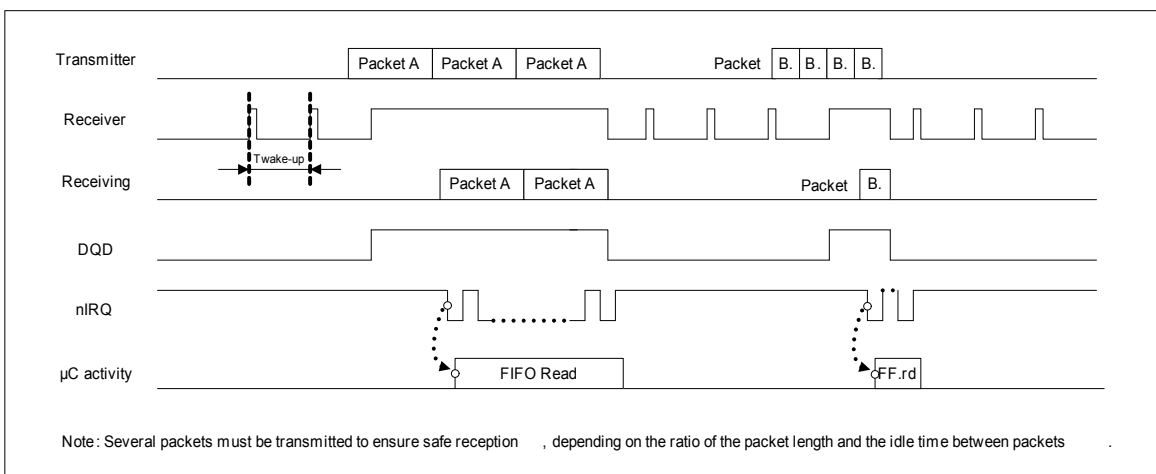

Figure 4. Application Proposal for LPDM (Low Power Duty-Cycle Mode) Receivers

5.10. Low Battery Detector and Microcontroller Clock Divider Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	cd2	cd1	cd0	elfc	t3	t2	t1	t0	C213h

Bit 7:5 <*cd2* : *cd0*>:Clock divider configuration (valid only if the crystal oscillator is on):

cd2	cd1	cd0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

Bit 4 <*elfc*>: Enables the low frequency (32 kHz) clock during sleep mode. The clock signal is present on the CLK pin regardless to the state of the *dc* bit ("5.3. Configuration Setting Command" on page 16).

Bit 3:0 <*t3* : *t0*>: The 4-bit value T of <*t3* : *t0*> determines the threshold voltage of the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.0 \text{ V} + T \times 0.1 \text{ V}$$

5.11. AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	rl1	rl0	st	fi	oe	aen	C687h

Bit 0 <*aen*>: Enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 <*oe*>: Enables the output (frequency offset) register

Bit 2 <*fi*>: Switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 <*st*>: Strobe edge. When *st* goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.

Bit 5:4 <*rl1* : *rl0*>: Limit the value of the frequency offset register to the following values:

rl1	rl0	Max dev [f_{res}]
0	0	No restriction
0	1	±4
1	0	±2
1	1	±1

f_{res}:

434MHz band:	10 kHz	
868MHz band:	20 kHz	
915MHz band:	20 kHz	

Bit 7:6 <*a1* : *a0*>:   Automatic operation mode selector:

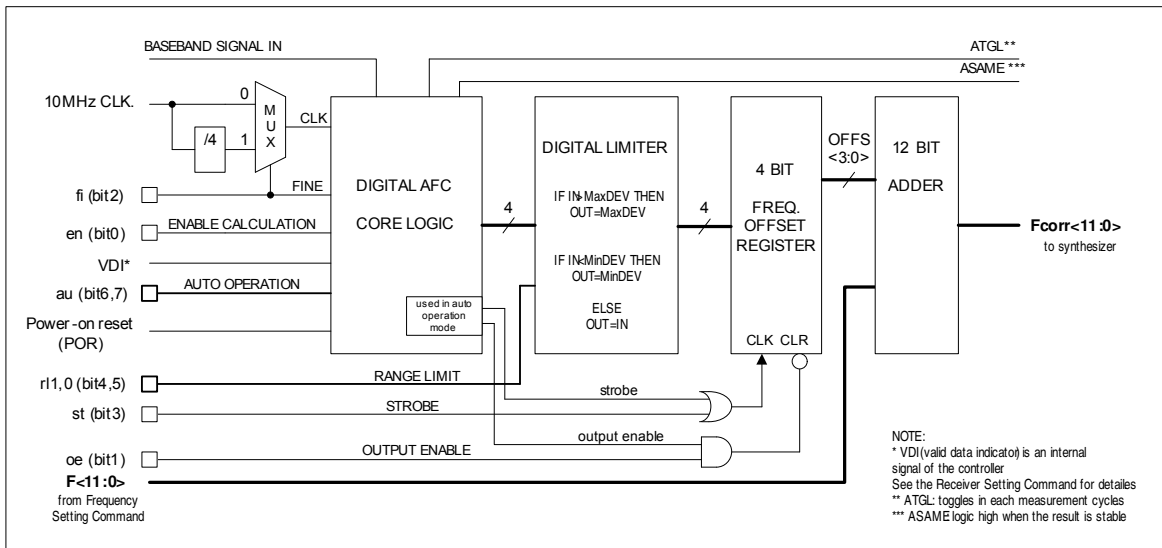| a1	a0	Operation mode
0	0	Auto mode off (Strobe is controlled by µC)
0	1	Runs only once after each power-up
1	0	Keep the f_{offset} only during receiving (VDI=high).
1	1	Keep the f_{offset} value

Figure 5. AFC Operation Block Diagram

In manual mode, the strobe signal is provided by the microcontroller. One measurement cycle can compensate about 50-60% of the actual frequency offset. Two measurement cycles can compensate 80%, and three measurement cycles can compensate 92%. The ATGL bit in the status register can be used to determine when the actual measurement cycle is finished.

In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register) the AFC circuit is automatically enabled when the VDI indicates potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

Without AFC the transmitter and the receiver needs to be tuned precisely to the same frequency. RX/TX frequency offset can lower the range. The units must be adjusted carefully during production, stable, expensive crystal must be used to avoid drift or the output power needs to be increased to compensate range loss.

The AFC block will calculate the TX-RX offset. This value will be used to pull the RX synthesizer close to the frequency of the transmitter. The main benefits of the automatic frequency control: low cost crystal can be used, the temperature or aging drift will not cause range loss and no production alignment needed.

There are four operation modes:

1. (*a1*=0, *a0*=0) Automatic operation of the AFC is off. Strobe bit can be controlled by the microcontroller.

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2. (*a1*=0, *a0*=1) The circuit measures the frequency offset only once after power up. This way, extended TX-RX distance can be achieved. In the final application, during the first receiving cycle, the circuit measures and compensates for the frequency offset caused by the crystal tolerances. This method allows the use of lower cost crystal in the application and provides protection against tracking an interferer.

3. (*a1*=1, *a0*=0) The frequency offset is calculated automatically and the center frequency is corrected when the VDI is high. The calculated value is dropped when the VDI goes low. To improve the efficiency of the AFC calculation two methods are recommended:

   a. The transmit package should start with a low effective baud rate pattern (i.e.: 00110011) because it is easier to receive. The circuit automatically measures the frequency offset during this initial pattern and changes the receiving frequency accordingly. The further part of the package will be received by the corrected frequency settings.

   b. The transmitter sends the first part of the packet with a step higher deviation than required during normal operation to ease the receiving. After the frequency shift was corrected, the deviation can be reduced.

   In both cases (3a and 3b), when the VDI indicates poor receiving conditions (VDI goes low), the output register is automatically cleared. Use this "drop offset" mode when the receiver communicates with more than one transmitter.

4. (*a1*=1, *a0*=1) It is similar mode 3, but suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is kept independently of the state of the VDI signal. When the receiver is paired with only one transmitter, it is possible to use this "keep offset" mode. In this case, the DRSSI limit should be selected carefully to minimize the range hysteresis.

5.12. Data Filter Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	al	ml	dsfi	sf	ewi	f2	f1	f0	C462h

Bit 7 <*al*>: Clock recovery (CR) auto lock control
   1: auto mode: the CR starts in fast mode and after locking it switches to slow mode. The *ml* bit (Bit 6) has no effect.
   0: manual mode: the clock recovery mode is set by Bit 6 <*ml*>

Bit 6 <*ml*>: Clock recovery lock control
   1: fast mode, fast attack and fast release (4 to 8-bit preamble (1010...) is recommended)
   0: slow mode, slow attack and slow release (12 to 16-bit preamble is recommended)
   Using the slow mode requires more accurate bit timing (see "5.13. Data Rate Command" on page 24).

Bit 5 <*dsfi*>: Disables auto-sleep on FIFO interrupt if set to 1.

This mode helps to decrease the average current consumption of the receiver. In normal mode (auto-sleep is disabled) the receiver remains active after receiving a given number of bits (set by the FIFO IT level, see the "5.14. FIFO Settings Command" on page 25). If the auto-sleep is enabled the part goes to stand-by mode when FIFO interrupt occurs – increasing this way the battery life. Use this mode when the transmitted data length is known and set the FIFO IT level to this value.

Bit 4 <*sf*>: Selects the type of the data filter

sf	Filter Type
0	Digital filter
1	Analog RC filter

Digital Filter: This is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the "5.13. Data Rate Command" on page 24.

Note: Bit rate cannot exceed 115 kbps in this mode.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kΩ resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates.

Data Rate [kbps]	1.2	2.4	4.8	9.6	19.2	38.4	57.6	115.2	256
Filter Capacitor Value	12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO cannot be used.

Bit 3 <*ewi*>:   Enables the automatic wake-up on any interrupt event. When the *ewi* bit is set, the crystal oscillator turns on automatically when an interrupt occurs. This time the crystal oscillator stays active until all the active interrupts cleared. Clearing the *ex* bit in the "5.3. Configuration Setting Command" on page 16 will not stop the oscillator.

Bit 2:0 <*f2 : f0*>:   DQD threshold parameter. The Data Quality Detector is a digital processing part of the radio, connected to the demodulator—it is an indicator reporting the quality of an FSK modulated RF signal. It works every time when the receiver is on. Setting its parameter defines how clean should be the incoming data stream to be qualified as good data (valid FSK signal).

If the internally calculated data quality value exceeds the DQD threshold parameter for five consecutive data bits for both the high and low periods, then the DQD signal goes high.

The DQD parameter in the Data Filter Command should be chosen according to the following rules:

- The DQD parameter can be calculated with the following formula:
  $DQD_{par} = 4 \times (deviation - TX\text{-}RX_{offset}) / bit\ rate$

- It should be larger than 4 because otherwise noise might be treated as a valid FSK signal.

- The maximum value is 7.

5.13. Data Rate Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C813h

Bit 7 <*cs*>:   Enables the prescaler in the data rate clock generation circuit (1/8 divider)

Bit 6:0 <*r6 : r0*>:   The seven bit value of R <*r6 : r0*> sets the divider ratio of the data rate clock generation circuit

The expected bit rate of the received data stream is determined by the R value and the *cs* bit. Set R according the next function:

$$R = (10\ MHz / 29 / (1 + cs \times 7) / BR) - 1, \text{ where BR is the bit rate}$$

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: $\Delta BR/BR < 1 / (29 \times N_{bit})$ Clock recovery in fast mode: $\Delta BR/BR < 3 / (29 \times N_{bit})$

BR is the bit rate set in the receiver and ΔBR is bit rate difference between the transmitter and the receiver. N_{bit} is the maximal number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1→0 and 0→1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

ΔBR is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or V_{DD} condition.

Supposing that the maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.

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5.14. FIFO Settings Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE87h

Bit 7:4 <*f3* : *f0*>: Together with bits <*f5* : *f4*> of the *Extended Features Command* (see below) determines the FIFO IT level. The FIFO generates IT when the number of the received data bits reaches this level.

Bit 3:2 <*s1* : *s0*>: Select the input of the FIFO fill start condition:

s1	s0	FIFO Start Condition
0	0	VDI
0	1	Synchron Pattern
1	0	
1	1	Always
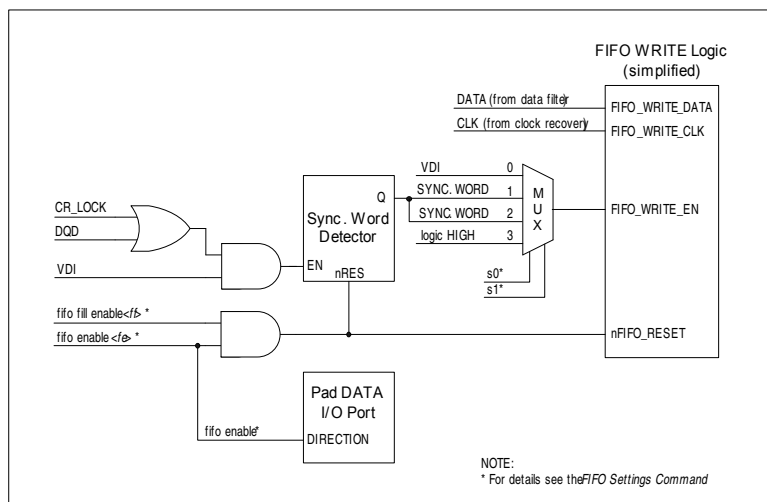
Note: For details of the VDI (Valid Data Indicator) signal see the "5.5. Receiver Setting Command" on page 18.

The synchron pattern consists of two bytes. Byte 1 is fixed 2Dh, Byte 0 is programmable (default D4h) in the "5.6. Synchron Pattern Command" on page 19.

Bit 1 <*ff*>: Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0 <*fe*>: Enables the 64-bit deep FIFO mode. To clear the counter of the FIFO, it has to be set to zero.

Note: To restart the synchron word reception, the *ff* bit should be cleared and set. This action will initialize the FIFO and clear its content.

The *fe* bit modifies the function of DATA (pin 6) and DCLK (pin 7) outputs. The DATA pin becomes FIFO select input (nFFS). If the chip is used in FIFO mode, do not allow this to be a floating input. The DCLK pin changes to FIFO interrupt output (FFIT) if this bit is set to 1.