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Si4330-B1

Si4330 ISM Receiver

Features

- Frequency Range = 240–960 MHz
- Sensitivity = –121 dBm
- Low Power Consumption
  - 18.5 mA receive
- Data Rate = 0.123 to 256 kbps
- FSK, GFSK, and OOK modulation
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Digital RSSI
- Wake-up timer
- Auto-frequency calibration (AFC)
- Clear channel assessment
- Programmable RX BW 2.6–620 kHz
- Programmable packet handler
- Programmable GPIOs
- Embedded antenna diversity algorithm
- Configurable packet handler
- Preamble detector
- RX 64 byte FIFO
- Low battery detector
- Temperature sensor and 8-bit ADC
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-Pin QFN package
- Low BOM
- Power-on-reset (POR)

Applications

- Remote control
- Home security & alarm
- Telemetry
- Personal data logging
- Toy control
- Tire pressure monitoring
- Wireless PC peripherals
- Remote meter reading
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Tag readers

Description

Silicon Laboratories' Si4330 is a highly integrated, single chip wireless ISM receiver. The high-performance EZRadioPRO® family includes a complete line of transmitters, receivers, and transceivers allowing the RF system designer to choose the optimal wireless part for their application.

The Si4330 offers advanced radio features including continuous frequency coverage from 240–960 MHz. The Si4330's high level of integration offers reduced BOM cost while simplifying the overall system design. The extremely low receive sensitivity (–121 dBm) ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance.

Additional system features such as an automatic wake-up timer, low battery detector, 64 byte RX FIFO, automatic packet handling, and preamble detection reduce overall current consumption and allow the use of a lower-cost system MCU. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.

The Si4330's digital receive architecture features a high-performance ADC and DSP based modem which performs demodulation, filtering, and packet handling for increased flexibility and performance.

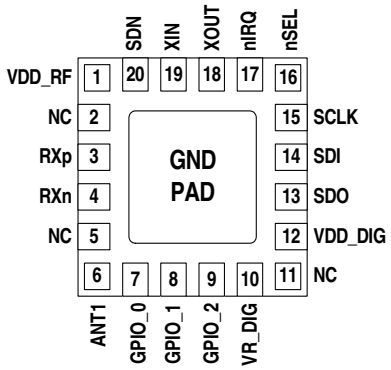
An easy-to-use calculator is provided to quickly configure the radio settings, simplifying customer's system design and reducing time to market.

Ordering Information:

See page 63.

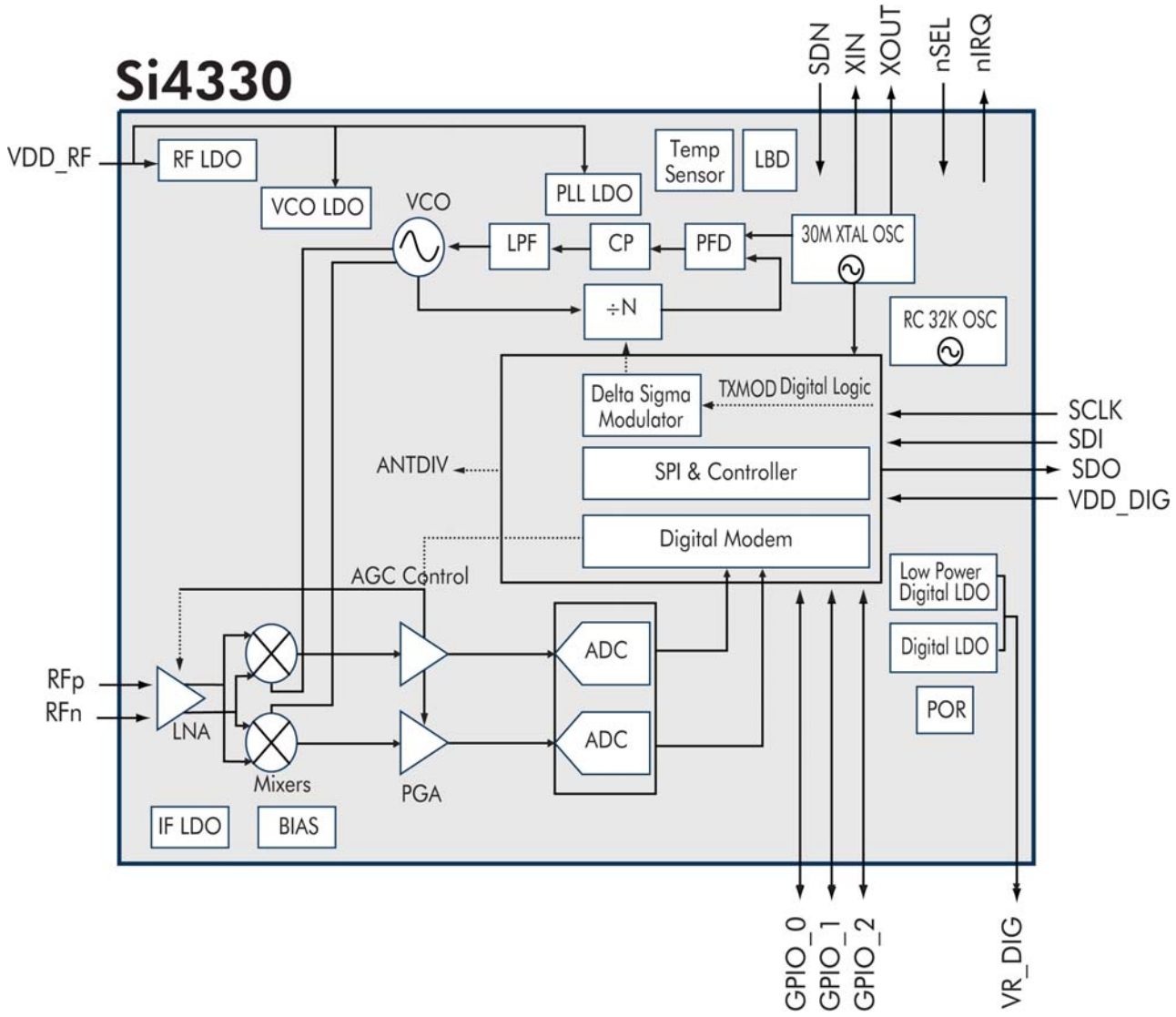
Pin Assignments

Si4330



Patents pending

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{DD}		1.8	3.0	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF[2]	—	15	50	nA
	$I_{Standby}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF	—	450	800	nA
	I_{Sleep}	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF	—	1	—	µA
	$I_{Sensor-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	$I_{Sensor-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled	—	800	—	µA
TUNE Mode Current	I_{Tune}	Synthesizer and regulators enabled	—	8.5	—	mA
RX Mode Current	I_{RX}		—	18.5	—	mA

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 13.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 13.

Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	F_{SYN}		240	—	960	MHz
Synthesizer Frequency Resolution[2]	F_{RES-LB}	Low Band, 240–480 MHz	—	156.25	—	Hz
	F_{RES-HB}	High Band, 480–960 MHz	—	312.5	—	Hz
Reference Frequency Input Level[2]	f_{REF_LV}	When using external reference signal driving XOUT pin, instead of using crystal. Measured peak-to-peak (V_{PP})	0.7	—	1.6	V
Synthesizer Settling Time[2]	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO calibration.	—	200	—	µs
Residual FM[2]	ΔF_{RMS}	Integrated over ±250 kHz bandwidth (500 Hz lower bound of integration)	—	2	4	kHz_{RMS}
Phase Noise[2]	$L\phi(f_M)$	ΔF = 10 kHz	—	–80	—	dBc/Hz
		ΔF = 100 kHz	—	–90	—	dBc/Hz
		ΔF = 1 MHz	—	–115	—	dBc/Hz
		ΔF = 10 MHz	—	–130	—	dBc/Hz

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 13.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 13.

Table 3. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range	F_{RX}		240	—	960	MHz
RX Sensitivity[2]	P_{RX_2}	(BER < 0.1%) (2 kbps, GFSK, BT = 0.5, Δf = ±5 kHz)[3]	—	–121	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)[3]	—	–108	—	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)[3]	—	–104	—	dBm
	P_{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, Δf = ±62.5 kHz)	—	–101	—	dBm
	P_{RX_OOK}	(BER < 0.1%) (4.8 kbps, 350 kHz BW, OOK)[3]	—	–110	—	dBm
		(BER < 0.1%) (40 kbps, 400 kHz BW, OOK)[3]	—	–102	—	dBm
RX Channel Bandwidth[3]	BW		2.6	—	620	kHz
BER Variation vs Power Level[3]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm
LNA Input Impedance[3] (Unmatched—measured differentially across RX input pins)	R_{IN-RX}	915 MHz	—	51–60j	—	Ω
		868 MHz	—	54–63j	—	
		433 MHz	—	89–110j	—	
		315 MHz	—	107–137j	—	
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[3]	C/I_{1-CH}	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5, channel spacing = 150 kHz	—	–31	—	dB
±2-Ch Offset Selectivity[3]	C/I_{2-CH}		—	–35	—	dB
≥ ±3-Ch Offset Selectivity[3]	C/I_{3-CH}		—	–40	—	dB
Blocking at 1 MHz Offset[3]	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5	—	–52	—	dB
Blocking at 4 MHz Offset[3]	$4M_{BLOCK}$		—	–56	—	dB
Blocking at 8 MHz Offset[3]	$8M_{BLOCK}$		—	–63	—	dB
Image Rejection[3]	Im_{REJ}	Rejection at the image frequency. IF=937 kHz	—	–30	—	dB
Spurious Emissions[3]	P_{OB_RX1}	Measured at RX pins	—	—	–54	dBm

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 13.
2. Receive sensitivity at multiples of 30 MHz may be degraded. If channels with a multiple of 30 MHz are required it is recommended to shift the crystal frequency. Contact Silicon Labs Applications Support for recommendations.
3. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 13.

Table 4. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature Sensor Accuracy[2]	TS_A	After calibrated via sensor offset register tvoffs[7:0]	—	0.5	—	°C
Temperature Sensor Sensitivity[2]	TS_S		—	5	—	mV/°C
Low Battery Detector Resolution[2]	LBD_{RES}		—	50	—	mV
Low Battery Detector Conversion Time[2]	LBD_{CT}		—	250	—	µs
Microcontroller Clock Output Frequency	F_{MC}	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768K	—	30M	Hz
General Purpose ADC Resolution[2]	ADC_{ENB}		—	8	—	bit
General Purpose ADC Bit Resolution[2]	ADC_{RES}		—	4	—	mV/bit
Temp Sensor & General Purpose ADC Conversion Time[2]	ADC_{CT}		—	305	—	µs
30 MHz XTAL Start-Up time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	600	—	µs
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	97	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	6	—	sec
32 kHz XTAL Accuracy using 32 kHz XTAL[2]	$32K_{RES}$	Using 20 ppm 32 kHz Crystal	—	100	—	ppm
32 kHz Accuracy using Internal RC Oscillator[2]	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	16	—	ms
Software Reset Time[2]	t_{soft}		—	100	—	µs

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 13.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 13.

Table 5. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 5 pF	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 5 pF	—	—	8	ns
Input Capacitance	C_{IN}		—	—	1	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} – 0.6	—	—	V
Logic Low Level Input Voltage	V_{IL}			—	0.6	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–100	—	100	nA
Logic High Level Output Voltage	V_{OH}	I_{OH}<1 mA source, V_{DD}=1.8 V	V_{DD} – 0.6	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OL}<1 mA sink, V_{DD}=1.8 V	—	—	0.6	V

Note: All specifications guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 13.

Table 6. GPIO Specifications (GPIO_0, GPIO_1, and GPIO_2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Input Capacitance	C_{IN}		—	—	1	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} – 0.6	—		V
Logic Low Level Input Voltage	V_{IL}		—	—	0.6	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–100	—	100	nA
Input Current If Pullup is Activated	I_{INP}	V_{IL}=0 V	5	—	25	µA
Maximum Output Current	I_{OmaxLL}	DRV<1:0>=LL	0.1	0.5	0.8	mA
	I_{OmaxLH}	DRV<1:0>=LH	0.9	2.3	3.5	mA
	I_{OmaxHL}	DRV<1:0>=HL	1.5	3.1	4.8	mA
	I_{OmaxHH}	DRV<1:0>=HH	1.8	3.6	5.4	mA
Logic High Level Output Voltage	V_{OH}	I_{OH}< I_{Omax} source, V_{DD}=1.8 V	V_{DD} – 0.6	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OL}< I_{Omax} sink, V_{DD}=1.8 V	—	—	0.6	V

Note: All specifications guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 13.

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.

1.1. Definition of Test Conditions

Production Test Conditions:

- T_A = +25 °C
- V_{DD} = +3.3 VDC
- Sensitivity measured at 919 MHz
- External reference signal (XOUT) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC
- Production test schematic (unless noted otherwise)
- All RF input and output levels referred to the pins of the Si4330 (not the RF module)

Extreme Test Conditions:

- T_A = –40 to +85 °C
- V_{DD} = +1.8 to +3.6 VDC
- Using 4330-T-B1-B-xxx reference design or production test schematic
- All RF input levels referred to the pins of the Si4330 (not the RF module)

2. Functional Description

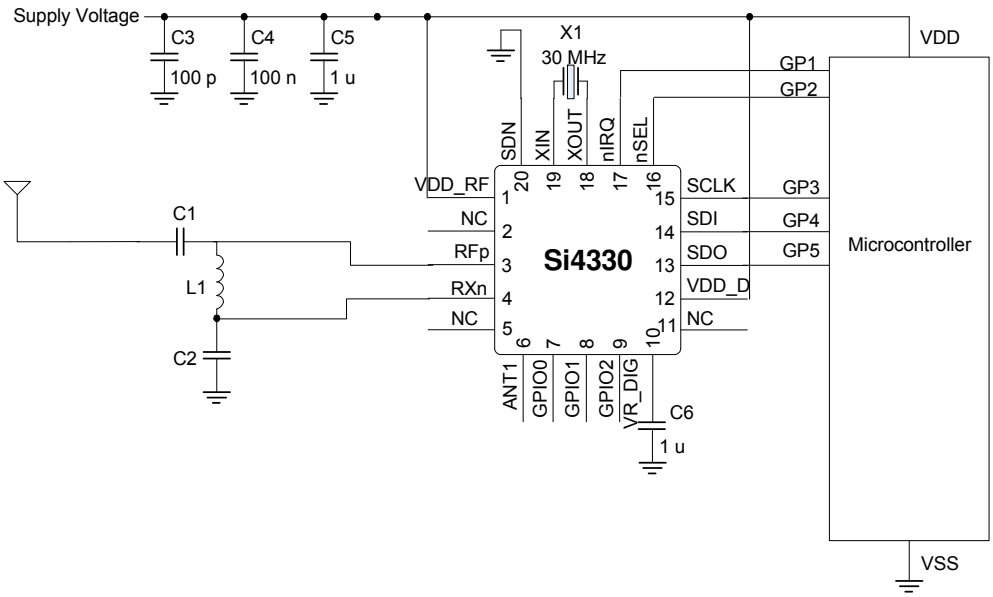
The Si4330 is an ISM wireless receiver with continuous frequency tuning over the specified bands which encompasses from 240–960 MHz. The wide operating voltage range of 1.8–3.6 V and low current consumption makes the Si4330 an ideal solution for battery powered applications.

The Si4330 receiver uses a single-conversion mixer to downconvert the 2-level FSK/GFSK/OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is then output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A high precision local oscillator (LO) is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency and frequency deviation at any frequency between 240–960 MHz.

The Si4330 supports frequency hopping and antenna diversity switch control to extend the link range and improve performance. Antenna diversity is completely integrated into the Si4330 and can improve the system link budget by 8–10 dB, resulting in substantial range increases depending on the environmental conditions.

The Si4330 is designed to work with a microcontroller, crystal, and a few external components to create a very low cost system. Voltage regulators are integrated on-chip which allows for a wide operating supply voltage range from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with an external microcontroller. Three configurable general purpose I/Os are available. A complete list of the available GPIO functions is shown in "8. Auxiliary Functions" on page 40 and includes microcontroller clock output, Antenna Diversity, Antenna Switch, POR, and various interrupts. A complete list of the available GPIO functions is shown in AN467: Si4330 Register Descriptions."



Programmable load capacitors for X1 are integrated.

L1, C1, and C2 values depend on frequency band, and antenna impedance.

Figure 1. RX Application Example

2.1. Operating Modes

The Si4330 provides several operating modes which can be used to optimize the power consumption for a given application. Depending upon the system communication protocol, an optimal trade-off between the radio wake time and power consumption can be achieved.

Table 8 summarizes the operating modes of the Si4330. In general, any given operating mode may be classified as an active mode or a power saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception of the SHUTDOWN mode, all can be dynamically selected by sending the appropriate commands over the SPI operating mode. An “X” in any cell means that, in the given mode of operation, that block can be independently programmed to be either ON or OFF, without noticeably impacting the current consumption. The SPI circuit block includes the SPI interface hardware and the device register space. The 32 kHz OSC block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor, general purpose ADC, and low-battery detector.

Table 8. Operating Modes

Mode Name	Circuit Blocks							
	Digital LDO	SPI	32 kHz OSC	AUX	30 MHz XTAL	PLL	RX	I_{VDD}
SHUTDOWN	OFF (Register contents lost)	OFF	OFF	OFF	OFF	OFF	OFF	15 nA
STANDBY	ON (Register contents retained)	ON	OFF	OFF	OFF	OFF	OFF	450 nA
SLEEP		ON	ON	X	OFF	OFF	OFF	1 µA
SENSOR		ON	X	ON	OFF	OFF	OFF	1 µA
READY		ON	X	X	ON	OFF	OFF	800 µA
TUNING		ON	X	X	ON	ON	OFF	8.5 mA
RECEIVE		ON	X	X	ON	ON	ON	18.5 mA

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si4330 communicates with the host MCU over a standard 3-wire SPI interface: SCLK, SDI, and nSEL. The host MCU can read data from the device on the SDO output pin. A SPI transaction is a 16-bit sequence which consists of a Read-Write ($\overline{R}$/W) select bit, followed by a 7-bit address field (ADDR), and an 8-bit data field (DATA) as demonstrated in Figure 2. The 7-bit address field is used to select one of the 128, 8-bit control registers. The $\overline{R}$/W select bit determines whether the SPI transaction is a read or write transaction. If $\overline{R}$/W = 1 it signifies a WRITE transaction, while $\overline{R}$/W = 0 signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4330 every eight clock cycles. The timing parameters for the SPI interface are shown in Table 9. The SCLK rate is flexible with a maximum rate of 10 MHz.

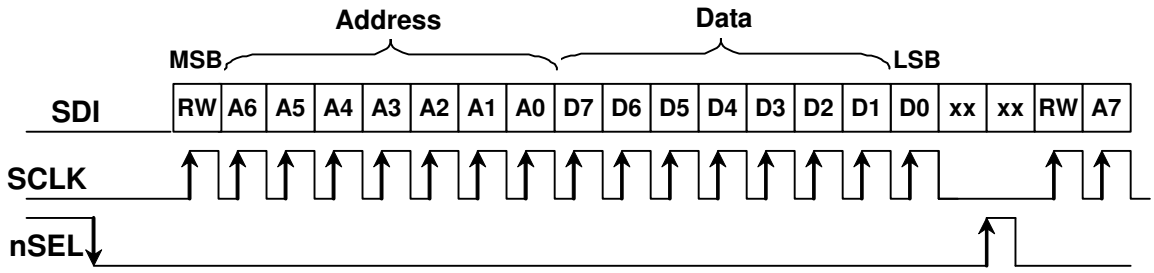
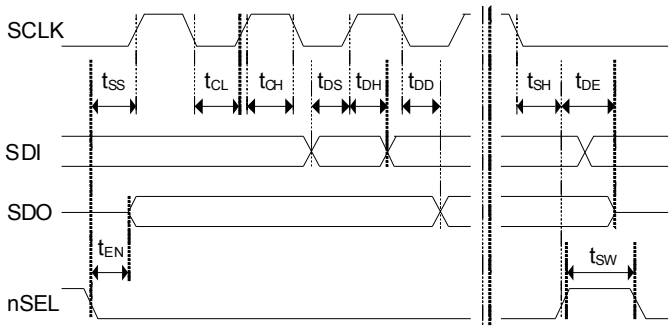


Figure 2. SPI Timing

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (nsec)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

To read back data from the Si4330, the R/W bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored n the SDI pin when R/W = 0. The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 3. After the READ function is completed the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pullup.

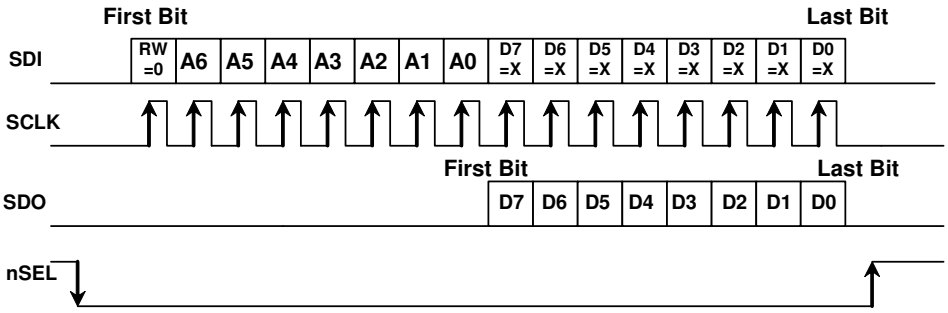


Figure 3. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode which allows for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An example burst write transaction is illustrated in Figure 4 and a burst read in Figure 5. As long as nSEL is held low, input data will be latched into the Si4330 every eight SCLK cycles.

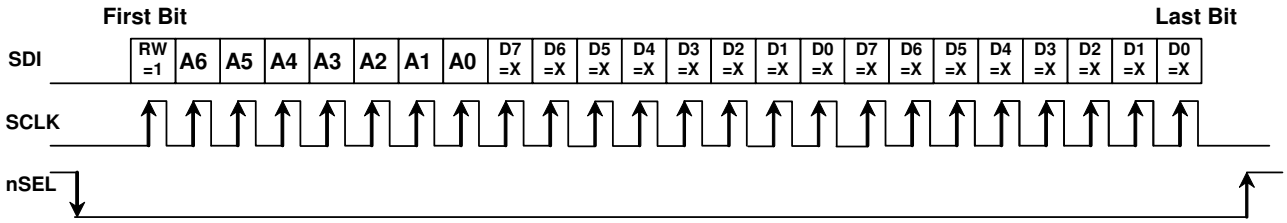


Figure 4. SPI Timing—Burst Write Mode

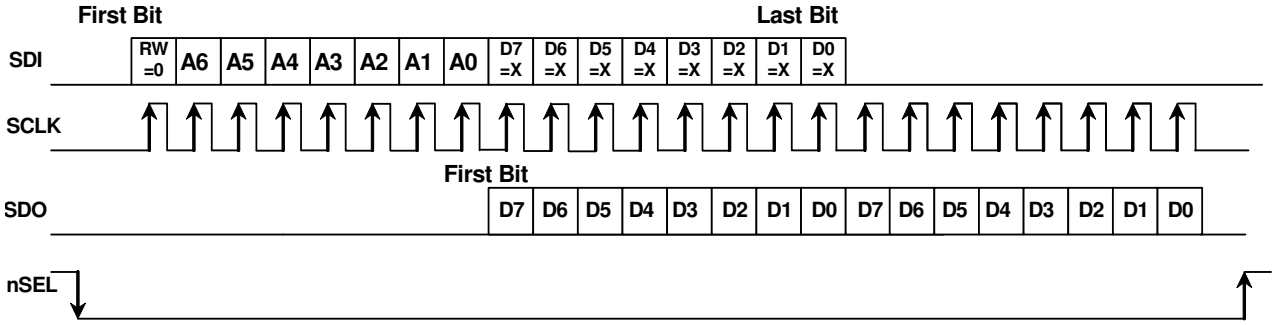


Figure 5. SPI Timing—Burst Read Mode

3.2. Operating Mode Control

There are three primary states in the Si4330 radio state machine: SHUTDOWN, IDLE, and RX (see Figure 6). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. "Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected with the exception of SHUTDOWN which is controlled by SDN pin 20. The RX state may be reached automatically from any of the IDLE states by setting the rxon bit in "Register 07h. Operating Mode and Function Control 1". Table 10 shows each of the operating modes with the time required to reach RX mode as well as the current consumption of each mode.

The Si4330 includes a low-power digital regulated supply (LPLDO) which is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR_DIG pin). This common digital supply voltage is connected to all digital circuit blocks including the digital modem, crystal oscillator, SPI, and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes. The main digital regulator is automatically enabled in all other modes.

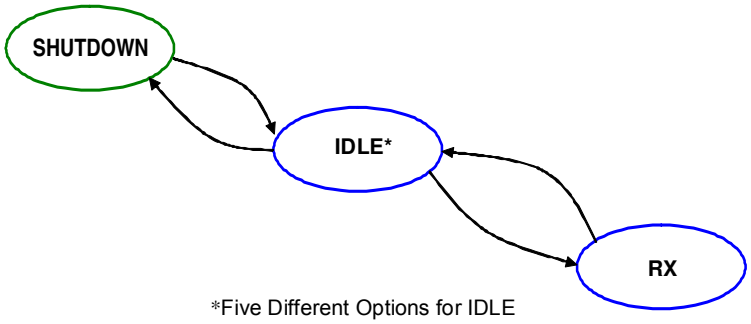


Figure 6. State Machine Diagram

Table 10. Operating Modes Response Time

State/Mode	Response Time to RX	Current in State /Mode [µA]
Shut Down State	16.8 ms	15 nA
Idle States:		
Standby Mode	800 µs	450 nA
Sleep Mode	800 µs	1 µA
Sensor Mode	800 µs	1 µA
Ready Mode	200 µs	800 µA
Tune Mode	200 µs	8.5 mA
RX State	NA	18.5 mA

3.2.1. SHUTDOWN State

The SHUTDOWN state is the lowest current consumption state of the device with nominally less than 15 nA of current consumption. The SHUTDOWN state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

3.2.2. IDLE State

There are five different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to RX mode. This tradeoff is shown in Table 10. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption of the five IDLE states with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The STANDBY mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "8.6. Wake-Up Timer and 32 kHz Clock Source" on page 46 for more information on the Wake-Up-Timer. SLEEP mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.3. SENSOR Mode

In SENSOR Mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 in "Register 07h. Operating Mode and Function Control 1". See "8.4. Temperature Sensor" on page 43 and "8.5. Low Battery Detector" on page 45 for more information on these features. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to RX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to RX mode by eliminating the crystal start-up time. READY mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled in “Register 62h. Crystal Oscillator Control and Test.” To exit ready mode, bufovr (bit 1) of this register must be set back to 0.

3.2.2.5. TUNE Mode

In TUNE Mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to RX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for frequency hopping spread spectrum systems (FHSS). TUNE mode is entered by setting pllon = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

3.2.3. RX State

The RX state may be entered from any of the IDLE modes when the rxon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the main digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the vcocal bit is “0”, default value is “1”).
5. Wait until PLL settles to required receive frequency (controlled by an internal timer).
6. Enable receive circuits: LNA, mixers, and ADC.
7. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

3.2.4. Device Status

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
02	R	Device Status	ffovfl	ffunfl	rxffem	headerr	freqerr		cps[1]	cps[0]	—

The operational status of the chip can be read from "Register 02h. Device Status".

3.3. Interrupts

The Si4330 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h–04h) containing the active Interrupt Status bit. The nIRQ output signal will then be reset until the next change in status is detected. The interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h–06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs it will not trigger the nIRQ pin, but the status may still be read at anytime in the Interrupt Status registers.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
03	R	Interrupt Status 1	ifferr	Reserved	Reserved	irxffafull	iext	Reserved	ipkvalid	icrcerror	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	Reserved	Reserved	enrxffafull	enext	Reserved	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h

For a complete descriptions of each interrupt, see “AN467: Si4330 Register Descriptions.”

3.4. System Timing

The system timing for RX mode is shown in Figure 7. The user only needs to program the desired mode, and the internal sequencer will properly transition the part from its current mode.

The VCO will automatically calibrate at every frequency change or power up. The PLL T0 time is to allow for bias settling of the VCO. The PLL TS time is for the settling time of the PLL, which has a default setting of 100 µs. The total time for PLL T0, PLL CAL, and PLL TS under all conditions is 200 µs. Under certain applications, the PLL T0 time and the PLL CAL may be skipped for faster turn-around time. Contact applications support if faster turnaround time is desired.

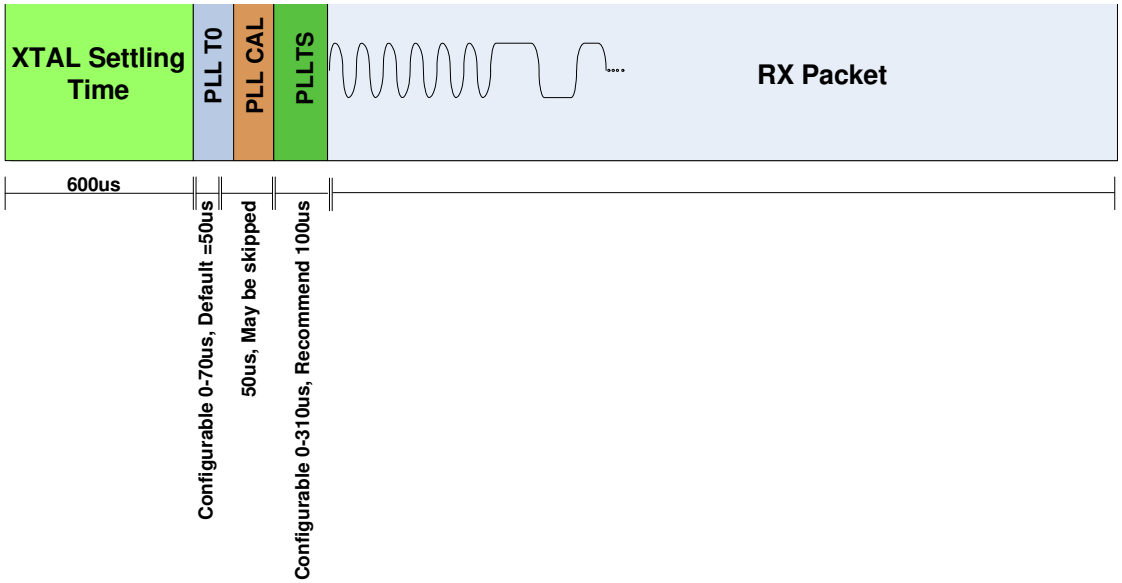


Figure 7. RX Timing

3.5. Frequency Control

For calculating the necessary frequency register settings it is recommended that customers use Silicon Labs' Wireless Design Suite (WDS) or the EZRadioPRO Register Calculator worksheet (in Microsoft Excel) available on the product website. These methods offer a simple method to quickly determine the correct settings based on the application requirements. The following information can be used to calculated these values manually.

3.5.1. Frequency Programming

In order to receive an RF signal, the desired channel frequency, $f_{carrier}$, must be programmed into the Si4330. Note that this frequency is the center frequency of the desired channel and not an LO frequency. The carrier frequency is generated by a Fractional-N Synthesizer, using 10 MHz both as the reference frequency and the clock of the (3rd order) ΔΣ modulator. This modulator uses modulo 64000 accumulators. This design was made to obtain the desired frequency resolution of the synthesizer. The overall division ratio of the feedback loop consist of an integer part (N) and a fractional part (F). In a generic sense, the output frequency of the synthesizer is as follows:

$$f_{OUT} = 10MHz \times (N + F)$$

The fractional part (F) is determined by three different values, Carrier Frequency (fc[15:0]), Frequency Offset (fo[8:0]), and Frequency Deviation (fd[7:0]). Due to the fine resolution and high loop bandwidth of the synthesizer, FSK modulation is applied inside the loop and is done by varying F according to the incoming data; this is discussed further in "3.5.4. Frequency Offset Adjustment" on page 26. Also, a fixed offset can be added to fine-tune the carrier frequency and counteract crystal tolerance errors. For simplicity assume that only the fc[15:0] register will determine the fractional component. The equation for selection of the carrier frequency is shown below:

$$f_{carrier} = 10MHz \times (hbsel + 1) \times (N + F)$$

$$f_{carrier} = 10MHz * (hbsel + 1) * (fb[4:0] + 24 + \frac{fc[15:0]}{64000})$$

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	fo[9]	fo[8]	00h
75	R/W	Frequency Band Select	Reserved	sbsel	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h

The integer part (N) is determined by fb[4:0]. Additionally, the frequency can be halved by connecting a ÷2 divider to the output. This divider is not inside the loop and is controlled by the hbsel bit in "Register 75h. Frequency Band Select." This effectively partitions the entire 240–960 MHz frequency range into two separate bands: High Band (HB) for hbsel = 1, and Low Band (LB) for hbsel = 0. The valid range of fb[4:0] is from 0 to 23. If a higher value is written into the register, it will default to a value of 23. The integer part has a fixed offset of 24 added to it as shown in the formula above. Table 11 demonstrates the selection of fb[4:0] for the corresponding frequency band.

After selection of the fb (N) the fractional component may be solved with the following equation:

$$fc[15:0] = \left(\frac{f_{carrier}}{10MHz * (hbsel + 1)} - fb[4:0] - 24 \right) * 64000$$

fb and fc are the actual numbers stored in the corresponding registers.

Table 11. Frequency Band Selection

fb[4:0] Value	N	Frequency Band	
		hbsel=0	hbsel=1
0	24	240–249.9 MHz	480–499.9 MHz
1	25	250–259.9 MHz	500–519.9 MHz
2	26	260–269.9 MHz	520–539.9 MHz
3	27	270–279.9 MHz	540–559.9 MHz
4	28	280–289.9 MHz	560–579.9 MHz
5	29	290–299.9 MHz	580–599.9 MHz
6	30	300–309.9 MHz	600–619.9 MHz
7	31	310–319.9 MHz	620–639.9 MHz
8	32	320–329.9 MHz	640–659.9 MHz
9	33	330–339.9 MHz	660–679.9 MHz
10	34	340–349.9 MHz	680–699.9 MHz
11	35	350–359.9 MHz	700–719.9 MHz
12	36	360–369.9 MHz	720–739.9 MHz
13	37	370–379.9 MHz	740–759.9 MHz
14	38	380–389.9 MHz	760–779.9 MHz
15	39	390–399.9 MHz	780–799.9 MHz
16	40	400–409.9 MHz	800–819.9 MHz
17	41	410–419.9 MHz	820–839.9 MHz
18	42	420–429.9 MHz	840–859.9 MHz
19	43	430–439.9 MHz	860–879.9 MHz
20	44	440–449.9 MHz	880–899.9 MHz
21	45	450–459.9 MHz	900–919.9 MHz
22	46	460–469.9 MHz	920–939.9 MHz
23	47	470–479.9 MHz	940–960 MHz

The chip will automatically shift the frequency of the Synthesizer down by 937.5 kHz (30 MHz ÷ 32) to achieve the correct Intermediate Frequency (IF) when RX mode is entered. Low-side injection is used in the RX Mixing architecture.

3.5.2. Easy Frequency Programming for FHSS

While Registers 73h–77h may be used to program the carrier frequency of the Si4330, it is often easier to think in terms of “channels” or “channel numbers” rather than an absolute frequency value in Hz. Also, there may be some timing-critical applications (such as for Frequency Hopping Systems) in which it is desirable to change frequency by programming a single register. Once the channel step size is set, the frequency may be changed by a single register corresponding to the channel number. A nominal frequency is first set using Registers 73h–77h, as described above. Registers 79h and 7Ah are then used to set a channel step size and channel number, relative to the nominal setting. The Frequency Hopping Step Size (fhs[7:0]) is set in increments of 10 kHz with a maximum channel step size of 2.56 MHz. The Frequency Hopping Channel Select Register then selects channels based on multiples of the step size.

$$F_{carrier} = Fnom + fhs[7:0] \times (fhch[7:0] \times 10kHz)$$

For example, if the nominal frequency is set to 900 MHz using Registers 73h–77h, the channel step size is set to 1 MHz using "Register 7Ah. Frequency Hopping Step Size," and "Register 79h. Frequency Hopping Channel Select" is set to 5d, the resulting carrier frequency would be 905 MHz. Once the nominal frequency and channel step size are programmed in the registers, it is only necessary to program the fhch[7:0] register in order to change the frequency.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h

3.5.3. Automatic State Transition for Frequency Change

If registers 79h or 7Ah are changed in RX mode, the state machine will automatically transition the chip back to TUNE and change the frequency. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System. This in turn reduces microcontroller activity, reducing current consumption.