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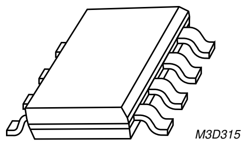


Si4420DY

N-channel enhancement mode field-effect transistor

Rev. 01 — 28 May 2001 **Product data**

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™[1] technology.

Product availability:

Si4420DY in SOT96-1 (SO8).

2. Features

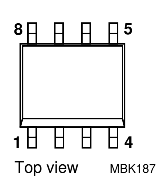
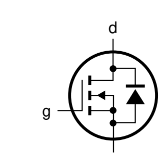
- Low on-state resistance
- Fast switching
- TrenchMOS™ technology.

3. Applications

- DC to DC convertors
- DC motor control
- Lithium-ion battery applications
- Notebook PC
- Portable equipment applications.

4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	 **SOT96-1 (SO8)**	
4	gate (g)		
5,6,7,8	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.

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5. Quick reference data

Table 2: Quick reference data

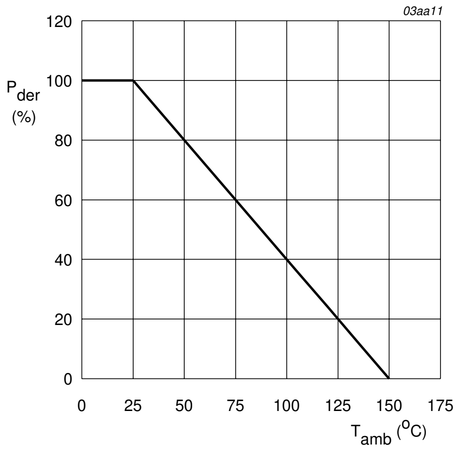
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 150 °C	–	30	V
I_D	drain current (DC)	T_{amb} = 25 °C; pulsed; $t_p \leq$ 10 s	–	12.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; pulsed; $t_p \leq$ 10 s	–	2.5	W
T_j	junction temperature		–	150	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 12.5 A	7.3	9	mΩ
		V_{GS} = 4.5 V; I_D = 10.5 A	10.9	13	mΩ

6. Limiting values

Table 3: Limiting values

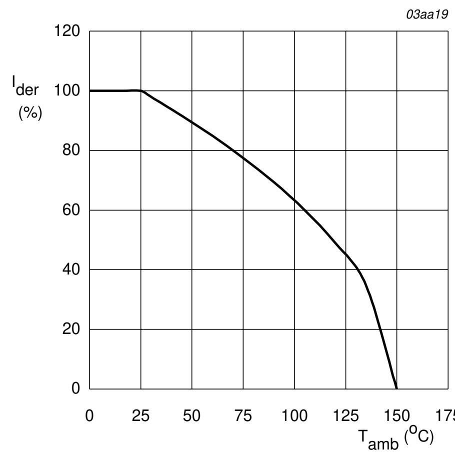
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 150 °C	–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_{amb} = 25 °C; pulsed; $t_p \leq$ 10 s; Figure 2 and 3	–	12.5	A
		T_{amb} = 70 °C; pulsed; $t_p \leq$ 10 s; Figure 2	–	10	A
I_{DM}	peak drain current	T_{amb} = 25 °C; pulsed; $t_p \leq$ 10 µs; Figure 3	–	50	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; pulsed; $t_p \leq$ 10 s;	–	2.5	W
		T_{amb} = 70 °C; pulsed; $t_p \leq$ 10 s; Figure 1	–	1.6	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{amb} = 25 °C; pulsed; $t_p \leq$ 10 s	–	2.3	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

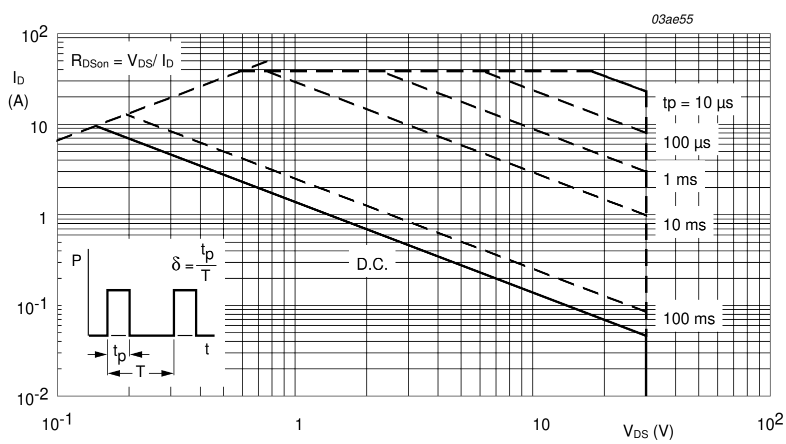
Fig 1. Normalized total power dissipation as a function of ambient temperature.



$V_{GS} \geq 10$ V

$$I_D = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



$T_{amb} = 25$ °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint, t ≤ 10 sec. Figure 4	50	K/W

7.1 Transient thermal impedance

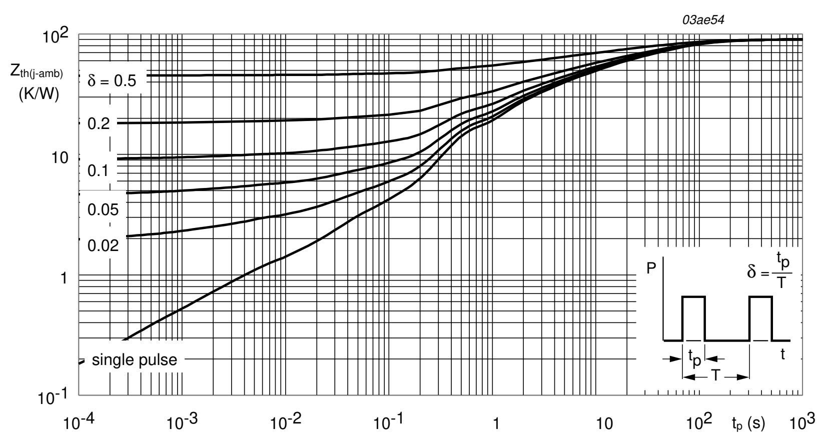


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{GS(th)}$	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; Figure 9	1	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	–	–	1	µA
		T_j = 55 °C	–	–	5	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	–	100	nA
$I_{D(on)}$	on-state drain current	V_{DS} ≥ 5 V; V_{GS} = 10 V	30		–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 12.5 A; Figure 7 and 8	–	7.3	9	mΩ
		V_{GS} = 4.5 V; I_D = 10.5 A; Figure 7 and 8	–	10.9	13	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 15 V; I_D = 7 A; Figure 11	–	15	–	S
$Q_{g(tot)}$	total gate charge	I_D = 12.5 A; V_{DD} = 15 V; V_{GS} = 10 V; Figure 14	–	64.5	120	nC
Q_{gs}	gate-source charge		–	7.6	–	nC
Q_{gd}	gate-drain (Miller) charge		–	11.5	–	nC
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_D = 15 Ω; V_{GS} = 10 V; R_G = 6 Ω	–	12	30	ns
t_r	turn-on rise time		–	15	60	ns
$t_{d(off)}$	turn-off delay time		–	60	150	ns
t_f	turn-off fall time		–	50	140	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 2.3 A; V_{GS} = 0 V; Figure 13	–	0.7	1.1	V
t_{rr}	reverse recovery time	I_S = 2.3 A; dI_S/dt = –100 A/µs	–	60	–	ns

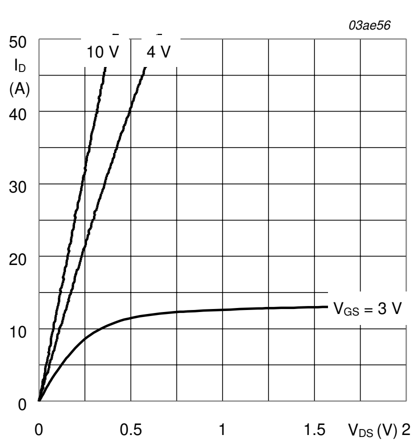
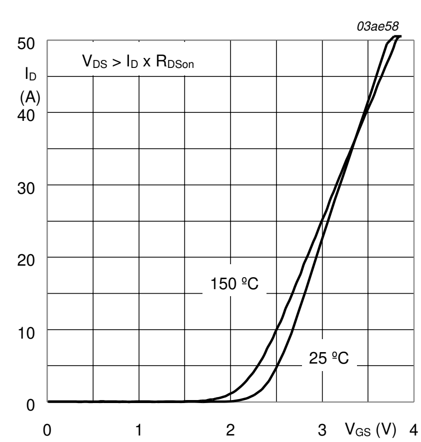
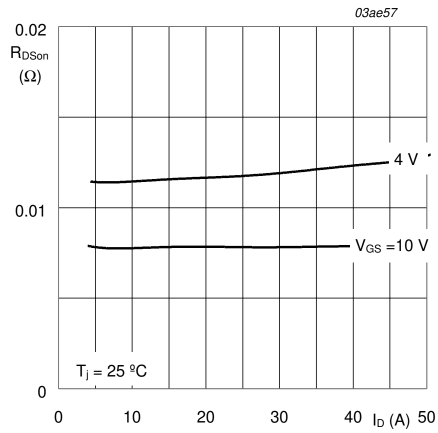


Fig 5. Output characteristic; drain current as a function of drain-source voltage; typical values.



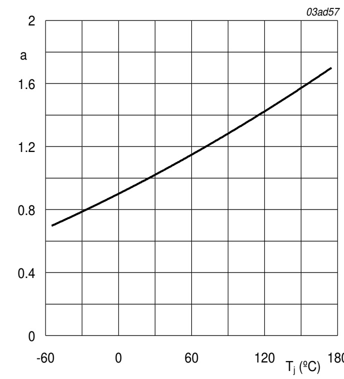
T_j = 25 °C and 150 °C; V_{DS} > I_D x R_{DSon}

Fig 6. Transfer characteristic: drain current as function of gate-source voltage; typical values



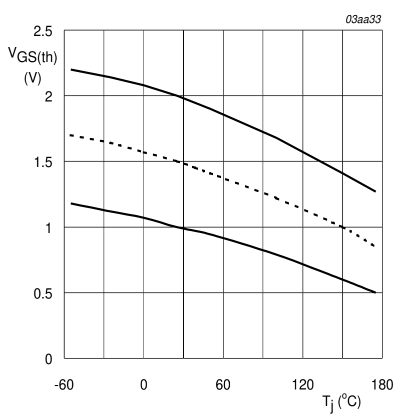
$T_j = 25$ °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



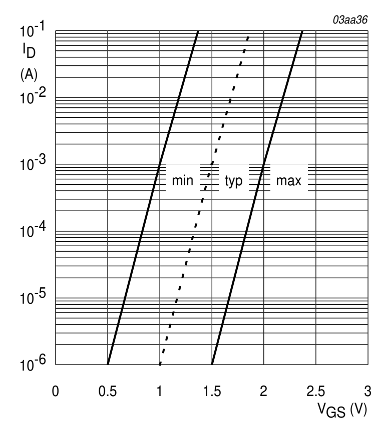
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



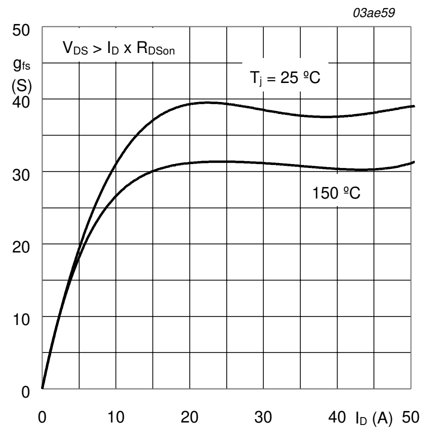
$I_D = 250$ µA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



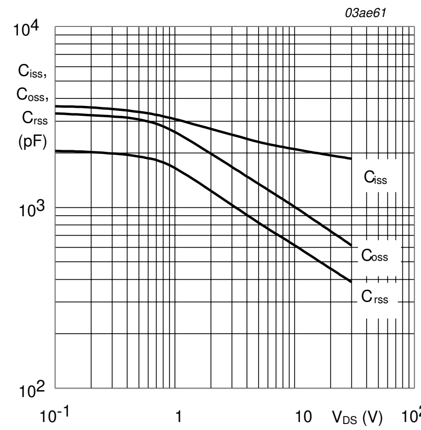
$T_j = 25$ °C; $V_{DS} = 5$ V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



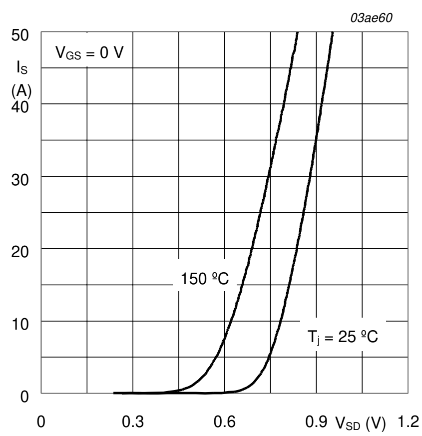
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



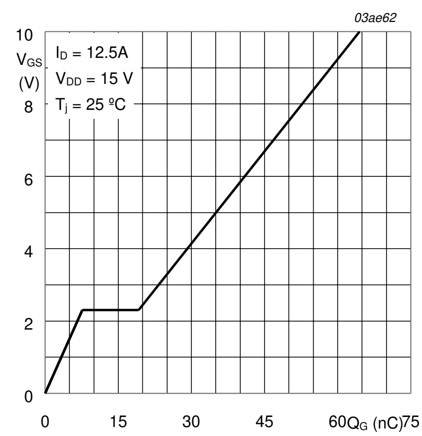
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

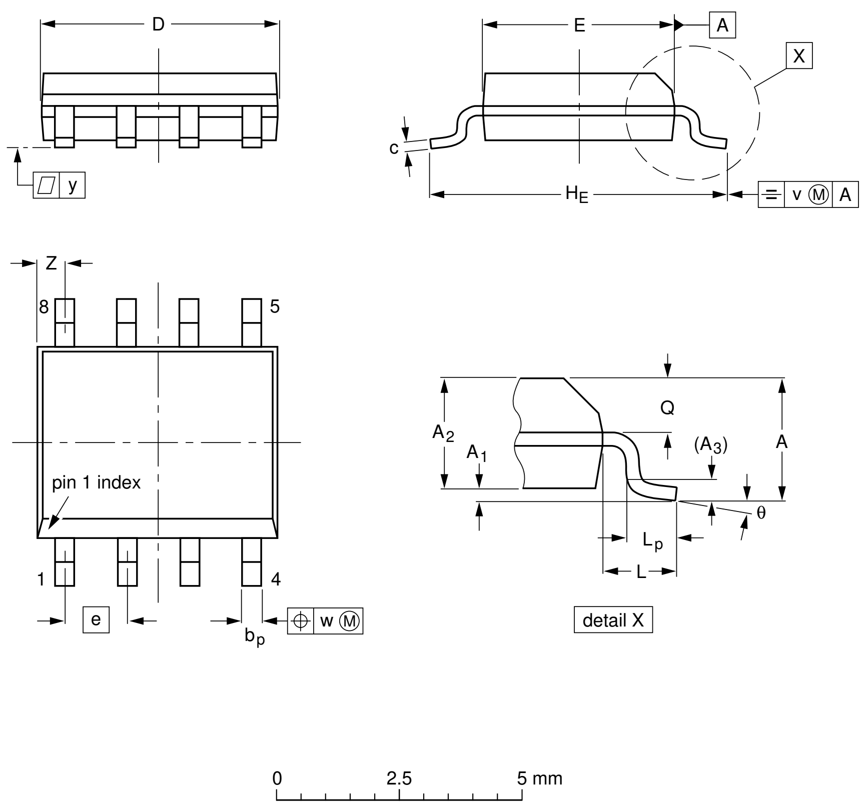


I_D = 12.5 A; V_{DD} =15 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

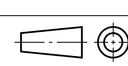
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

Fig 15. SOT96-1 (SO8).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010528	-	Product specification; initial version

11. Data sheet status

Data sheet status [1]	Product status [2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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