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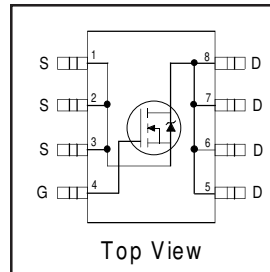
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Si4420DY

HEXFET[®] Power MOSFET

- N-Channel MOSFET
- Low On-Resistance
- Low Gate Charge
- Surface Mount
- Logic Level Drive

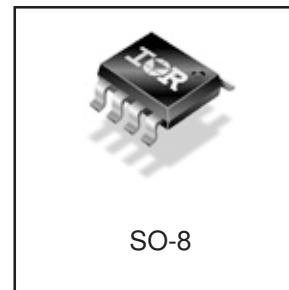


$V_{DSS} = 30V$
$R_{DS(on)} = 0.009\Omega$

Description

This N-channel HEXFET[®] power MOSFET is produced using International Rectifier's advanced HEXFET power MOSFET technology. The low on-resistance and low gate charge inherent to this technology make this device ideal for low voltage or battery driven power conversion applications

The SO-8 package with copper leadframe offers enhanced thermal characteristics that allow power dissipation of greater than 800mW in typical board mount applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	30	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	± 12.5	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	± 10	
I_{DM}	Pulsed Drain Current ①	± 50	
$P_D @ T_A = 25^\circ C$	Power Dissipation ③	2.5	W
$P_D @ T_A = 70^\circ C$	Power Dissipation ③	1.6	
	Linear Derating Factor	0.02	W/ $^\circ C$
E_{AS}	Single Pulse Avalanche Energy④	400	mJ
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	$^\circ C$

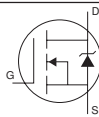
Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	50	$^\circ C/W$

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.028	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.009	Ω	V _{GS} = 10V, I _D = 12.5A ②
		—	—	0.013		V _{GS} = 4.5V, I _D = 10.5A ②
V _{GS(th)}	Gate Threshold Voltage	1.0	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	—	29	—	S	V _{DS} = 15V, I _D = 12.5A
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 30V, V _{GS} = 0V
		—	—	5.0		V _{DS} = 30V, V _{GS} = 0V, T _J = 55°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	—	52	78	nC	I _D = 12.5A
Q _{gs}	Gate-to-Source Charge	—	8.7	—		V _{DS} = 15V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	12	—		V _{GS} = 10V, See Fig. 6 ②
t _{d(on)}	Turn-On Delay Time	—	15	—	ns	V _{DD} = 15V
t _r	Rise Time	—	10	—		I _D = 1.0A
t _{d(off)}	Turn-Off Delay Time	—	55	—		R _G = 6.0Ω
t _f	Fall Time	—	47	—		R _D = 15Ω, ②
C _{iss}	Input Capacitance	—	2240	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1100	—		V _{DS} = 15V
C _{rss}	Reverse Transfer Capacitance	—	150	—		f = 1.0MHz, See Fig. 5②

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Diode Conduction)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	50		
V _{SD}	Diode Forward Voltage	—	—	1.1	V	T _J = 25°C, I _S = 2.3A, V _{GS} = 0V ②
t _{rr}	Reverse Recovery Time	—	52	78	ns	T _J = 25°C, I _F = 2.3A

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ③ When mounted on FR4 Board, t ≤ 10 sec
- ④ Starting T_J = 25°C, L = 13mH
R_G = 25Ω, I_{AS} = 8.9A. (See Figure 15)

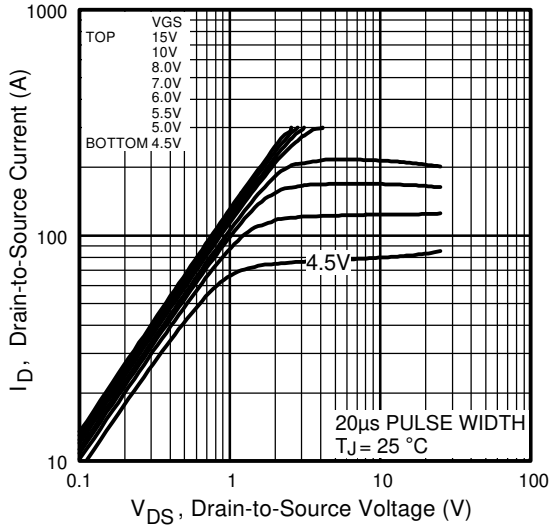


Fig 1. Typical Output Characteristics

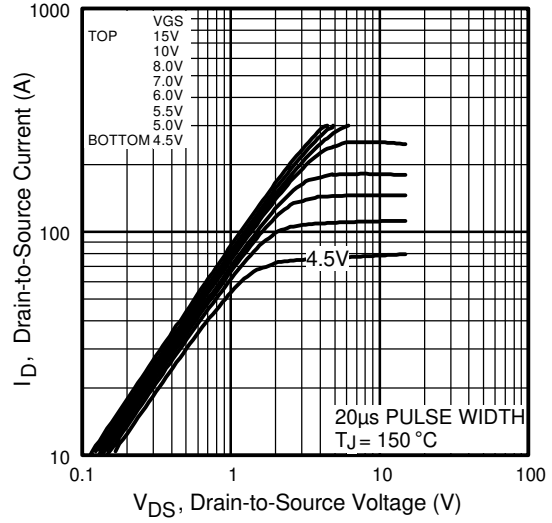


Fig 2. Typical Output Characteristics

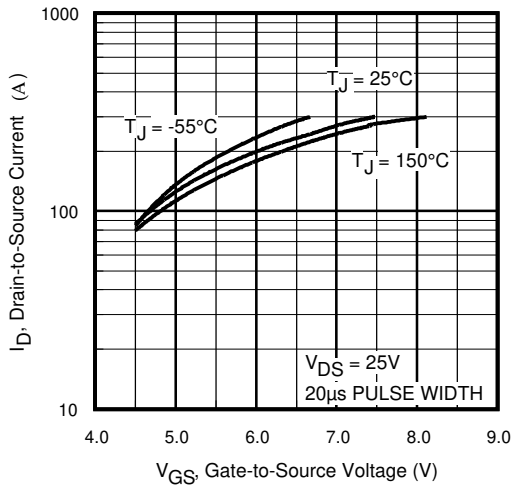


Fig 3. Typical Transfer Characteristics

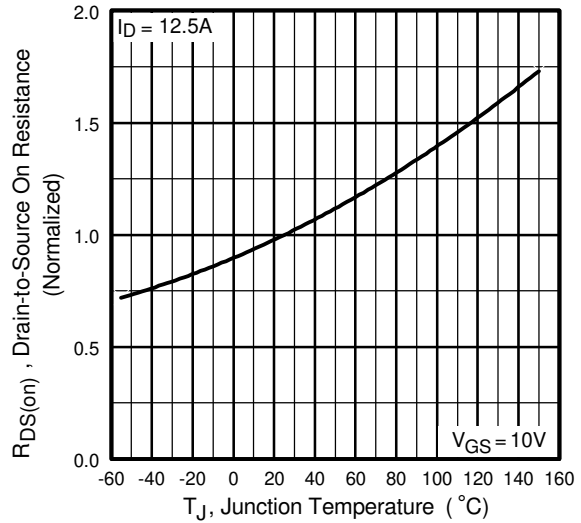


Fig 4. Normalized On-Resistance Vs. Temperature

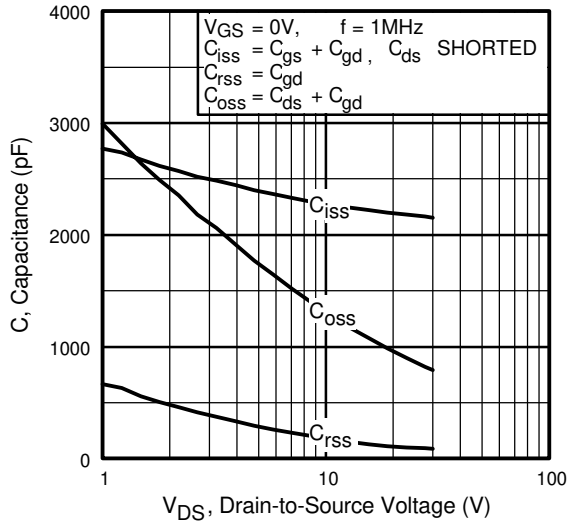


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

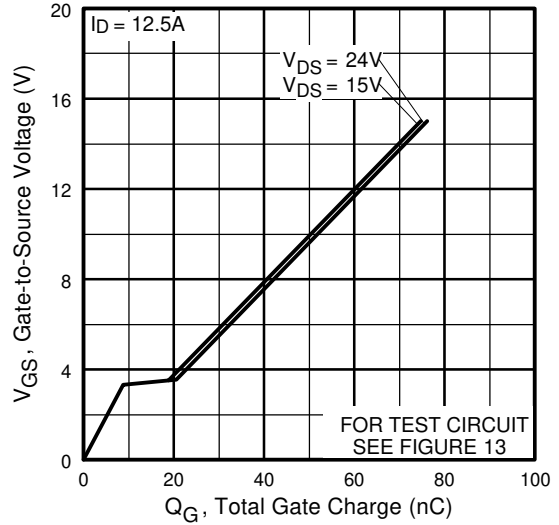


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

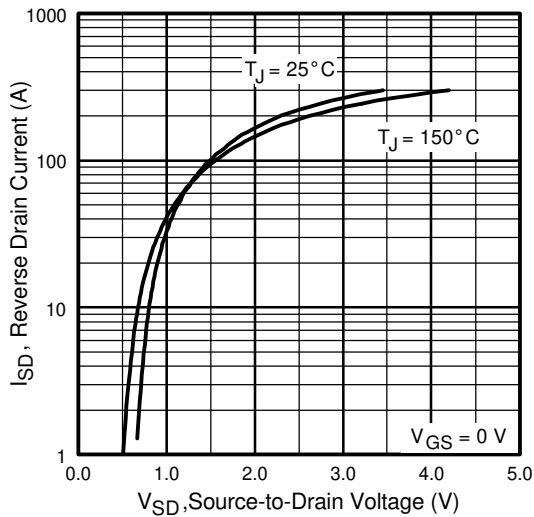


Fig 7. Typical Source-Drain Diode Forward Voltage

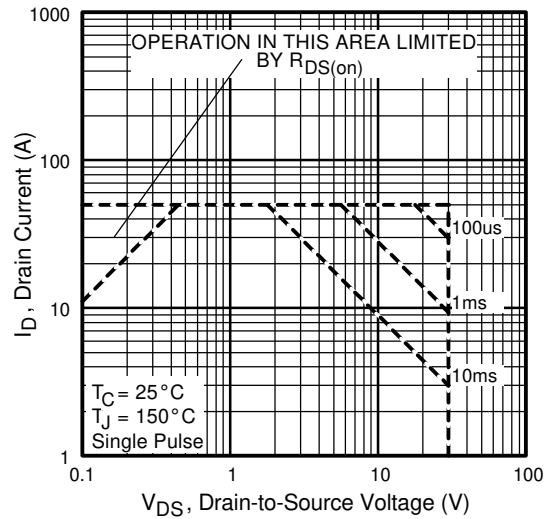


Fig 8. Maximum Safe Operating Area

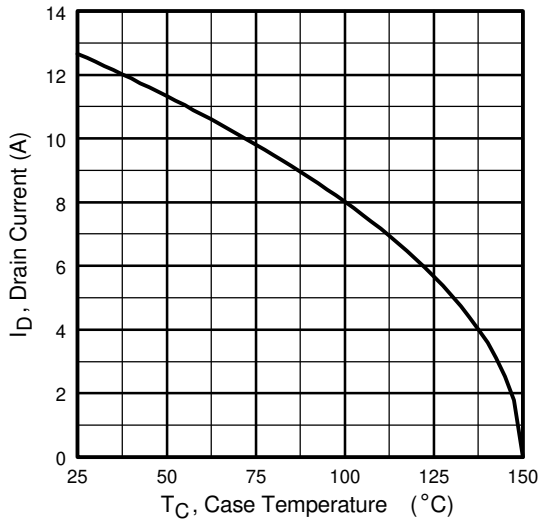


Fig 9. Maximum Drain Current Vs. Case Temperature

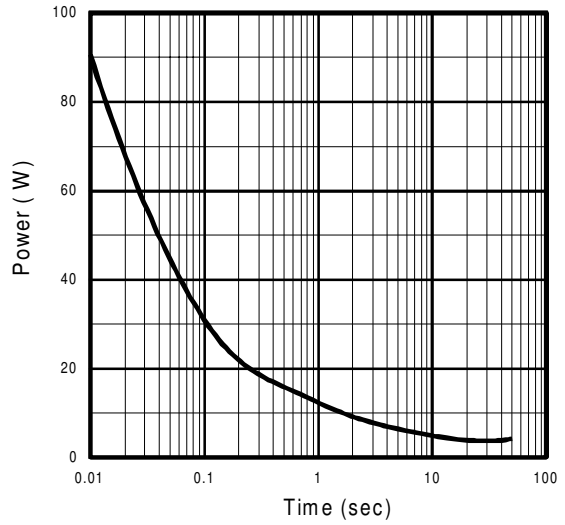


Fig 10. Typical Power Vs. Time

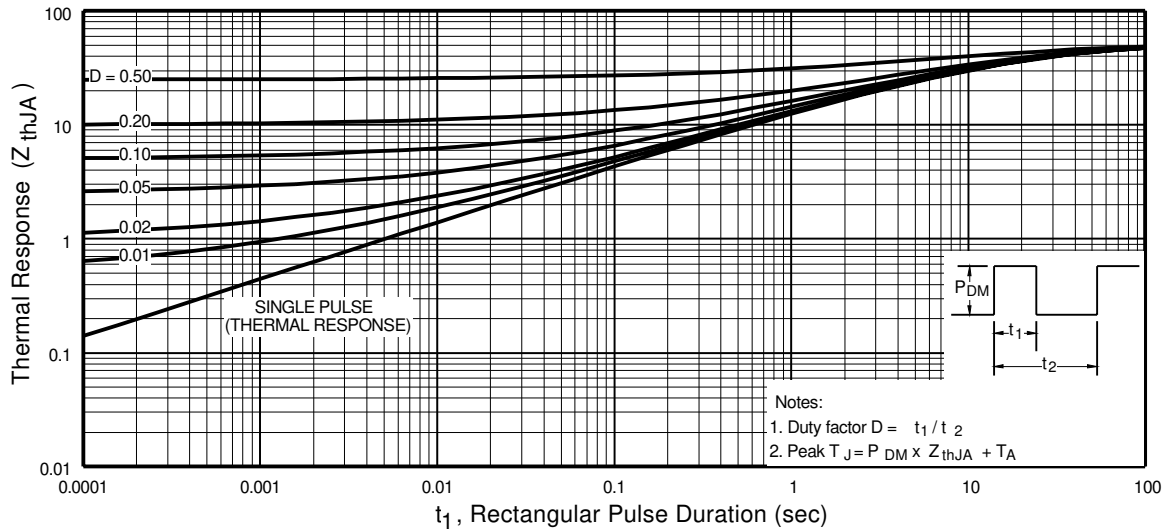


Fig 11. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

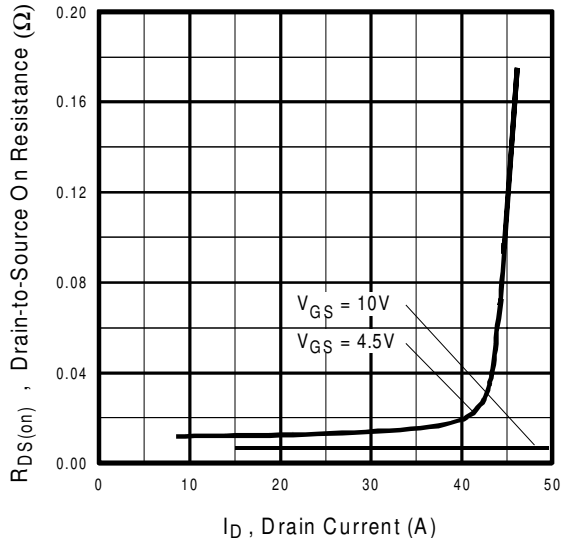


Fig 12. Typical On-Resistance Vs. Drain Current

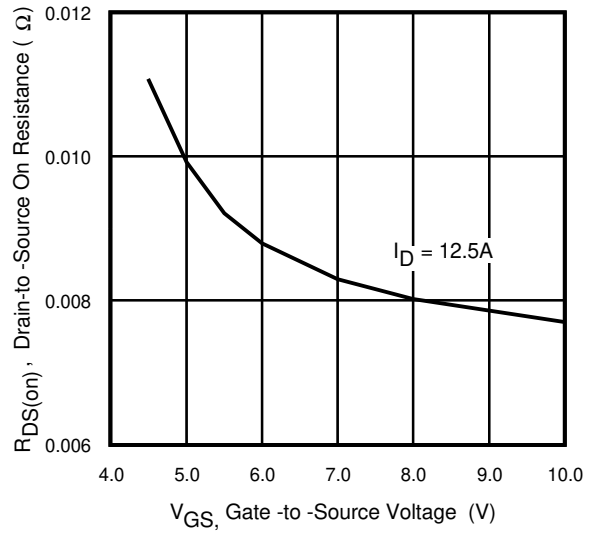


Fig 13. Typical On-Resistance Vs. Gate Voltage

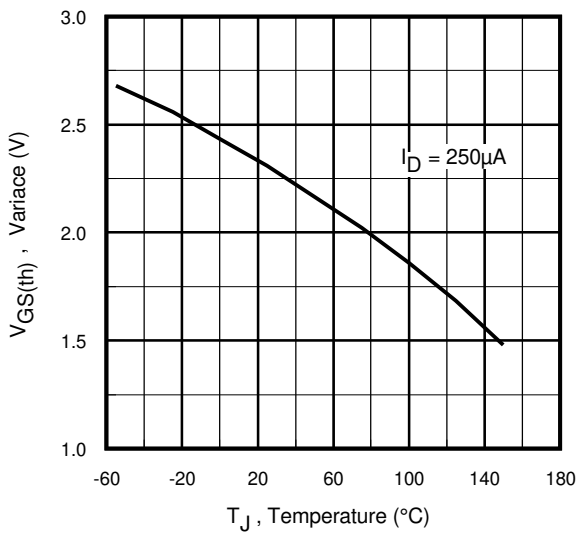


Fig 14. Typical Threshold Voltage Vs. Temperature

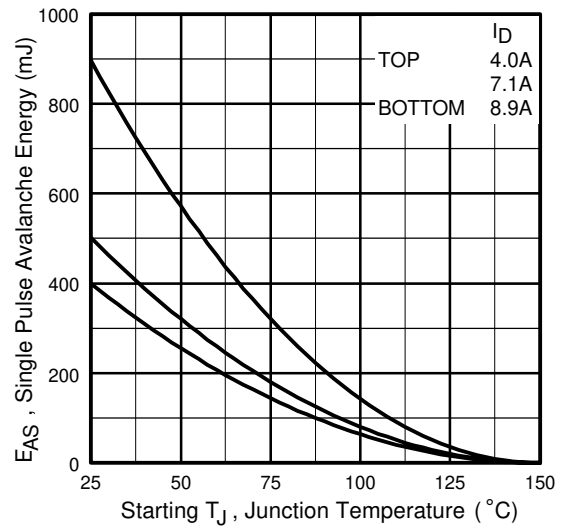
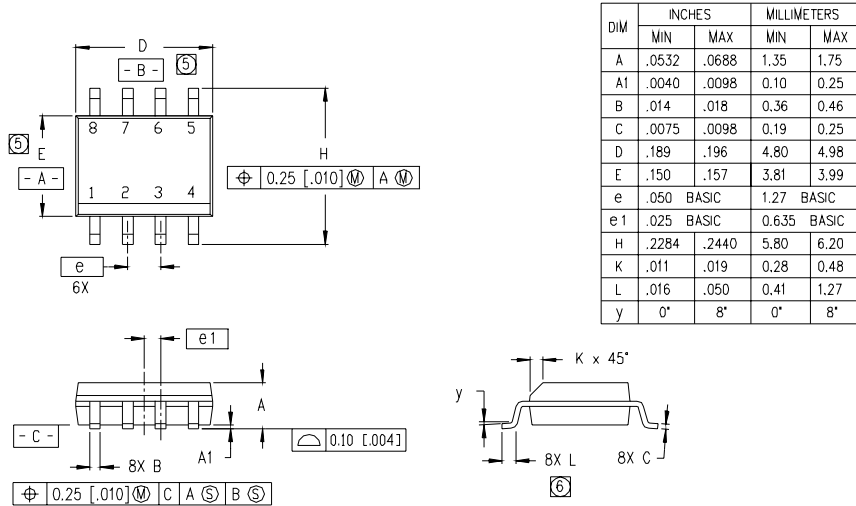


Fig 15. Maximum Avalanche Energy Vs. Drain Current

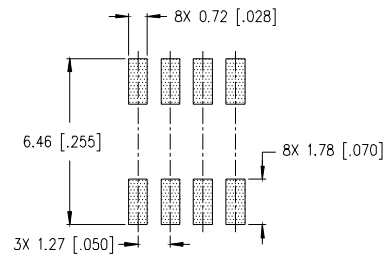
SO-8 Package Outline



NOTES:

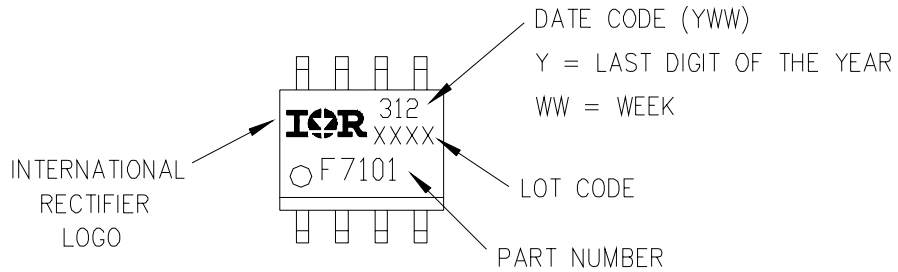
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
- ⑥ DIMENSION IS THE LENGTH OF LEAD FOR
SOLDERING TO A SUBSTRATE.

RECOMMENDED FOOTPRINT



SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101

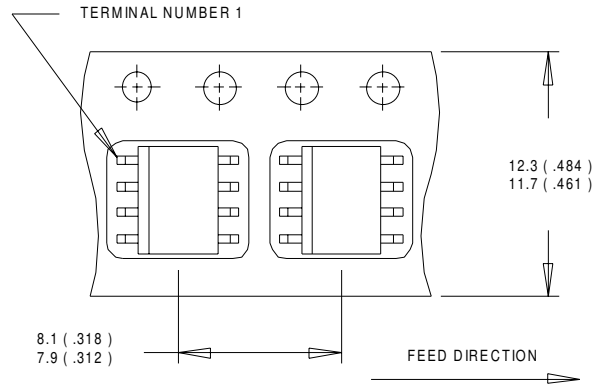


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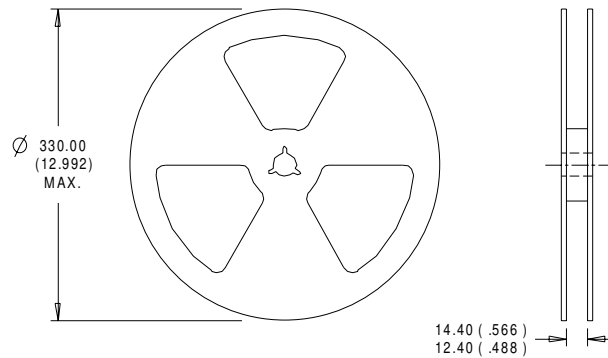
SO-8 Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
IR Rectifier

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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

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Data and specifications subject to change without notice. 1/2000