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Si4430

Si4430 ISM TRANSCEIVER

Features

- Frequency Range = 900–960 MHz
- Sensitivity = –118 dBm
- +13 dBm Max Output Power
  - Configurable –8 to +13 dBm
- Low Power Consumption
  - 18.5 mA receive
  - 28 mA @ +13 dBm transmit
- Data Rate = 1 to 128 kbps
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Digital RSSI
- Wake-on-radio
- Auto-frequency calibration (AFC)

- Antenna diversity and TR switch control
- Configurable packet structure
- Preamble detector
- TX and RX 64 byte FIFOs
- Low battery detector
- Temperature sensor and 8-bit ADC
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-Pin QFN package
- FSK, GFSK, and OOK modulation
- Low BOM
- Power-on-reset (POR)

Applications

- Remote control
- Home security & alarm
- Telemetry
- Personal data logging
- Toy control
- Tire pressure monitoring
- Wireless PC peripherals

- Remote meter reading
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
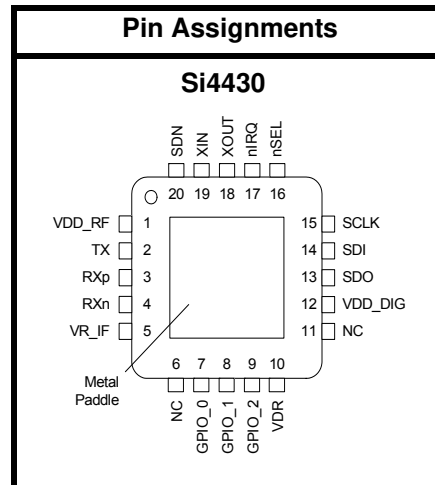- Health monitors
- Tag readers

Ordering Information:
See page 150.

Pin Assignments

Si4430

Patents pending

Description

Silicon Laboratories' Si4430 highly integrated, single chip wireless ISM transceiver is part of the EZRadioPRO™ family. The EZRadioPRO family includes a complete line of transmitters, receivers, and transceivers allowing the RF system designer to choose the optimal wireless part for their application.

The Si4430 offers advanced radio features including continuous frequency coverage from 900–960 MHz The Si4430's high level of integration offers reduced BOM cost while simplifying the overall system design. The extremely low receive sensitivity (–118 dBm) coupled with industry leading +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance.

Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, automatic packet handling, and preamble detection reduce overall current consumption and allow the use of lower-cost system MCUs. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.
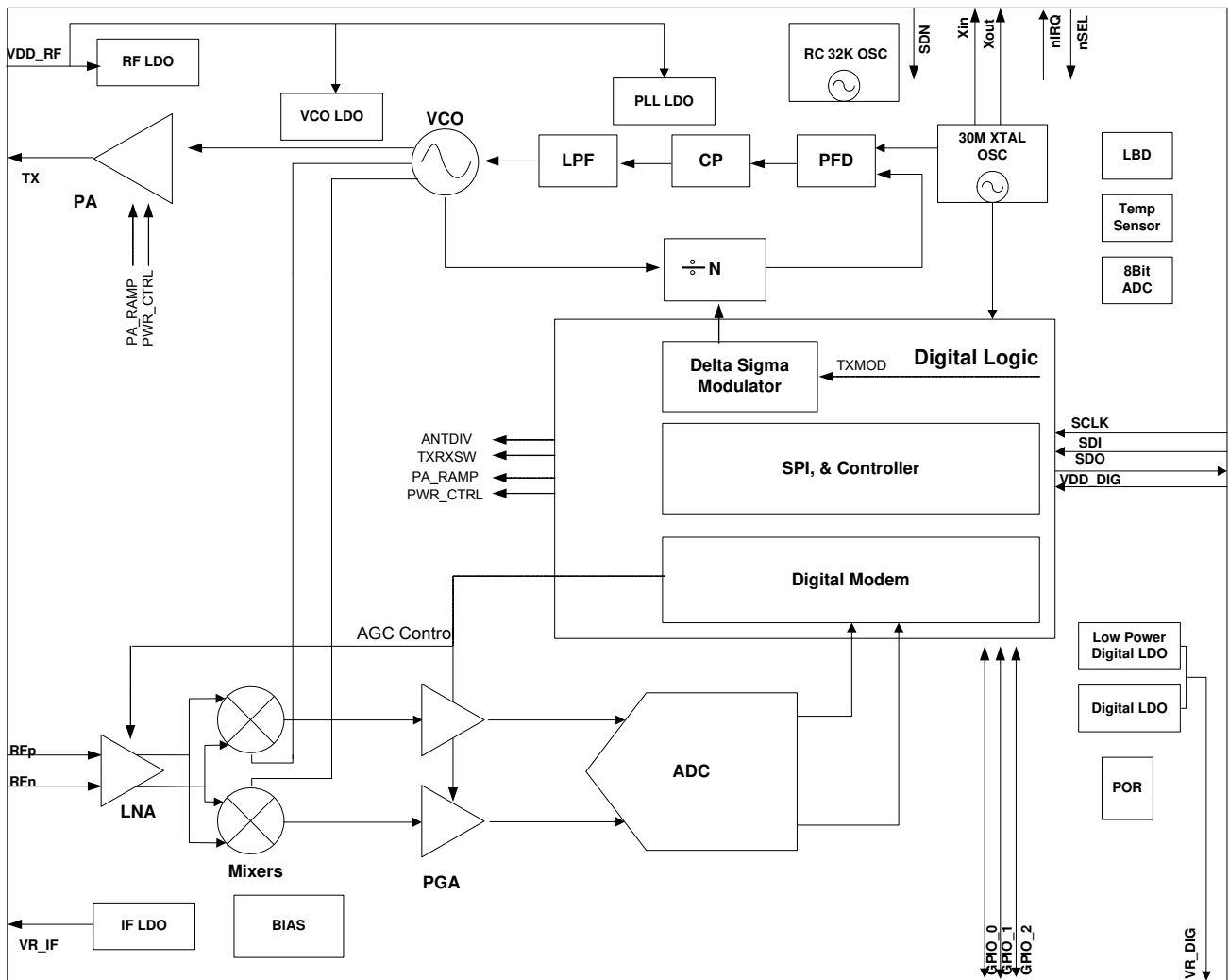
The Si4430's digital receive architecture features a high-performance ADC and DSP based modem which performs demodulation, filtering, and packet handling for increased flexibility and performance. This digital architecture simplifies system design while allowing for the use of lower-end MCUs. The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading ensuring compliance with ARIB regulations.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Si4430

Functional Block Diagram

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1. Electrical Specifications

Table 1. DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	—	Units
Supply Voltage Range	V_{dd}		1.8	3.0	—	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF[2]	—	10	—	nA
	$I_{Standby}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF[1]	—	400	—	nA
	I_{Sleep}	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF[1]	—	800	—	nA
	$I_{Sensor-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	$I_{Sensor-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled[1]	—	600	—	µA
TUNE Mode Current	I_{Tune}	Synthesizer and regulators enabled	—	9.5	—	mA
RX Mode Current	I_{RX}		—	18.5	—	mA
TX Mode Current	I_{TX_+13}	txpow[2:0] = 11 (+13 dBm), VDD = 3.3 V	—	28	—	mA
	I_{TX_+1}	txpow[2:0] = 00 (+1 dBm), VDD = 3.3 V	—	18	—	mA
Notes: 1. All specification guaranteed by production test unless otherwise noted. 2. Guaranteed by qualification.						

Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	F_{SYNTH}		900	—	960	MHz
Synthesizer Frequency Resolution[2]	F_{RES}		—	312.5	—	Hz
Reference Frequency	f_{REF}	$f_{crystal}$ / 3	—	10	—	MHz
Reference Frequency Input Level[2]	f_{REF_LV}	When using reference frequency instead of crystal. Measured peak-to-peak (V_{PP})	0.7	—	1.6	V
Synthesizer Settling Time[2]	t_{LOCK}	Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration	—	200	—	µs
Residual FM[2]	ΔF_{RMS}	Integrated over ±250 kHz bandwidth (500 Hz lower bound of integration)	—	2	4	kHz_{RMS}
Phase Noise[2]	$L\phi(f_M)$	ΔF = 10 kHz	—	–80	—	dBc/Hz
		ΔF = 100 kHz	—	–90	—	dBc/Hz
		ΔF = 1 MHz	—	–115	—	dBc/Hz
		ΔF = 10 MHz	—	–130	—	dBc/Hz

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

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Table 3. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range	F_{SYNTH}		900	—	960	MHz
RX Sensitivity	P_{RX_2}	(BER < 0.1%) (2 kbps, GFSK, BT = 0.5, $\Delta f = \pm 5$ kHz)[2]	—	−118	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, $\Delta f = \pm 20$ kHz)[2]	—	−107	—	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, $\Delta f = \pm 50$ kHz)[2]	—	−103	—	dBm
	P_{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, $\Delta f = \pm 62.5$ kHz)[1]	—	−101	—	dBm
	P_{RX_OOK}	(BER < 0.1%) (4.8 kbps, 350 kHz BW, OOK)[2]	—	−110	—	dBm
		(BER < 0.1%) (40 kbps, 400 kHz BW, OOK)[1]	—	−102	—	dBm
RX Bandwidth[2]	BW		2.6	—	620	kHz
Residual BER Performance[2]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm
Input Intercept Point, 3rd Order[2]	$IIP3_{RX}$	$f_1 = 915$ MHz, $f_2 = 915$ MHz, $P_1 = P_2 = -40$ dBm	—	−20	—	dBm
LNA Input Impedance[2] (Unmatched, measured differentially across RX input pins)	$R_{IN\text{-}RX}$	915 MHz	—	40–55	—	Ω
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[2] (BER < 0.1%)	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps $\Delta F = 20$ kHz GFSK with BT = 0.5, channel spacing = 150 kHz	—	−31	—	dB
±2-Ch Offset Selectivity[2] (BER < 0.1%)	$C/I_{2\text{-}CH}$		—	−35	—	dB
≥ ±3-Ch Offset Selectivity[2] (BER < 0.1%)	$C/I_{3\text{-}CH}$		—	−40	—	dB
Blocking at 1 MHz[2]	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps $\Delta F = 20$ kHz GFSK with BT = 0.5	—	−52	—	dB
Blocking at 4 MHz[2]	$4M_{BLOCK}$		—	−56	—	dB
Blocking at 8 MHz[2]	$8M_{BLOCK}$		—	−63	—	dB
Image Rejection[2]	Im_{REJ}	IF=937 kHz	—	−30	—	dB
Spurious Emissions[2]	P_{OB_RX1}	Measured at RX pins (LO feed through)	—	—	−54	dBm

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 4. Transmitter AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range[1]	F_{SYNTH}		900	—	960	MHz
FSK Modulation Data Rate[2]	DR_{FSK}		1	—	128	kbps
OOK Modulation Data Rate[2]	DR_{OOK}		1.2	—	40	kbps
Modulation Deviation[1]	Δf	Production tests maximum limit of 320 kHz	±0.625		±320	kHz
Modulation Deviation Resolution	Δf_{RES}		—	0.625	—	kHz
Output Power Range[1]	P_{TX}	Power control by txpow[2:0] Register Production test at txpow[2:0] = 111 Tested at 915 MHz	–8	—	+13	dBm
TX RF Output Steps[2]	ΔP_{RF_OUT}	controlled by txpow[2:0] Register	—	3	—	dB
TX RF Output Level Variation vs. Voltage[2]	ΔP_{RF_V}	Measured from VDD=3.6 V to VDD=1.8 V	—	2	—	dB
TX RF Output Level[2] Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2	—	dB
TX RF Output Level Variation vs. Frequency[2]	ΔP_{RF_FREQ}	Measured across any one frequency band	—	1	—	dB
Transmit Modulation Filtering[2]	B*T	Gaussian Filtering Bandwith Time Product	—	0.5	—	
Spurious Emissions[2]	P_{OB-TX1}	P_{OUT} = 11 dBm, Frequencies <1 GHz	—	—	–54	dBm
	P_{OB-TX2}	1–12.75 GHz, excluding harmonics	—	—	–54	dBm
Harmonics[2]	P_{2HARM}	Using Reference Design TX Matching Network and Filter with Max Output Power (+13 dBm). Harmonics reduce linearly with output power	—	—	–42	dBm
	P_{3HARM}		—	—	–42	dBm

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

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Table 5. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature Sensor Accuracy[2]	TS_A	When calibrated using temp sensor offset register	—	0.5	—	°C
Temperature Sensor Sensitivity[2]	TS_S		—	5	—	mV/°C
Low Battery Detector Resolution[2]	LBD_{RES}		—	50	—	mV
Low Battery Detector Conversion Time[2]	LBD_{CT}		—	250	—	µs
Microcontroller Clock Output Frequency	MC	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768K	—	30M	Hz
General Purpose ADC Accuracy[2]	ADC_{ENB}		—	8	—	bit
General Purpose ADC Resolution[2]	ADC_{RES}		—	4	—	mV
Temp Sensor & General Purpose ADC Conversion Time[2]	ADC_{CT}		—	305	—	µsec
30 MHz XTAL Start-Up time	t_{30M}		—	1	—	ms
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	97	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	6	—	sec
32 kHz XTAL Accuracy[2]	$32K_{RES}$		—	100	—	ppm
32 kHz RC OSC Accuracy[2]	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	16	—	ms
Software Reset Time[2]	t_{soft}		—	100	—	µs

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 6. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 5 pF	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 5 pF	—	—	8	ns
Input Capacitance	C_{IN}		—	—	1	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} – 0.6	—	—	V
Logic Low Level Input Voltage	V_{IL}			—	0.6	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	−100	—	100	nA
Logic High Level Output Voltage	V_{OH}	I_{OH}<1 mA source, V_{DD}=1.8 V	V_{DD} – 0.6	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OL}<1 mA sink, V_{DD}=1.8 V	—	—	0.6	V
Note: All specification guaranteed by production test unless otherwise noted.						

Table 7. GPIO Specifications (GPIO_0, GPIO_1, and GPIO_2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Input Capacitance	C_{IN}		—	—	1	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} – 0.6	—		V
Logic Low Level Input Voltage	V_{IL}		—	—	0.6	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	−100	—	100	nA
Input Current If Pullup is Activated	I_{INP}	V_{IL}=0 V	5	—	25	µA
Maximum Output Current	I_{OmaxLL}	DRV<1:0>=LL	0.1	0.5	0.8	mA
	I_{OmaxLH}	DRV<1:0>=LH	0.9	2.3	3.5	mA
	I_{OmaxHL}	DRV<1:0>=HL	1.5	3.1	4.8	mA
	I_{OmaxHH}	DRV<1:0>=HH	1.8	3.6	5.4	mA
Logic High Level Output Voltage	V_{OH}	I_{OH}< I_{Omax} source, V_{DD}=1.8 V	V_{DD} – 0.6	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OL}< I_{Omax} sink, V_{DD}=1.8 V	—	—	0.6	V
Note: All specification guaranteed by production test unless otherwise noted.						

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Table 8. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
V_{DD} to GND on TX Output Pin	–0.3, +8.0	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	–55 to +125	°C
Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device. Power Amplifier may be damaged if switched on without proper load or termination connected.		

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Si4430

1.1. Definition of Test Conditions

Production Test Conditions:

T_A = +25 °C

V_{DD} = +3.3 VDC

External reference signal (XOUT) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC

Production test schematic (unless noted otherwise)

All RF input and output levels referred to the pins of the Si4430 (not the RF module)

Extreme Test Conditions:

T_A = –40 to +85 °C

V_{DD} = +1.8 to +3.6 VDC

External reference signal (XOUT) = 0.7 to 1.6 V_{PP} at 30 MHz centered around 0.8 VDC

Production test schematic (unless noted otherwise)

All RF input and output levels referred to the pins of the Si4430 (not the RF module)

Test Notes:

All electrical parameters with Min/Max values are guaranteed by one (or more) of the following test methods. Electrical parameters shown with only Typical values are not guaranteed.

- Guaranteed by design and/or simulation but not tested.
- Guaranteed by Engineering Qualification testing at Extreme Test Conditions.
- Guaranteed by 100% Production Test Screening at Production Test Conditions.

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2. Functional Description

The Si4430 is a 100% CMOS ISM wireless transceiver with continuous frequency tuning over the complete 900–960 MHz band. The wide operating voltage range of 1.8–3.6 V and low current consumption makes the Si4430 and ideal solution for battery powered applications.

The Si4430 operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion, image-reject mixer to downconvert the 2-level FSK/GFSK/OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance $\Delta\Sigma$ ADC allowing filtering, demodulation, slicing, error correction, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is then output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and $\Delta\Sigma$ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency, frequency deviation, and Gaussian filtering at any frequency between 900–960 MHz. The transmit FSK data is modulated directly into the $\Delta\Sigma$ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The PA output power can be configured between –8 and +13 dBm in 3 dB steps. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The Si4430 supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Antenna diversity is completely integrated into the Si4430 and can improve the system link budget by 8–10 dB, resulting in substantial range increases depending on the environmental conditions.

The Si4430 is designed to work with a microcontroller, crystal, and a few passives to create a very low cost system as shown Figure 1. Voltage regulators are integrated on-chip which allow for a wide range of operating supply voltage conditions from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with the microcontroller. Three configurable general purpose

I/Os are available for use to tailor towards the needs of the system. A more complete list of the available GPIO functions is shown in "8. Auxiliary Functions" on page 53 but just to name a few, microcontroller clock output, Antenna Diversity, POR, and specific interrupts. A limited number of passive components are needed to match the LNA and PA.

The application shown in Figure 1 is designed for a system with an TX/RX direct-tie configuration without the use of a TX/RX switch. Most lower power applications will use this configuration. A direct-tie reference design is available from Silicon Laboratories applications support.

For applications seeking improved performance in the presence of multipath fading antenna diversity can be used. Antenna diversity includes a switch to select the optimal antenna between a pair of antennas for improved performance. The Antenna Diversity Control Algorithm is completely integrated into the chip and is discussed further in Figure 24 on page 55. A complete Antenna Diversity reference design is available from Silicon Laboratories applications support.

An application example with a separate RX and TX antenna is shown in Figure 31, "Split RF I/Os with Separated TX and RX Connectors—Schematic," on page 67. This example is used for testing of the TX and RX paths in a lab environment and shows, conceptually, the matching of the TX and RX antennas.
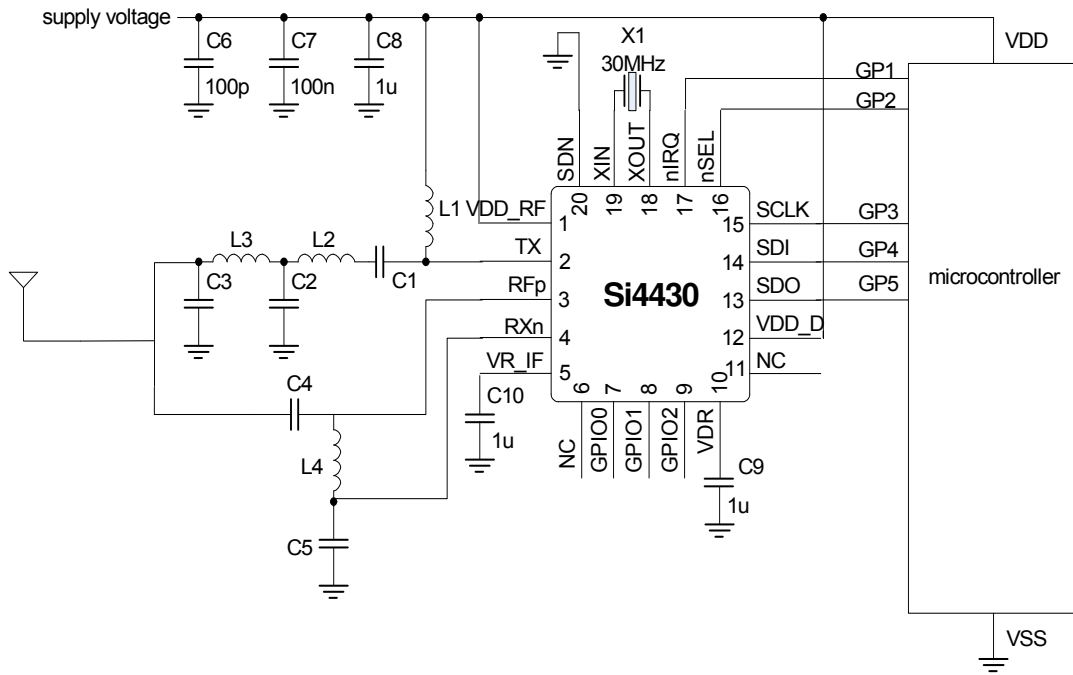
Si4430

Programmable load capacitors for X1 are integrated.

R1, L1-L5 and C1-C4 values depend on frequency band, antenna impedance, output power and supply voltage range.

Figure 1. Si4430 RX/TX Direct-Tie Application Example

Preliminary Rev. 0.4

2.1. Operating Modes

The Si4430 provides several modes of operation which can be used to optimize the power consumption of the device application. Depending upon the system communication protocol, the optimal trade-off between the radio wake time and power consumption can be achieved.

Table 9 summarizes the modes of operation of the Si4430. In general, any given mode of operation may be classified as an Active mode or a Power Saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI in order to optimize the average current consumption. An "X" in any cell means that, in the given mode of operation, that block can be independently programmed to be either ON or OFF, without noticeably affecting the current consumption. The SPI circuit block includes the SPI interface and the register space. The 32 kHz OSC circuit block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator, and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor, general purpose ADC, and low-battery detector.

Table 9. Operating Modes

Mode Name	Circuit Blocks								
	Digital LDO	SPI	32 kHz OSC	AUX	30 MHz XTAL	PLL	PA	RX	I_{VDD}
Shutdown	OFF (Register contents lost)	OFF	OFF	OFF	OFF	OFF	OFF	OFF	10 nA
Standby	ON (Register contents retained)	ON	OFF	OFF	OFF	OFF	OFF	OFF	400 nA
Sleep		ON	ON	X	OFF	OFF	OFF	OFF	800 nA
Sensor		ON	X	ON	OFF	OFF	OFF	OFF	1 µA
Ready		ON	X	X	ON	OFF	OFF	OFF	600 µA
Tuning		ON	X	X	ON	ON	OFF	OFF	9.5 mA
Transmit		ON	X	X	ON	ON	ON	OFF	28 mA*
Receive		ON	X	X	ON	ON	OFF	ON	18.5 mA
*Note: 28 mA at +13 dBm.									

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si4430 communicates with the host MCU over a 3 wire SPI interface: SCLK, SDI, and nSEL. The host MCU can also read data from internal registers on the SDO output pin. A SPI transaction is a 16-bit sequence which consists of a Read-Write ($\overline{\text{R}}$/W) select bit, followed by a 7-bit address field (ADDR), and an 8-bit data field (DATA), as demonstrated in Figure 2. The 7-bit address field supports reading from or writing to one of the 128, 8-bit control registers. The $\overline{\text{R}}$/W select bit determines whether the SPI transaction is a write or read transaction. If $\overline{\text{R}}$/W = 1, it signifies a WRITE transaction, while $\overline{\text{R}}$/W = 0 signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4430 every eight clock cycles. The timing parameters for the SPI interface are shown in Table 10. The SCLK rate is flexible with a maximum rate of 10 MHz.
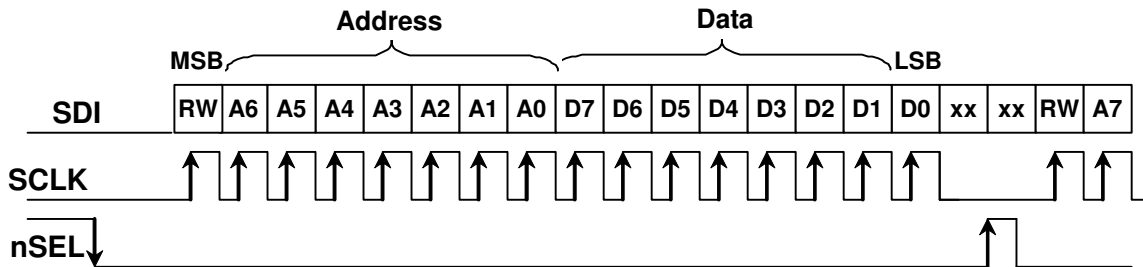
Figure 2. SPI Timing

Table 10. Serial Interface Timing Parameters

Symbol	Parameter	Min (nsec)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

To read back data from the Si4430, the $\overline{\text{R}}$/W bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored when $\overline{\text{R}}$/W = 0. The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 3. After the READ function is completed the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pullup.
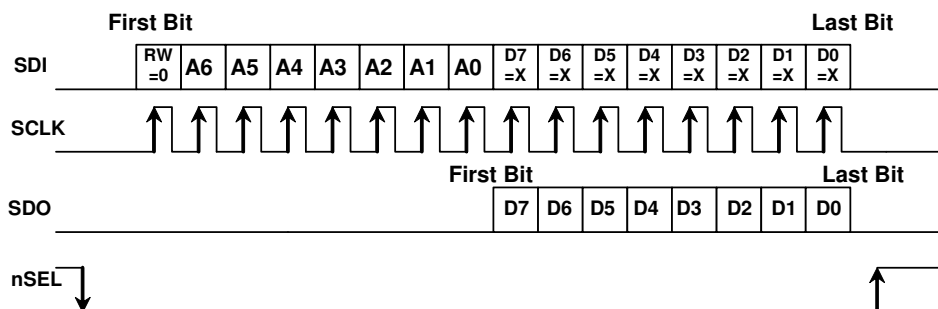
Figure 3. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode which will allows for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An SPI burst write transaction is demonstrated in Figure 4 and burst read in Figure 3. As long as nSEL is held low, input data will be latched into the Si4430 every eight SCLK cycles. A burst read transaction is also demonstrated in Figure 5.
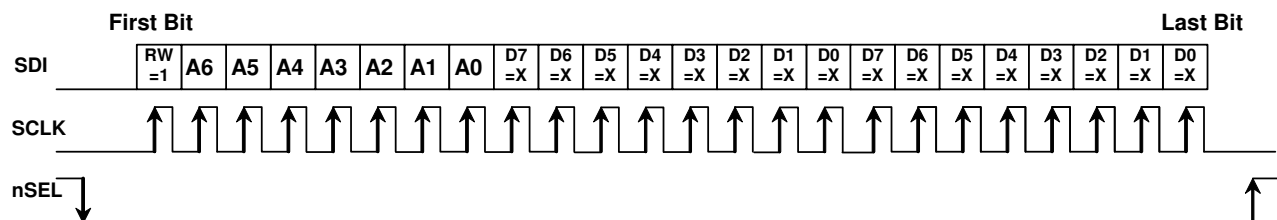
Figure 4. SPI Timing—Burst Write Mode
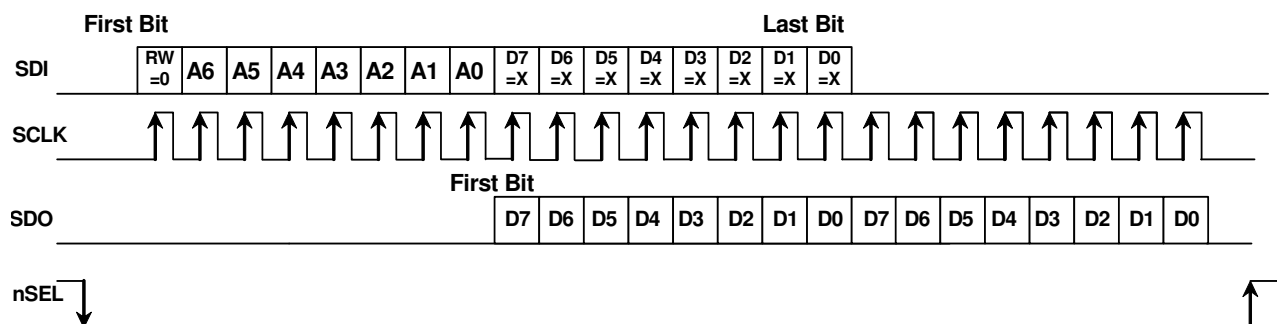
Figure 5. SPI Timing—Burst Read Mode

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3.2. Operating Mode Control

There are four primary states in the Si4430 radio state machine: SHUTDOWN, IDLE, TX, and RX (see Figure 6). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. "Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected. The TX and RX state may be reached automatically from any of the IDLE states by setting the txon/rxon bits in "Register 07h. Operating Mode and Function Control 1". Table 11 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode.

The output of the LPLDO is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the digital modem, crystal oscillator, and SPI and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.

*Five Different Options for IDLE
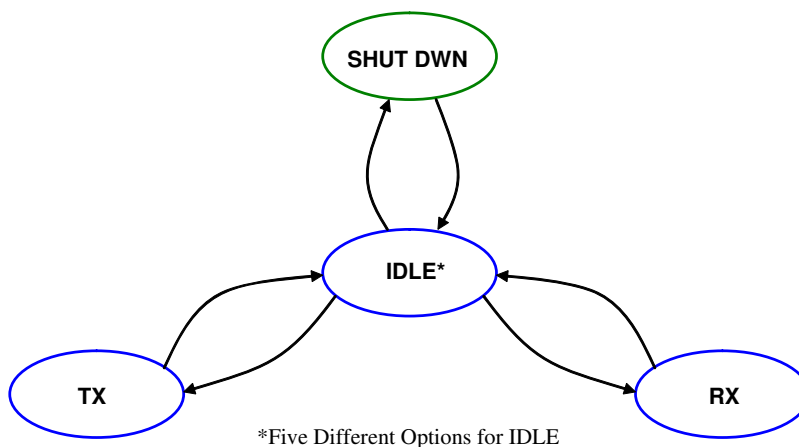
Figure 6. State Machine Diagram

Table 11. Operating Modes

State/Mode	xtal	pll	wt	LBD or TS	Response Time to		Current in State /Mode [µA]
					TX	RX	
Shut Down State	X	X	X	X	16.21 ms	16.21 ms	10 nA
Idle States:							
Standby Mode	0	0	0	0	1.21 ms	1.21 ms	400 nA
Sleep Mode	0	0	1	0			800 nA
Sensor Mode	0	0	X	1			1 µA
Ready Mode	1	0	X	X	210 µs	210 µs	600 µA
Tune Mode	1	1	X	X	200 µs	200 µs	9.5 mA
TX State	1	1	X	X	NA	200 µs	28 mA @ +13 dBm
RX State	1	1	X	X	200 µs	NA	18.5 mA

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3.2.1. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 10 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

3.2.2. Idle State

There are five different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX/RX mode. This tradeoff is shown in Table 11. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption possible with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The standby mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "8.6. Wake-Up Timer" on page 61 for more information on the Wake-Up-Timer. Sleep mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.3. SENSOR Mode

In SENSOR Mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 and the temperature sensor can be enabled by setting ents = 1 in "Register 07h. Operating Mode and Function Control 1". See "8.4. Temperature Sensor" on page 58 and "8.5. Low Battery Detector" on page 60 for more information on these features. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to the TX or RX mode by eliminating the crystal start-up time. Ready mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled. This is done by setting "Register 62h. Crystal Oscillator/Power-on-Reset Control" to a value of 02h. To exit ready mode, bufovr (bit 1) of this register must be set back to 0.

3.2.2.5. TUNE Mode

In TUNE Mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for Frequency Hopping Systems (FHS). Tune mode is entered by setting pllon = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

3.2.3. TX State

The TX state may be entered from any of the IDLE modes when the txon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA to prevent unwanted spectral splatter. The following sequence of events will occur automatically when going from STANDBY mode to TX mode by setting the txon bit.

1. Enable the Main Digital LDO and the Analog LDOs.

2. Start up crystal oscillator and wait until ready (controlled by timer).

3. Enable PLL.

4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").

5. Wait until PLL settles to required transmit frequency (controlled by timer).

6. Activate Power Amplifier and wait until power ramping is completed (controlled by timer).

7. Transmit Packet.

The first few steps may be eliminated depending on which IDLE mode the chip is configured to prior to setting the txon bit. By default, the VCO and PLL are calibrated every time the PLL is enabled. If the ambient temperature is constant and the same frequency band is being used these functions may be skipped by setting the appropriate bits in "Register 55h. Calibration Control".

3.2.4. RX State

The RX state may be entered from any of the Idle modes when the rxon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the Main Digital LDO and the Analog LDOs.

2. Start up crystal oscillator and wait until ready (controlled by timer).

3. Enable PLL.

4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").

5. Wait until PLL settles to required transmit frequency (controlled by timer).

6. Enable receive circuits: LNA, mixers, and ADC.

7. Calibrate ADC (RC calibration).

8. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

3.2.5. Device Status

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
02	R	Device Status	ffovfl	ffunfl	rxffem	headerr			cps[1]	cps[0]	—

The operational status of the chip can be read from "Register 02h. Device Status".

3.3. Interrupts

The Si4430 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has been detected by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h–04h) containing the active Interrupt Status bit; the nIRQ output signal will then be reset until the next change in status is detected. All of the interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h–06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs inside of the chip it will not trigger the nIRQ pin, but the status may still be read correctly at anytime in the Interrupt Status registers.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
03	R	Interrupt Status 1	ifferr	itxffafull	itxffaem	irxffafull	iext	ipksent	ipkvalid	icrcerror	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	entxffafull	entxffaem	enrxffafull	enext	enpksent	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h

See "Register 03h. Interrupt/Status 1," on page 79 and "Register 04h. Interrupt/Status 2," on page 81 for a complete list of interrupts.

3.4. Device Code

The device version code is readable from "Register 01h. Version Code (VC)". This is a read only register.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.	Notes
01	R	Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	00h	DV

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3.5. System Timing

The system timing for TX and RX modes is shown in Figures 8 and 7. The timing is shown transitioning from STANDBY mode to TX mode and going automatically through the built-in sequencer of required steps. If a small range of frequencies is being used and the temperature range is fairly constant a calibration may only be needed at the initial power up of the device. The relevant system timing registers are shown below.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
53	R/W	PLL Tune Time			pllts[4:0]				pllt0[2:0]		45h
54	R/W	Reserved 1	X	X	X	X	X	X	X	X	00h
55	R/W	Calibration Control		xtal-starthalf	adccal-done	enrcfcal	rccal	vco-caldp	vcocal	skip-vco	04h

The VCO will automatically calibrate at every frequency change or power up. The VCO CAL may also be forced by setting the vcocal bit. The 32.768 kHz RC oscillator is also automatically calibrated but the calibration may also be forced. The enrcfcal will enable the RC Fine Calibration which will occur every 30 seconds. The rccal bit will force a complete calibration of the RC oscillator which will take approximately 2 ms. The PLL T0 time is to allow for bias settling of the VCO, the default for this should be adequate. The PLL TS time is for the settling time of the PLL, which has a default setting of 200 µs. This setting should be adequate for most applications but may be reduced if small frequency jumps are used. For more information on the PLL register configuration options, see "Register 53h. PLL Tune Time," on page 126 and "Register 55h. Calibration Control," on page 127.
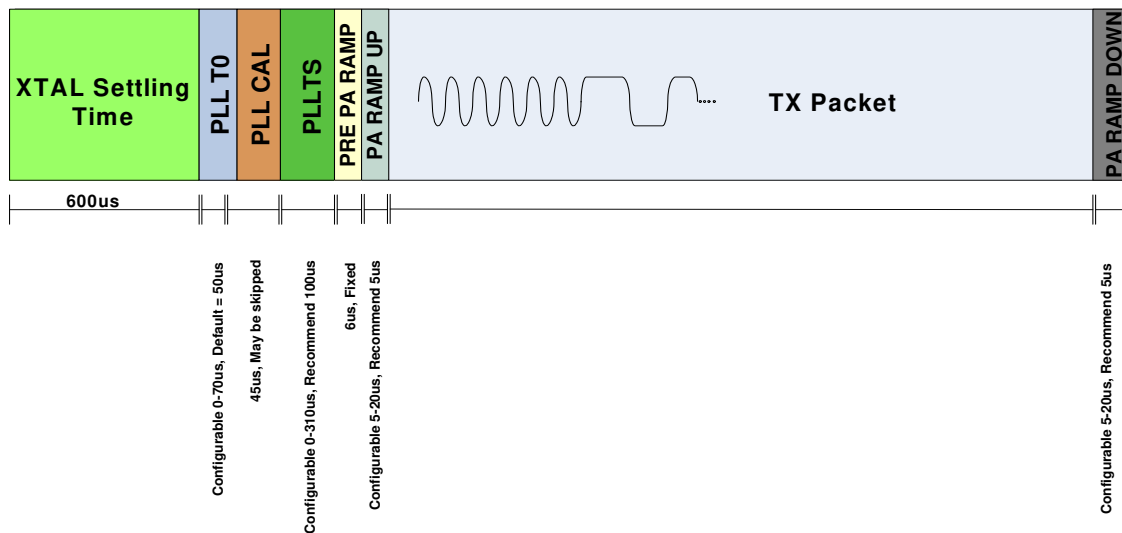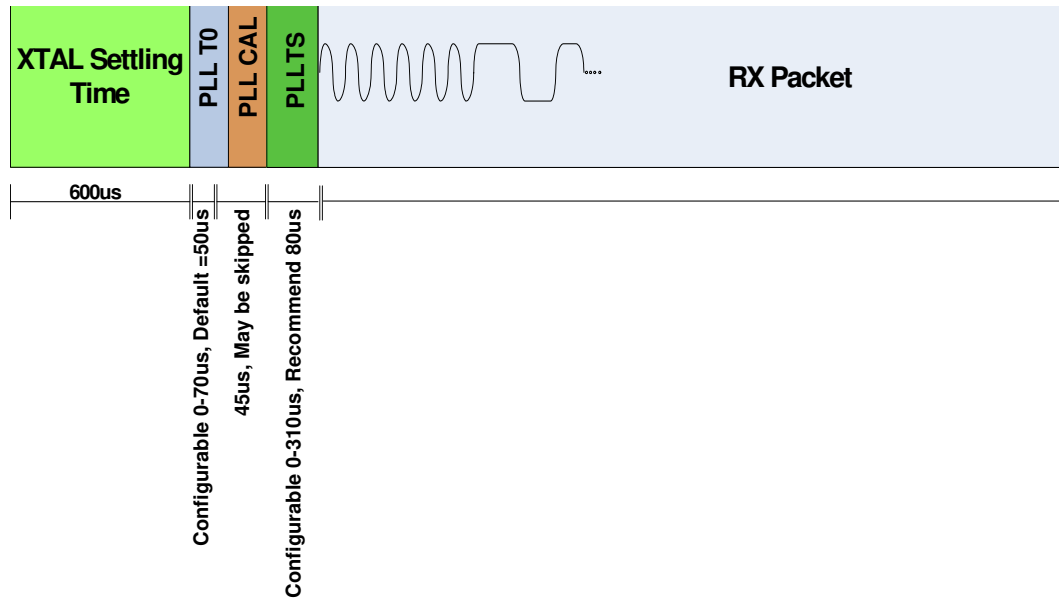

Figure 7. TX Timing

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Figure 8. RX Timing

The figure shows a timeline with the following segments:
- **XTAL Settling Time** (600us)
- **PLL T0** — Configurable 0-70us, Default =50us
- **PLL CAL** — 45us, May be skipped
- **PLLTS** — Configurable 0-310us, Recommend 80us
- **RX Packet**

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