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## Si4430/31/32 ISM TRANSCEIVER

### Features

- Frequency Range
  - 240–930 MHz (Si4431/32)
  - 900–960 MHz (Si4430)
- Sensitivity = –121 dBm
- Output power range
  - +20 dBm Max (Si4432)
  - +13 dBm Max (Si4430/31)
- Low Power Consumption
  - 18.5 mA receive
  - 30 mA @ +13 dBm transmit
  - 85 mA @ +20 dBm transmit
- Data Rate = 0.123 to 256 kbps
- FSK, GFSK, and OOK modulation
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Digital RSSI
- Wake-up timer
- Auto-frequency calibration (AFC)
- Power-on-reset (POR)
- Antenna diversity and TR switch control
- Configurable packet handler
- Preamble detector
- TX and RX 64 byte FIFOs
- Low battery detector
- Temperature sensor and 8-bit ADC
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-Pin QFN package
- Low BOM

### Applications

- Remote control
- Home security & alarm
- Telemetry
- Personal data logging
- Toy control
- Tire pressure monitoring
- Wireless PC peripherals
- Remote meter reading
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Tag readers

### Description

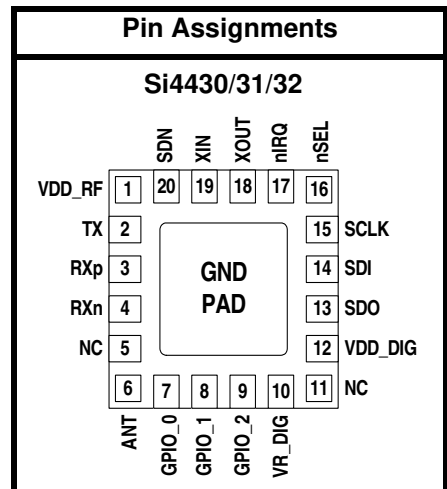
Silicon Laboratories' Si4430/31/32 devices are highly integrated, single chip wireless ISM transceivers. The high-performance EZRadioPRO® family includes a complete line of transmitters, receivers, and transceivers allowing the RF system designer to choose the optimal wireless part for their application.

The Si4430/31/32's high level of integration offers reduced BOM cost while simplifying the overall system design. The extremely low receive sensitivity (–121 dBm) coupled with industry leading +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance.

The Si4430/31/32 offers advanced radio features including continuous frequency coverage from 240–960 MHz in 156 Hz or 312 Hz steps allowing precise tuning control. Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, automatic packet handling, and preamble detection reduce overall current consumption and allow the use of lower-cost system MCUs. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.

The Si4430/31/32's digital receive architecture features a high-performance ADC and DSP based modem which performs demodulation, filtering, and packet handling for increased flexibility and performance. The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading ensuring compliance with global regulations including FCC, ETSI, ARIB, and 802.15.4d regulations.

An easy-to-use calculator is provided to quickly configure the radio settings, simplifying customer's system design and reducing time to market.

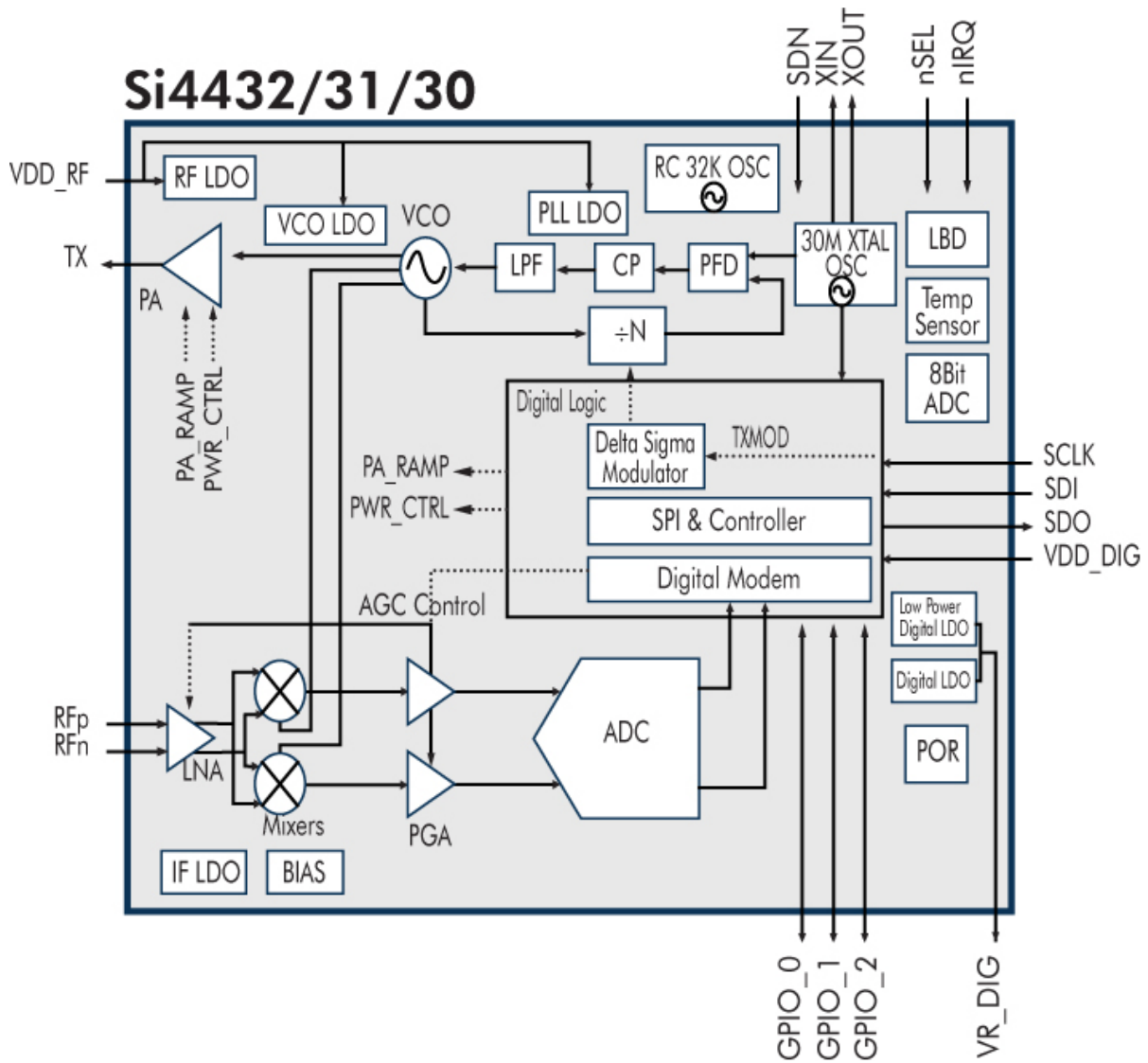


Patents pending



# Si4430/31/32-B1

## Functional Block Diagram



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**TABLE OF CONTENTS**


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<b><u>Section</u></b>	<b><u>Page</u></b>
<b>1. Electrical Specifications</b> .....	<b>7</b>
1.1. Definition of Test Conditions .....	14
<b>2. Functional Description</b> .....	<b>15</b>
2.1. Operating Modes .....	17
<b>3. Controller Interface</b> .....	<b>18</b>
3.1. Serial Peripheral Interface (SPI) .....	18
3.2. Operating Mode Control .....	20
3.3. Interrupts .....	23
3.4. System Timing .....	24
3.5. Frequency Control .....	25
<b>4. Modulation Options</b> .....	<b>32</b>
4.1. Modulation Type .....	32
4.2. Modulation Data Source .....	33
<b>5. Internal Functional Blocks</b> .....	<b>37</b>
5.1. RX LNA .....	37
5.2. RX I-Q Mixer .....	37
5.3. Programmable Gain Amplifier .....	37
5.4. ADC .....	37
5.5. Digital Modem .....	37
5.6. Synthesizer .....	38
5.7. Power Amplifier .....	39
5.8. Crystal Oscillator .....	40
5.9. Regulators .....	40
<b>6. Data Handling and Packet Handler</b> .....	<b>41</b>
6.1. RX and TX FIFOs .....	41
6.2. Packet Configuration .....	42
6.3. Packet Handler TX Mode .....	43
6.4. Packet Handler RX Mode .....	43
6.5. Data Whitening, Manchester Encoding, and CRC .....	46
6.6. Preamble Detector .....	46
6.7. Preamble Length .....	47
6.8. Invalid Preamble Detector .....	47
6.9. Synchronization Word Configuration .....	47
6.10. Receive Header Check .....	48
6.11. TX Retransmission and Auto TX .....	48
<b>7. RX Modem Configuration</b> .....	<b>49</b>
7.1. Modem Settings for FSK and GFSK .....	49
<b>8. Auxiliary Functions</b> .....	<b>50</b>
8.1. Smart Reset .....	50

# Si4430/31/32-B1

---

8.2. Microcontroller Clock	51
8.3. General Purpose ADC	52
8.4. Temperature Sensor	53
8.5. Low Battery Detector	55
8.6. Wake-Up Timer and 32 kHz Clock Source	56
8.7. Low Duty Cycle Mode	58
8.8. GPIO Configuration	59
8.9. Antenna Diversity	60
8.10. RSSI and Clear Channel Assessment	61
<b>9. Reference Design</b>	<b>62</b>
<b>10. Application Notes and Reference Designs</b>	<b>63</b>
<b>11. Customer Support</b>	<b>63</b>
<b>12. Register Table and Descriptions</b>	<b>64</b>
<b>13. Pin Descriptions: Si4430/31/32</b>	<b>66</b>
<b>14. Ordering Information</b>	<b>67</b>
<b>15. Package Markings (Top Marks)</b>	<b>68</b>
15.1. Si4430/31/32 Top Mark	68
15.2. Top Mark Explanation	68
<b>16. Package Outline: Si4430/31/32</b>	<b>69</b>
<b>17. PCB Land Pattern: Si4430/31/32</b>	<b>70</b>
<b>Document Change List</b>	<b>72</b>
<b>Contact Information</b>	<b>74</b>

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**LIST OF FIGURES**


---

Figure 1. Si4430/31 RX/TX Direct-Tie Application Example .....	16
Figure 2. Si4432 Antenna Diversity Application Example .....	16
Figure 3. SPI Timing.....	18
Figure 4. SPI Timing—READ Mode .....	19
Figure 5. SPI Timing—Burst Write Mode .....	19
Figure 6. SPI Timing—Burst Read Mode .....	19
Figure 7. State Machine Diagram.....	20
Figure 8. TX Timing.....	24
Figure 9. RX Timing .....	24
Figure 10. Frequency Deviation .....	28
Figure 11. Sensitivity at 1% PER vs. Carrier Frequency Offset .....	29
Figure 12. FSK vs GFSK Spectrums.....	32
Figure 13. Direct Synchronous Mode Example.....	35
Figure 14. Direct Asynchronous Mode Example.....	35
Figure 15. Microcontroller Connections.....	36
Figure 16. PLL Synthesizer Block Diagram.....	38
Figure 17. FIFO Thresholds .....	41
Figure 18. Packet Structure.....	42
Figure 19. Multiple Packets in TX Packet Handler .....	43
Figure 20. Required RX Packet Structure with Packet Handler Disabled .....	43
Figure 21. Multiple Packets in RX Packet Handler.....	43
Figure 22. Multiple Packets in RX with CRC or Header Error .....	44
Figure 23. Operation of Data Whitening, Manchester Encoding, and CRC .....	46
Figure 24. Manchester Coding Example .....	46
Figure 25. Header .....	48
Figure 26. POR Glitch Parameters.....	50
Figure 27. General Purpose ADC Architecture .....	52
Figure 28. Temperature Ranges using ADC8 .....	54
Figure 29. WUT Interrupt and WUT Operation.....	57
Figure 30. Low Duty Cycle Mode .....	58
Figure 31. RSSI Value vs. Input Power.....	61
Figure 32. TX/RX Direct-Tie Reference Design—Schematic.....	62
Figure 33. 20-Pin Quad Flat No-Lead (QFN) .....	69
Figure 34. PCB Land Pattern .....	70

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## LIST OF TABLES

---

Table 1. DC Characteristics <sup>1</sup> .....	7
Table 2. Synthesizer AC Electrical Characteristics <sup>1</sup> .....	8
Table 3. Receiver AC Electrical Characteristics <sup>1</sup> .....	9
Table 4. Transmitter AC Electrical Characteristics <sup>1</sup> .....	10
Table 5. Auxiliary Block Specifications <sup>1</sup> .....	11
Table 6. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ) .....	12
Table 7. GPIO Specifications (GPIO_0, GPIO_1, and GPIO_2) .....	12
Table 8. Absolute Maximum Ratings .....	13
Table 9. Operating Modes .....	17
Table 10. Serial Interface Timing Parameters .....	18
Table 11. Operating Modes Response Time .....	20
Table 12. Frequency Band Selection .....	26
Table 13. Packet Handler Registers .....	45
Table 14. Minimum Receiver Settling Time .....	47
Table 15. POR Parameters .....	50
Table 16. Temperature Sensor Range .....	53
Table 17. Antenna Diversity Control .....	60
Table 18. Register Descriptions .....	64
Table 19. Package Dimensions .....	69
Table 20. PCB Land Pattern Dimensions .....	71

## 1. Electrical Specifications

Table 1. DC Characteristics<sup>1</sup>

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	$V_{DD}$		1.8	3.0	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF <sup>2</sup>	—	15	50	nA
	$I_{Standby}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF	—	450	800	nA
	$I_{Sleep}$	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF	—	1	—	$\mu$ A
	$I_{Sensor-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF <sup>2</sup>	—	1	—	$\mu$ A
	$I_{Sensor-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF <sup>2</sup>	—	1	—	$\mu$ A
	$I_{Ready}$	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled	—	800	—	$\mu$ A
TUNE Mode Current	$I_{Tune}$	Synthesizer and regulators enabled	—	8.5	—	mA
RX Mode Current	$I_{RX}$		—	18.5	—	mA
TX Mode Current —Si4432	$I_{TX_{+20}}$	txpow[2:0] = 111 (+20 dBm) Using Silicon Labs' Reference Design. TX current consumption is dependent on match and board layout.	—	85	—	mA
TX Mode Current —Si4430/31	$I_{TX_{+13}}$	txpow[2:0] = 110 (+13 dBm) Using Silicon Labs' Reference Design. TX current consumption is dependent on match and board layout.	—	30	—	mA
	$I_{TX_{+1}}$	txpow[2:0] = 010 (+1 dBm) Using Silicon Labs' Reference Design. TX current consumption is dependent on match and board layout.	—	17	—	mA

**Notes:**

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.



**Table 2. Synthesizer AC Electrical Characteristics<sup>1</sup>**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range—Si4431/32	$F_{\text{SYN}}$		240	—	930	MHz
Synthesizer Frequency Range—Si4430	$F_{\text{SYN}}$		900	—	960	MHz
Synthesizer Frequency Resolution <sup>2</sup>	$F_{\text{RES-LB}}$	Low Band, 240–480 MHz	—	156.25	—	Hz
	$F_{\text{RES-HB}}$	High Band, 480–960 MHz	—	312.5	—	Hz
Reference Frequency Input Level <sup>2</sup>	$f_{\text{REF-LV}}$	When using external reference signal driving XOUT pin, instead of using crystal. Measured peak-to-peak ( $V_{\text{PP}}$ )	0.7	—	1.6	V
Synthesizer Settling Time <sup>2</sup>	$t_{\text{LOCK}}$	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	200	—	$\mu\text{s}$
Residual FM <sup>2</sup>	$\Delta F_{\text{RMS}}$	Integrated over $\pm 250$ kHz bandwidth (500 Hz lower bound of integration)	—	2	4	$\text{kHz}_{\text{RMS}}$
Phase Noise <sup>2</sup>	$L_{\phi}(f_M)$	$\Delta F = 10$ kHz	—	-80	—	$\text{dBc/Hz}$
		$\Delta F = 100$ kHz	—	-90	—	$\text{dBc/Hz}$
		$\Delta F = 1$ MHz	—	-115	—	$\text{dBc/Hz}$
		$\Delta F = 10$ MHz	—	-130	—	$\text{dBc/Hz}$

**Notes:**

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2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.

Table 3. Receiver AC Electrical Characteristics<sup>1</sup>

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range—Si4431/32	$F_{RX}$		240	—	930	MHz
RX Frequency Range—Si4430	$F_{RX}$		900	—	960	MHz
RX Sensitivity <sup>2</sup>	$P_{RX\_2}$	(BER < 0.1%) (2 kbps, GFSK, BT = 0.5, $\Delta f = \pm 5$ kHz) <sup>3</sup>	—	-121	—	dBm
	$P_{RX\_40}$	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, $\Delta f = \pm 20$ kHz) <sup>3</sup>	—	-108	—	dBm
	$P_{RX\_100}$	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, $\Delta f = \pm 50$ kHz) <sup>3</sup>	—	-104	—	dBm
	$P_{RX\_125}$	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, $\Delta f = \pm 62.5$ kHz)	—	-101	—	dBm
	$P_{RX\_OOK}$	(BER < 0.1%) (4.8 kbps, 350 kHz BW, OOK) <sup>3</sup>	—	-110	—	dBm
(BER < 0.1%) (40 kbps, 400 kHz BW, OOK) <sup>3</sup>		—	-102	—	dBm	
RX Channel Bandwidth <sup>3</sup>	BW		2.6	—	620	kHz
BER Variation vs Power Level <sup>3</sup>	$P_{RX\_RES}$	Up to +5 dBm Input Level	—	0	0.1	ppm
LNA Input Impedance <sup>3</sup> (Unmatched—measured differentially across RX input pins)	$R_{IN-RX}$	915 MHz	—	51–60j	—	$\Omega$
		868 MHz	—	54–63j	—	
		433 MHz	—	89–110j	—	
		315 MHz	—	107–137j	—	
RSSI Resolution	$RES_{RSSI}$		—	$\pm 0.5$	—	dB
$\pm 1$ -Ch Offset Selectivity <sup>3</sup>	$C/I_{1-CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer and desired modulated with 40 kbps $\Delta F = 20$ kHz GFSK with BT = 0.5, channel spacing = 150 kHz	—	-31	—	dB
$\pm 2$ -Ch Offset Selectivity <sup>3</sup>	$C/I_{2-CH}$		—	-35	—	dB
$\geq \pm 3$ -Ch Offset Selectivity <sup>3</sup>	$C/I_{3-CH}$		—	-40	—	dB
Blocking at 1 MHz Offset <sup>3</sup>	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps $\Delta F = 20$ kHz GFSK with BT = 0.5	—	-52	—	dB
Blocking at 4 MHz Offset <sup>3</sup>	$4M_{BLOCK}$		—	-56	—	dB
Blocking at 8 MHz Offset <sup>3</sup>	$8M_{BLOCK}$		—	-63	—	dB
Image Rejection <sup>3</sup>	$Im_{REJ}$	Rejection at the image frequency. IF=937 kHz	—	-30	—	dB
Spurious Emissions <sup>3</sup>	$P_{OB\_RX1}$	Measured at RX pins	—	—	-54	dBm

**Notes:**

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 14.
2. Receive sensitivity at multiples of 30 MHz may be degraded. If channels with a multiple of 30 MHz are required it is recommended to shift the crystal frequency. Contact Silicon Labs Applications Support for recommendations.
3. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.

# Si4430/31/32-B1

**Table 4. Transmitter AC Electrical Characteristics<sup>1</sup>**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range—Si4431/32	$F_{TX}$		240	—	930	MHz
TX Frequency Range—Si4430	$F_{TX}$		900	—	960	MHz
FSK Data Rate <sup>2</sup>	$DR_{FSK}$		0.123	—	256	kbps
OOK Data Rate <sup>2</sup>	$DR_{OOK}$		0.123	—	40	kbps
Modulation Deviation	$\Delta f_1$	860–960 MHz	$\pm 0.625$		$\pm 320$	kHz
	$\Delta f_2$	240–860 MHz	$\pm 0.625$		$\pm 160$	kHz
Modulation Deviation Resolution <sup>2</sup>	$\Delta f_{RES}$		—	0.625	—	kHz
Output Power Range—Si4432 <sup>3</sup>	$P_{TX}$		+1	—	+20	dBm
Output Power Range—Si4430/31 <sup>3</sup>	$P_{TX}$		–8	—	+13	dBm
TX RF Output Steps <sup>2</sup>	$\Delta P_{RF\_OUT}$	controlled by txpow[2:0]	—	3	—	dB
TX RF Output Level <sup>2</sup> Variation vs. Temperature	$\Delta P_{RF\_TEMP}$	–40 to +85 °C	—	2	—	dB
TX RF Output Level Variation vs. Frequency <sup>2</sup>	$\Delta P_{RF\_FREQ}$	Measured across any one frequency band	—	1	—	dB
Transmit Modulation Filtering <sup>2</sup>	B*T	Gaussian Filtering Bandwidth Time Product	—	0.5	—	
Spurious Emissions <sup>2</sup>	$P_{OB-TX1}$	$P_{OUT} = +13$ dBm, Frequencies <1 GHz	—	—	–54	dBm
	$P_{OB-TX2}$	1–12.75 GHz, excluding harmonics	—	—	–54	dBm
Harmonics <sup>2</sup>	$P_{2HARM}$	Using reference design TX matching network and filter with max output power. Harmonics reduce linearly with output power.	—	—	–42	dBm
	$P_{3HARM}$		—	—	–42	dBm

**Notes:**

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.
3. Output power is dependent on matching components, board layout, and is measured at the pin.

Table 5. Auxiliary Block Specifications<sup>1</sup>

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature Sensor Accuracy <sup>2</sup>	TS <sub>A</sub>	After calibrated via sensor offset register tvoffs[7:0]	—	0.5	—	°C
Temperature Sensor Sensitivity <sup>2</sup>	TS <sub>S</sub>		—	5	—	mV/°C
Low Battery Detector Resolution <sup>2</sup>	LBD <sub>RES</sub>		—	50	—	mV
Low Battery Detector Conversion Time <sup>2</sup>	LBD <sub>CT</sub>		—	250	—	μs
Microcontroller Clock Output Frequency	F <sub>MC</sub>	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768K	—	30M	Hz
General Purpose ADC Resolution <sup>2</sup>	ADC <sub>ENB</sub>		—	8	—	bit
General Purpose ADC Bit Resolution <sup>2</sup>	ADC <sub>RES</sub>		—	4	—	mV/bit
Temp Sensor & General Purpose ADC Conversion Time <sup>2</sup>	ADC <sub>CT</sub>		—	305	—	μs
30 MHz XTAL Start-Up time	t <sub>30M</sub>	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	600	—	μs
30 MHz XTAL Cap Resolution <sup>2</sup>	30M <sub>RES</sub>	See "5.8. Crystal Oscillator" on page 40 for total load capacitance calculation	—	97	—	fF
32 kHz XTAL Start-Up Time <sup>2</sup>	t <sub>32k</sub>		—	6	—	sec
32 kHz Accuracy using Internal RC Oscillator <sup>2</sup>	32KRC <sub>RES</sub>		—	1000	—	ppm
32 kHz RC Oscillator Start-Up	t <sub>32kRC</sub>		—	500	—	μs
POR Reset Time	t <sub>POR</sub>		—	16	—	ms
Software Reset Time <sup>2</sup>	t <sub>soft</sub>		—	250	—	μs

**Notes:**

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.

# Si4430/31/32-B1

**Table 6. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	$T_{RISE}$	$0.1 \times V_{DD}$ to $0.9 \times V_{DD}$ , $C_L = 5 \text{ pF}$	—	—	8	ns
Fall Time	$T_{FALL}$	$0.9 \times V_{DD}$ to $0.1 \times V_{DD}$ , $C_L = 5 \text{ pF}$	—	—	8	ns
Input Capacitance	$C_{IN}$		—	—	1	pF
Logic High Level Input Voltage	$V_{IH}$		$V_{DD} - 0.6$	—	—	V
Logic Low Level Input Voltage	$V_{IL}$		—	—	0.6	V
Input Current	$I_{IN}$	$0 < V_{IN} < V_{DD}$	-100	—	100	nA
Logic High Level Output Voltage	$V_{OH}$	$I_{OH} < 1 \text{ mA}$ source, $V_{DD} = 1.8 \text{ V}$	$V_{DD} - 0.6$	—	—	V
Logic Low Level Output Voltage	$V_{OL}$	$I_{OL} < 1 \text{ mA}$ sink, $V_{DD} = 1.8 \text{ V}$	—	—	0.6	V

**Note:** All specifications guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.

**Table 7. GPIO Specifications (GPIO\_0, GPIO\_1, and GPIO\_2)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	$T_{RISE}$	$0.1 \times V_{DD}$ to $0.9 \times V_{DD}$ , $C_L = 10 \text{ pF}$ , $DRV < 1:0 > = HH$	—	—	8	ns
Fall Time	$T_{FALL}$	$0.9 \times V_{DD}$ to $0.1 \times V_{DD}$ , $C_L = 10 \text{ pF}$ , $DRV < 1:0 > = HH$	—	—	8	ns
Input Capacitance	$C_{IN}$		—	—	1	pF
Logic High Level Input Voltage	$V_{IH}$		$V_{DD} - 0.6$	—	—	V
Logic Low Level Input Voltage	$V_{IL}$		—	—	0.6	V
Input Current	$I_{IN}$	$0 < V_{IN} < V_{DD}$	-100	—	100	nA
Input Current If Pullup is Activated	$I_{INP}$	$V_{IL} = 0 \text{ V}$	5	—	25	$\mu\text{A}$
Maximum Output Current	$I_{OmaxLL}$	$DRV < 1:0 > = LL$	0.1	0.5	0.8	mA
	$I_{OmaxLH}$	$DRV < 1:0 > = LH$	0.9	2.3	3.5	mA
	$I_{OmaxHL}$	$DRV < 1:0 > = HL$	1.5	3.1	4.8	mA
	$I_{OmaxHH}$	$DRV < 1:0 > = HH$	1.8	3.6	5.4	mA
Logic High Level Output Voltage	$V_{OH}$	$I_{OH} < I_{Omax}$ source, $V_{DD} = 1.8 \text{ V}$	$V_{DD} - 0.6$	—	—	V
Logic Low Level Output Voltage	$V_{OL}$	$I_{OL} < I_{Omax}$ sink, $V_{DD} = 1.8 \text{ V}$	—	—	0.6	V

**Note:** All specifications guaranteed by qualification. Qualification test conditions are listed in the "Production Test Conditions" section on page 14.



Table 8. Absolute Maximum Ratings

Parameter	Value	Unit
$V_{DD}$ to GND	-0.3, +3.6	V
Instantaneous $V_{RF-peak}$ to GND on TX Output Pin	-0.3, +8.0	V
Sustained $V_{RF-peak}$ to GND on TX Output Pin	-0.3, +6.5	V
Voltage on Digital Control Inputs	-0.3, $V_{DD} + 0.3$	V
Voltage on Analog Inputs	-0.3, $V_{DD} + 0.3$	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range $T_A$	-40 to +85	°C
Thermal Impedance $\theta_{JA}$	30	°C/W
Junction Temperature $T_J$	+125	°C
Storage Temperature Range $T_{STG}$	-55 to +125	°C
<p><b>Note:</b> Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX <math>V_{RF-peak}</math> on TX output pin. Caution: ESD sensitive device.</p>		

# Si4430/31/32-B1

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## 1.1. Definition of Test Conditions

### Production Test Conditions:

- $T_A = +25\text{ }^\circ\text{C}$
- $V_{DD} = +3.3\text{ VDC}$
- Sensitivity measured at 919 MHz
- TX output power measured at 915 MHz
- External reference signal (XOUT) =  $1.0\text{ V}_{PP}$  at 30 MHz, centered around 0.8 VDC
- Production test schematic (unless noted otherwise)
- All RF input and output levels referred to the pins of the Si4430/31/32 (not the RF module)

### Qualification Test Conditions:

- $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$
- $V_{DD} = +1.8\text{ to }+3.6\text{ VDC}$
- Using TX/RX Split Antenna reference design or production test schematic
- All RF input and output levels referred to the pins of the Si4430/31/32 (not the RF module)

## 2. Functional Description

The Si4430/31/32 are ISM wireless transceivers with continuous frequency tuning over their specified bands which encompasses from 240–960 MHz. The wide operating voltage range of 1.8–3.6 V and low current consumption makes the Si4430/31/32 an ideal solution for battery powered applications.

The Si4430/31/32 operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2-level FSK/GFSK/OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance  $\Delta\Sigma$  ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is then output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and  $\Delta\Sigma$  Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency and frequency deviation at any frequency between 240–960 MHz. The transmit FSK data is modulated directly into the  $\Delta\Sigma$  data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

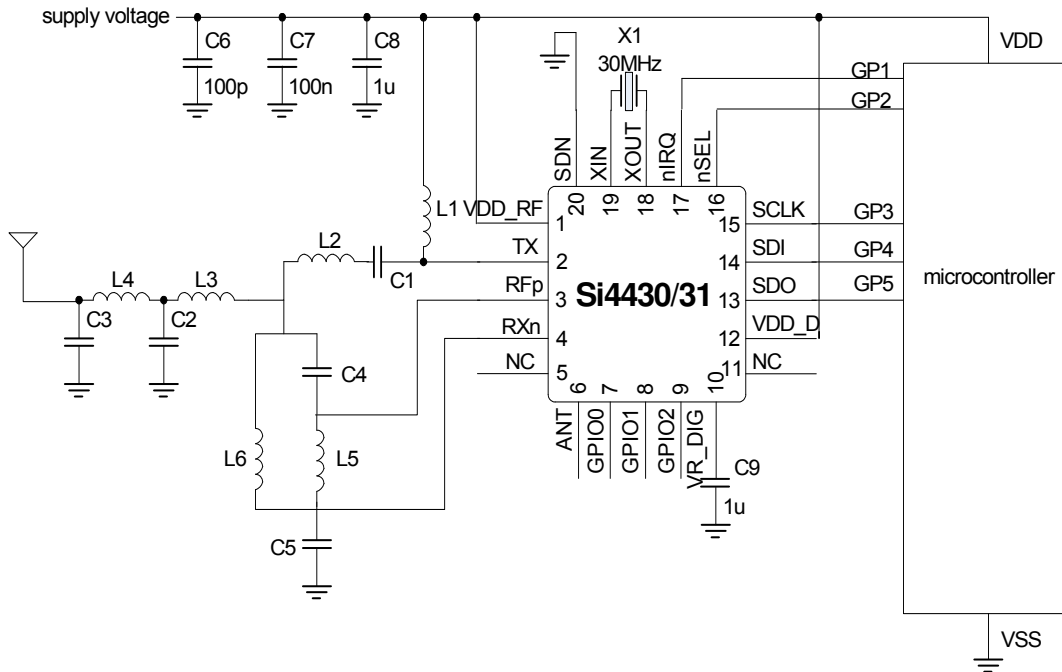
The Si4432's PA output power can be configured between +1 and +20 dBm in 3 dB steps, while the Si4430/31's PA output power can be configured between –8 and +13 dBm in 3 dB steps. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and rampdown control to reduce unwanted spectral spreading. The +20 dBm power amplifier of the Si4432 can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. Competing solutions require large and expensive external PAs to achieve comparable performance. The Si4430/31/32 supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance.

The Si4430/31/32 is designed to work with a microcontroller, crystal, and a few external components to create a very low cost system as shown Figure 1. Voltage regulators are integrated on-chip which allows for a wide operating supply voltage range from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with an external microcontroller. Three configurable general purpose I/Os are available. A complete list of the available GPIO functions is shown in "8. Auxiliary Functions" on page 50 and includes microcontroller clock output, Antenna Diversity, POR, and various interrupts.

The application shown in Figure 1 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most lower power applications will use this configuration. A complete direct-tie reference design is available from Silicon Laboratories applications support.

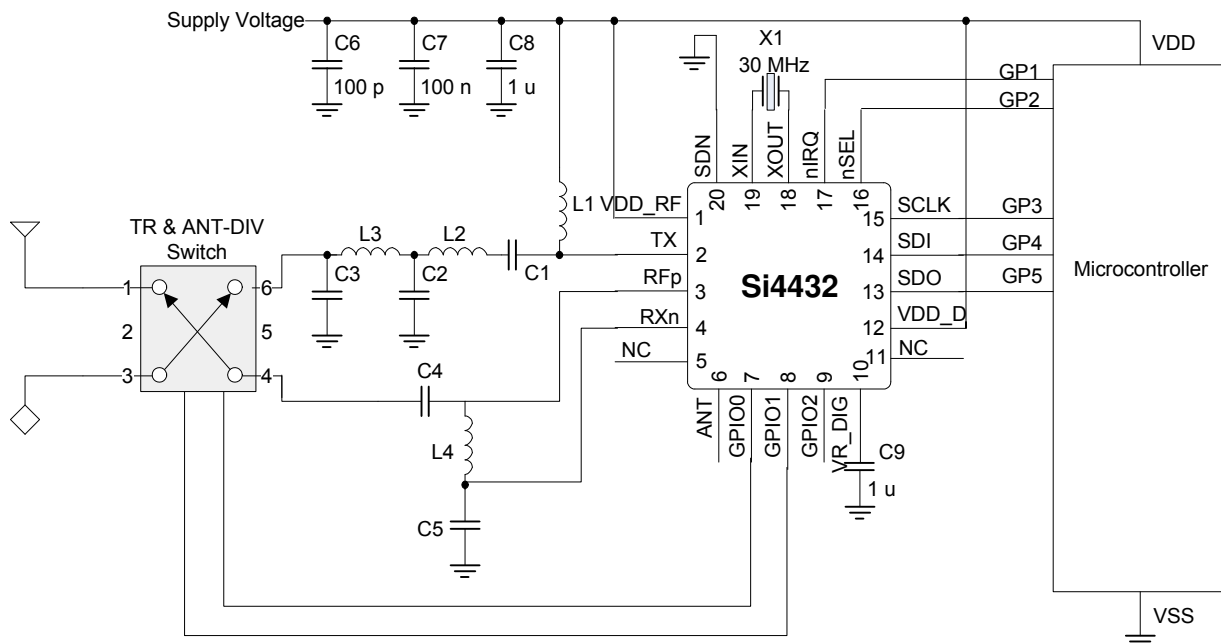
For applications seeking improved performance in the presence of multipath fading antenna diversity can be used. Antenna diversity support is integrated into the Si4430/31/32 and can improve the system link budget by 8–10 dB in the presence of these fading conditions, resulting in substantial range increases. A complete Antenna Diversity reference design is available from Silicon Laboratories applications support.

# Si4430/31/32-B1



Programmable load capacitors for X1 are integrated.  
L1-L6 and C1-C5 values depend on frequency band, antenna impedance, output power and supply voltage range.

**Figure 1. Si4430/31 RX/TX Direct-Tie Application Example**



Programmable load capacitors for X1 are integrated.  
L1-L4 and C1-C5 values depend on frequency band, antenna impedance, output power, and supply voltage range.

**Figure 2. Si4432 Antenna Diversity Application Example**

## 2.1. Operating Modes

The Si4430/31/32 provides several operating modes which can be used to optimize the power consumption for a given application. Depending upon the system communication protocol, an optimal trade-off between the radio wake time and power consumption can be achieved.

Table 9 summarizes the operating modes of the Si4430/31/32. In general, any given operating mode may be classified as an active mode or a power saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception of the SHUTDOWN mode, all can be dynamically selected by sending the appropriate commands over the SPI. An “X” in any cell means that, in the given mode of operation, that block can be independently programmed to be either ON or OFF, without noticeably impacting the current consumption. The SPI circuit block includes the SPI interface hardware and the device register space. The 32 kHz OSC block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor, general purpose ADC, and low-battery detector.

**Table 9. Operating Modes**

Mode Name	Circuit Blocks								I <sub>VDD</sub>
	Digital LDO	SPI	32 kHz OSC	AUX	30 MHz XTAL	PLL	PA	RX	
SHUT-DOWN	OFF (Register contents lost)	OFF	OFF	OFF	OFF	OFF	OFF	OFF	15 nA
STANDBY	ON (Register contents retained)	ON	OFF	OFF	OFF	OFF	OFF	OFF	450 nA
SLEEP		ON	ON	X	OFF	OFF	OFF	OFF	1 μA
SENSOR		ON	X	ON	OFF	OFF	OFF	OFF	1 μA
READY		ON	X	X	ON	OFF	OFF	OFF	800 μA
TUNING		ON	X	X	ON	ON	OFF	OFF	8.5 mA
TRANSMIT		ON	X	X	ON	ON	ON	OFF	30 mA*
RECEIVE		ON	X	X	ON	ON	OFF	ON	18.5 mA
<b>*Note:</b> Using Si4430/31 at +13 dBm using recommended reference design.									



## 3. Controller Interface

### 3.1. Serial Peripheral Interface (SPI)

The Si4430/31/32 communicates with the host MCU over a standard 3-wire SPI interface: SCLK, SDI, and nSEL. The host MCU can read data from the device on the SDO output pin. A SPI transaction is a 16-bit sequence which consists of a Read-Write ( $\overline{R/W}$ ) select bit, followed by a 7-bit address field (ADDR), and an 8-bit data field (DATA) as demonstrated in Figure 3. The 7-bit address field is used to select one of the 128, 8-bit control registers. The  $\overline{R/W}$  select bit determines whether the SPI transaction is a read or write transaction. If  $\overline{R/W} = 1$  it signifies a WRITE transaction, while  $\overline{R/W} = 0$  signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4430/31/32 every eight clock cycles. The timing parameters for the SPI interface are shown in Table 10. The SCLK rate is flexible with a maximum rate of 10 MHz.

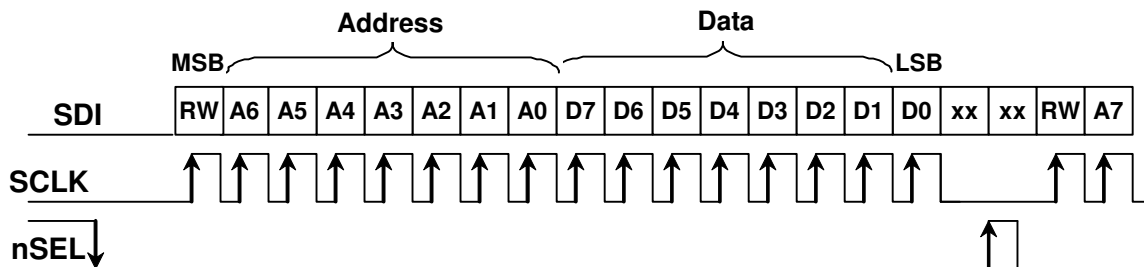


Figure 3. SPI Timing

Table 10. Serial Interface Timing Parameters

Symbol	Parameter	Min (nsec)	Diagram
$t_{CH}$	Clock high time	40	
$t_{CL}$	Clock low time	40	
$t_{DS}$	Data setup time	20	
$t_{DH}$	Data hold time	20	
$t_{DD}$	Output data delay time	20	
$t_{EN}$	Output enable time	20	
$t_{DE}$	Output disable time	50	
$t_{SS}$	Select setup time	20	
$t_{SH}$	Select hold time	50	
$t_{SW}$	Select high period	80	

To read back data from the Si4430/31/32, the R/W bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored on the SDI pin when  $R/W = 0$ . The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 4. After the READ function is completed the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pullup.

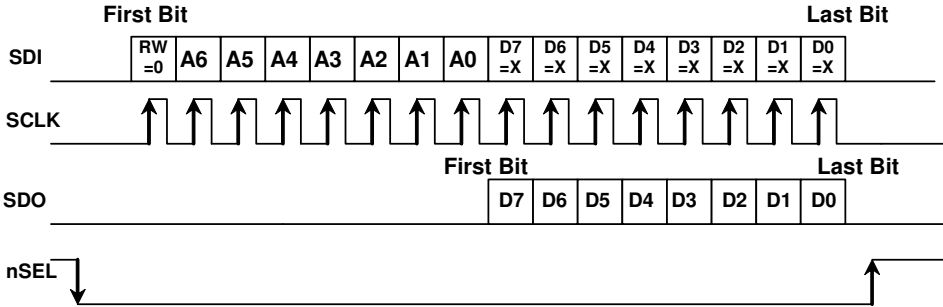


Figure 4. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode which allows for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An example burst write transaction is illustrated in Figure 5 and a burst read in Figure 6. As long as nSEL is held low, input data will be latched into the Si4430/31/32 every eight SCLK cycles.

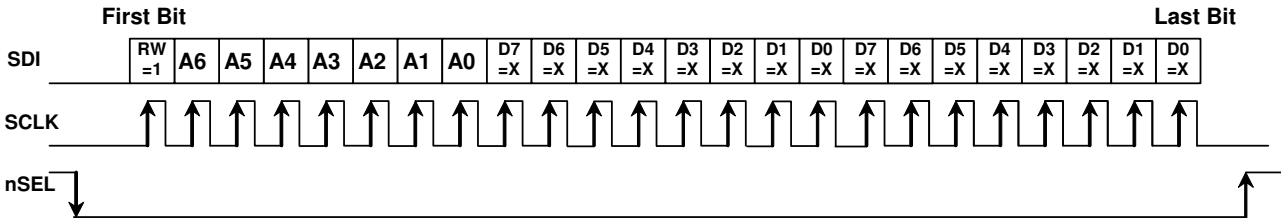


Figure 5. SPI Timing—Burst Write Mode

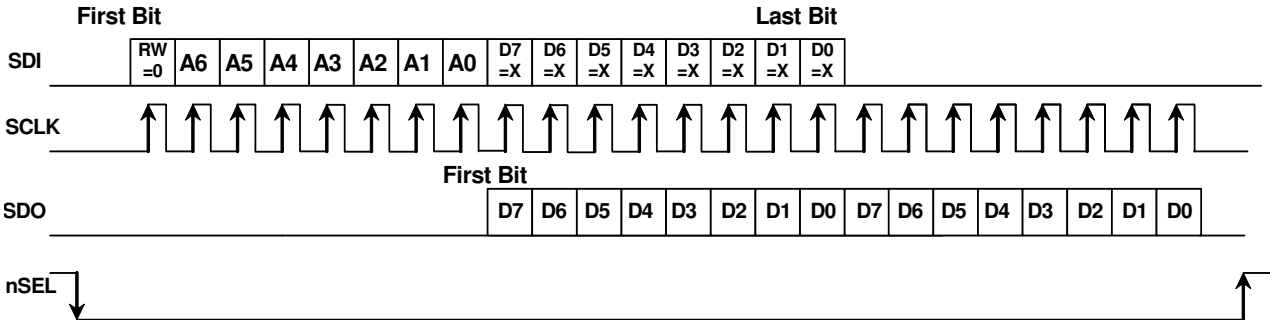
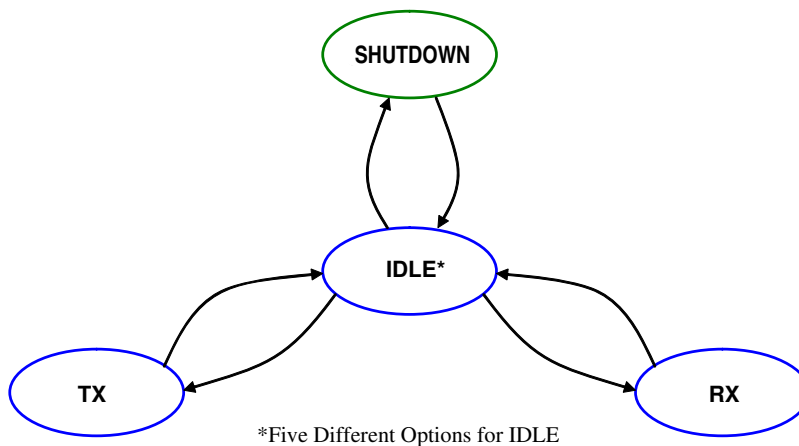


Figure 6. SPI Timing—Burst Read Mode

## 3.2. Operating Mode Control

There are four primary states in the Si4430/31/32 radio state machine: SHUTDOWN, IDLE, TX, and RX (see Figure 7). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. "Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected with the exception of SHUTDOWN which is controlled by SDN pin 20. The TX and RX state may be reached automatically from any of the IDLE states by setting the txon/rxon bits in "Register 07h. Operating Mode and Function Control 1". Table 11 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode.

The Si4430/31/32 includes a low-power digital regulated supply (LPLDO) which is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR\_DIG pin). This common digital supply voltage is connected to all digital circuit blocks including the digital modem, crystal oscillator, SPI, and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes. The main digital regulator is automatically enabled in all other modes.



**Figure 7. State Machine Diagram**

**Table 11. Operating Modes Response Time**

State/Mode	Response Time to		Current in State /Mode [ $\mu$ A]
	TX	RX	
Shut Down State	16.8 ms	16.8 ms	15 nA
Idle States:			
Standby Mode	800 $\mu$ s	800 $\mu$ s	450 nA
Sleep Mode	800 $\mu$ s	800 $\mu$ s	1 $\mu$ A
Sensor Mode	800 $\mu$ s	800 $\mu$ s	1 $\mu$ A
Ready Mode	200 $\mu$ s	200 $\mu$ s	800 $\mu$ A
Tune Mode	200 $\mu$ s	200 $\mu$ s	8.5 mA
TX State	NA	200 $\mu$ s	30 mA @ +13 dBm
RX State	200 $\mu$ s	NA	18.5 mA

## 3.2.1. SHUTDOWN State

The SHUTDOWN state is the lowest current consumption state of the device with nominally less than 15 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

## 3.2.2. IDLE State

There are five different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX/RX mode. This tradeoff is shown in Table 11. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

### 3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption of the five IDLE states with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The STANDBY mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

### 3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "8.6. Wake-Up Timer and 32 kHz Clock Source" on page 56 for more information on the Wake-Up-Timer. SLEEP mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

### 3.2.2.3. SENSOR Mode

In SENSOR mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 in "Register 07h. Operating Mode and Function Control 1". See "8.4. Temperature Sensor" on page 53 and "8.5. Low Battery Detector" on page 55 for more information on these features. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

### 3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time. READY mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled in "Register 62h. Crystal Oscillator Control and Test." To exit READY mode, bufovr (bit 1) of this register must be set back to 0.

### 3.2.2.5. TUNE Mode

In TUNE mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for frequency hopping spread spectrum systems (FHSS). TUNE mode is entered by setting pllcn = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

### 3.2.3. TX State

The TX state may be entered from any of the IDLE modes when the txon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The following sequence of events will occur automatically when going from STANDBY mode to TX mode by setting the txon bit.

1. Enable the main digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the skipvco bit is 1, default value is 0).
5. Wait until PLL settles to required transmit frequency (controlled by an internal timer).
6. Activate power amplifier and wait until power ramping is completed (controlled by an internal timer).
7. Transmit packet.

Steps in this sequence may be eliminated depending on which IDLE mode the chip is configured to prior to setting the txon bit. By default, the VCO and PLL are calibrated every time the PLL is enabled.

### 3.2.4. RX State

The RX state may be entered from any of the IDLE modes when the rxon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the main digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the skipvco bit is 1, default value is 0).
5. Wait until PLL settles to required receive frequency (controlled by an internal timer).
6. Enable receive circuits: LNA, mixers, and ADC.
7. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

### 3.2.5. Device Status

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
02	R	Device Status	ffovfl	ffunfl	rxffem	headerr	freqerr		cps[1]	cps[0]	—

The operational status of the chip can be read from "Register 02h. Device Status".



### 3.3. Interrupts

The Si4430/31/32 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h–04h) containing the active Interrupt Status bit. The nIRQ output signal will then be reset until the next change in status is detected. The interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h–06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs it will not trigger the nIRQ pin, but the status may still be read at anytime in the Interrupt Status registers.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
03	R	Interrupt Status 1	ifferr	itxffafull	itxffaem	irxffafull	iext	ipksent	ipkvalid	icrcerror	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	entxffafull	entxffaem	enrxffafull	enext	enpksent	enpvalid	enrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h

See “AN440: EZRadioPRO Detailed Register Descriptions” for a complete list of interrupts.

## 3.4. System Timing

The system timing for TX and RX modes is shown in Figures 8 and 9. The figures demonstrate transitioning from STANDBY mode to TX or RX mode through the built-in sequencer of required steps. The user only needs to program the desired mode, and the internal sequencer will properly transition the part from its current mode.

The VCO will automatically calibrate at every frequency change or power up. The PLL T0 time is to allow for bias settling of the VCO. The PLL TS time is for the settling time of the PLL, which has a default setting of 100  $\mu$ s. The total time for PLL T0, PLL CAL, and PLL TS under all conditions is 200  $\mu$ s. Under certain applications, the PLL T0 time and the PLL CAL may be skipped for faster turn-around time. Contact applications support if faster turnaround time is desired.

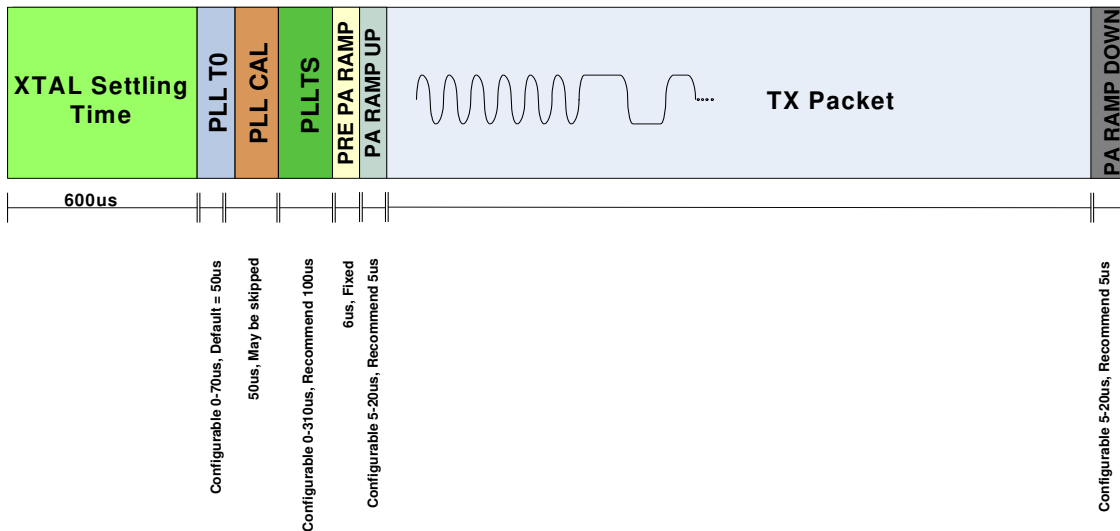


Figure 8. TX Timing

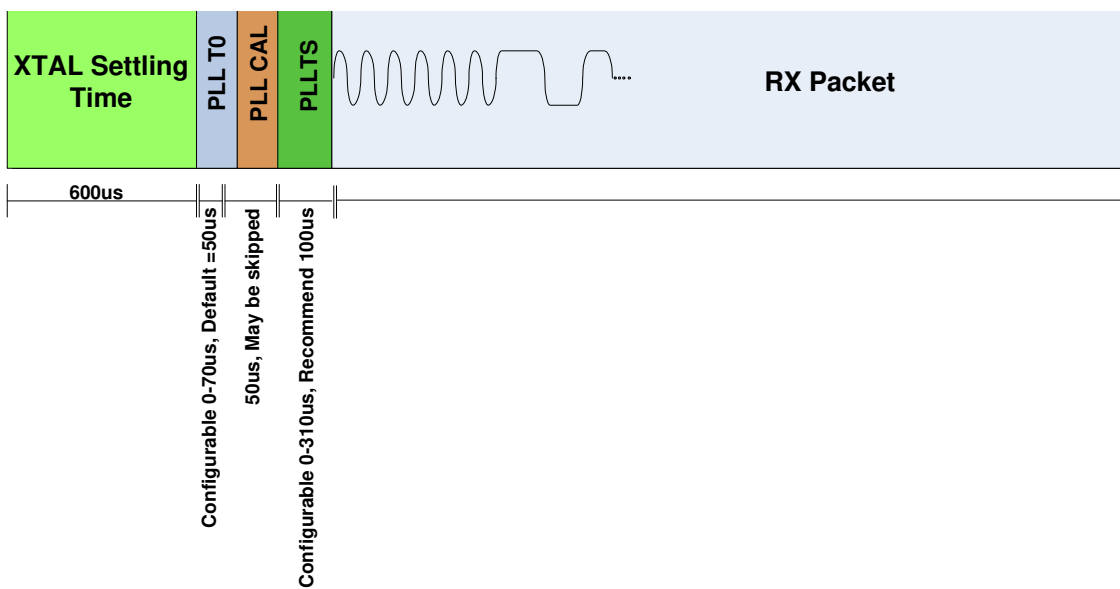


Figure 9. RX Timing

### 3.5. Frequency Control

For calculating the necessary frequency register settings it is recommended that customers use Silicon Labs' Wireless Design Suite (WDS) or the EZRadioPRO Register Calculator worksheet (in Microsoft Excel) available on the product website. These methods offer a simple method to quickly determine the correct settings based on the application requirements. The following information can be used to calculate these values manually.

#### 3.5.1. Frequency Programming

In order to receive or transmit an RF signal, the desired channel frequency,  $f_{carrier}$ , must be programmed into the Si4430/31/32. The Si4431/32 and Si4430 cover different frequencies. This section discusses the frequency range covered by all EZRadioPRO devices. Note that this frequency is the center frequency of the desired channel and not an LO frequency. The carrier frequency is generated by a Fractional-N Synthesizer, using 10 MHz both as the reference frequency and the clock of the (3<sup>rd</sup> order)  $\Delta\Sigma$  modulator. This modulator uses modulo 64000 accumulators. This design was made to obtain the desired frequency resolution of the synthesizer. The overall division ratio of the feedback loop consist of an integer part (N) and a fractional part (F). In a generic sense, the output frequency of the synthesizer is as follows:

$$f_{OUT} = 10MHz \times (N + F)$$

The fractional part (F) is determined by three different values, Carrier Frequency (fc[15:0]), Frequency Offset (fo[8:0]), and Frequency Deviation (fd[7:0]). Due to the fine resolution and high loop bandwidth of the synthesizer, FSK modulation is applied inside the loop and is done by varying F according to the incoming data; this is discussed further in "3.5.4. Frequency Deviation" on page 27. Also, a fixed offset can be added to fine-tune the carrier frequency and counteract crystal tolerance errors. For simplicity assume that only the fc[15:0] register will determine the fractional component. The equation for selection of the carrier frequency is shown below:

$$f_{carrier} = 10MHz \times (hbssel + 1) \times (N + F)$$

$$f_{TX} = 10MHz * (hbssel + 1) * (fb[4:0] + 24 + \frac{fc[15:0]}{64000})$$

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2							fo[9]	fo[8]	00h
75	R/W	Frequency Band Select		sbsel	hbssel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h

The integer part (N) is determined by fb[4:0]. Additionally, the output frequency can be halved by connecting a ÷2 divider to the output. This divider is not inside the loop and is controlled by the hbssel bit in "Register 75h. Frequency Band Select." This effectively partitions the entire 240–960 MHz frequency range into two separate bands: High Band (HB) for hbssel = 1, and Low Band (LB) for hbssel = 0. The valid range of fb[4:0] is from 0 to 23. If a higher value is written into the register, it will default to a value of 23. The integer part has a fixed offset of 24 added to it as shown in the formula above. Table 12 demonstrates the selection of fb[4:0] for the corresponding frequency band.

After selection of the fb (N) the fractional component may be solved with the following equation:

$$fc[15:0] = \left( \frac{f_{TX}}{10MHz * (hbssel + 1)} - fb[4:0] - 24 \right) * 64000$$

fb and fc are the actual numbers stored in the corresponding registers.