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Easy-to-Use, Low-Current OOK/(G)FSK Sub-GHz Transceiver

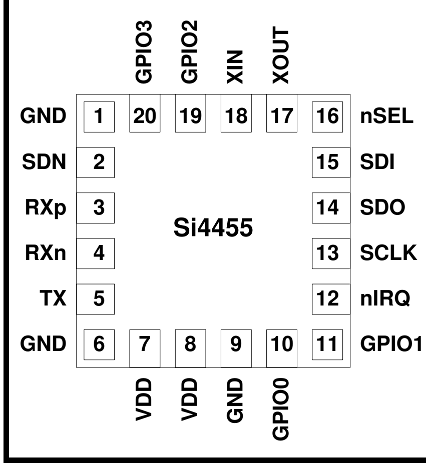
Features

- Frequency range = 283–960 MHz
- Receive sensitivity = –116 dBm
- Modulation
  - (G)FSK
  - OOK
- Max output power = +13 dBm
- Low active power consumption
  - 10 mA RX
  - 18 mA TX @ +10 dBm
- Low standby current = 50 nA
- Max data rate = 500 kbps
- Power supply = 1.8 to 3.6 V
- TX and RX 64 byte FIFOs
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Integrated battery voltage sensor
- Packet handling including preamble, sync word detection, and CRC
- Low BOM
- 20-Pin 3x3 mm QFN package

Applications

- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors

Pin Assignments



Patents pending

Description

Silicon Laboratories' Si4455 is an easy-to-use, low current, sub-GHz EZRadio® transceiver. Covering all major bands, it combines plug-and-play simplicity with the flexibility needed to handle a wide variety of applications. The compact 3x3 mm package size combined with a low external BOM count makes the Si4455 both space efficient and cost effective. The +13 dBm output power and excellent sensitivity of –116 dBm allows for a longer operating range, while the low current consumption of 18 mA TX (at 10 dBm), 10 mA RX, and 50 nA standby, provides for superior battery life. By fully integrating all components from the antenna to the GPIO or SPI interface to the MCU, the Si4455 makes realizing this performance in an application easy. Design simplicity is further exemplified in the Wireless Development Suite (WDS) user interface module. This configuration module provides simplified programming options for a broad range of applications in an easy to use format that results in both a faster and lower risk development. The Si4455 is capable of supporting major worldwide regulatory standards such as FCC, ETSI, ARIB and China regulatory standards.

Functional Block Diagram

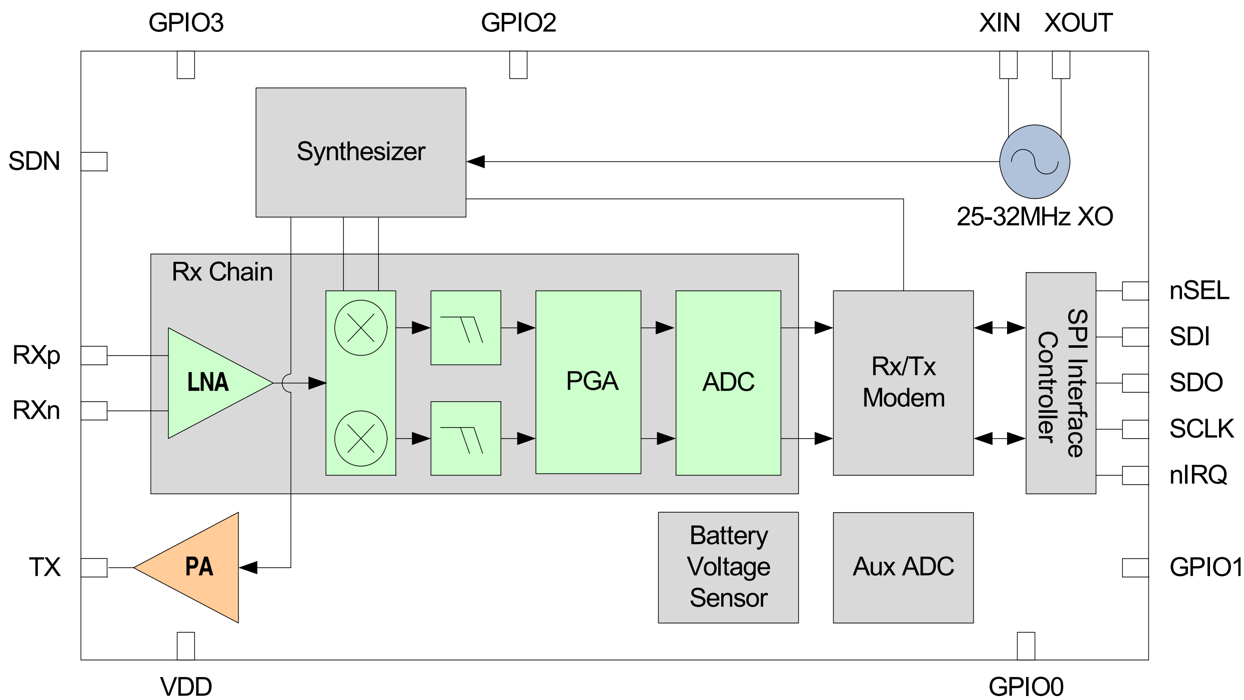


Table of Contents

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Supply Voltage	V_{DD}		1.8		3.6	V
I/O Drive Voltage	V_{GPIO}		1.8		3.6	V

Table 2. DC Characteristics*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.8	3.3	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC oscillator, main digital regulator, and low power digital regulator OFF.	—	30	—	nA
	$I_{Standby}$	Register values maintained.	—	50	—	nA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF.	—	2	—	mA
	ISPI Active	SPI active state		1.35		mA
TUNE Mode Current	I_{Tune_RX}	RX Tune	—	6.5	—	mA
	I_{Tune_TX}	TX Tune	—	6.9	—	mA
RX Mode Current	I_{RX}		—	10	—	mA
TX Mode Current	I_{TX}	+10 dBm output power, 868 MHz	—	18	—	mA
		+13 dBm output power, 868 MHz	—	30	—	mA

***Note:** All specifications are guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in section "1.1. Definition of Test Conditions" on page 11.

Table 3. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		283	—	350	MHz
			425	—	525	MHz
			850	—	960	MHz
Synthesizer Frequency Resolution[2]	$F_{RES-960}$	850–960 MHz	—	114.4	—	Hz
	$F_{RES-525}$	425–525 MHz	—	57.2	—	Hz
	$F_{RES-350}$	283–350 MHz	—	38.1	—	Hz

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in section "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in section "1.1. Definition of Test Conditions" on page 11.

Table 4. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		283	—	350	MHz
			425	—	525	MHz
			850	—	960	MHz
RX Sensitivity	P_{RX-_2}	(BER < 0.1%) (2.4 kbps, GFSK, BT = 0.5, ΔF = ±30 kHz, 114 kHz Rx BW)[2]	—	–116	—	dBm
	P_{RX-_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, ΔF = ±25 kHz, 114 kHz Rx BW)[2]	—	–108	—	dBm
	P_{RX-_128}	(BER < 0.1%) (128 kbps, GFSK, BT = 0.5, ΔF = ±70 kHz, 305 kHz Rx BW)[2]	—	–103	—	dBm
	P_{RX-_OOK}	(BER < 0.1%, 1 kbps, 185 kHz Rx BW, OOK, PN15 data)[2]	—	–113	—	dBm
		(BER < 0.1%, 40 kbps, 185 kHz Rx BW, OOK, PN15 data)[2]	—	–102	—	dBm
RX Channel Bandwidth[2]	BW		40	—	850	kHz
BER Variation vs Power Level[2]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[2]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW and desired modulated with 1.2 kbps, ΔF = 5.2 kHz, GFSK with BT= 0.5, RX BW = 58 kHz channel spacing = 100 kHz	—	–56	—	dB
±2-Ch Offset Selectivity[2]	$C/I_{2\text{-}CH}$		—	–59	—	dB
Blocking 200 kHz–1 MHz	$200K_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW and desired modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, RX BW = 58 kHz	—	–58	—	dB
Blocking 1 MHz Offset[2]	$1M_{BLOCK}$		—	–61	—	dB
Blocking 8 MHz Offset[2]	$8M_{BLOCK}$		—	–79	—	dB
Image Rejection[2]	Im_{REJ}	Rejection at the image frequency IF = 468 kHz	—	–35	—	dB
Spurious Emissions[3]	P_{OB_RX1}	Measured at RX pins	—	–54	—	dBm

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in section "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in section "1.1. Definition of Test Conditions" on page 11.
3. Emissions specifications are based on frequency, matching components, and board layout.

Table 5. Transmitter AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		283	—	350	MHz
			425	—	525	MHz
			850	—	960	MHz
(G)FSK Data Rate[2]	DR_{FSK}		1.0	—	500	kbps
OOK Data Rate[2]	DR_{OOK}		0.5	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–960 MHz	—	—	500	kHz
	Δf_{525}	425–525 MHz	—	—	500	kHz
	Δf_{350}	283–350 MHz	—	—	500	kHz
Modulation Deviation Resolution[2]	$F_{RES\text{-}960}$	850–1050 MHz	—	114.4	—	Hz
	$F_{RES\text{-}525}$	425–525 MHz	—	57.2	—	Hz
	$F_{RES\text{-}350}$	283–350 MHz	—	38.1	—	Hz
Output Power Range[3]	P_{TX}		–40	—	+13	dBm
TX RF Output Steps[2]	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.1	—	dB
TX RF Output Level[2] Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	1	—	dB
TX RF Output Level Variation vs. Frequency[2]	ΔP_{RF_FREQ}	Measured across 902–928 MHz	—	0.5	—	dB
Transmit Modulation Filtering[2]	B*T	Gaussian Filtering Bandwith Time Product	—	0.5	—	
Spurious Emissions[3]	$P_{OB\text{-}TX1}$	P_{OUT} = +13 dBm, Frequencies < 1 GHz	—	–54	—	dBm
	$P_{OB\text{-}TX2}$	1–12.75 GHz, excluding harmonics	—	–42	—	dBm
Harmonics[3]	P_{2HARM}	Using reference design TX matching network and filter with max output power. Harmonics reduce linearly with output power.	—	–42	—	dBm
	P_{3HARM}		—	–42	—	dBm

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
3. Output power and emissions specifications are dependent on transmit frequency, matching components, and board layout.

Table 6. Auxiliary Block Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XTAL Range[2]	$XTAL_{RANGE}$		25	—	32	MHz
30 MHz XTAL Start-Up time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	250	—	µs
30 MHz XTAL Cap Resolution[3]	$30M_{RES}$		—	70	—	fF
POR Reset Time	t_{POR}		—	—	5	ms

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. XTAL Range tested in production using an external clock source (similar to using a TCXO).
3. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.

Table 7. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 10 pF, DRV<1:0> = LL V_{DD} = 3.3 V	—	2.3	—	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x $V_{DD,}$ C_L= 10 pF, DRV<1:0> = LL V_{DD} = 3.3 V	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	$0 < V_{IN} < V_{DD}$	–10	—	10	µA
Input Current if Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	10	µA
Drive Strength for Output Low Level[2]	I_{OmaxLL}	DRV[1:0] = LL	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	1.13	—	mA
Drive Strength for Output High Level (GPIO1, GPIO2, GPIO3)[2]	I_{OmaxLL}	DRV[1:0] = LL	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	0.96	—	mA
Drive Strength for Output High Level (GPIO0)[2]	I_{OmaxLL}	DRV[1:0] = LL	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	1.7	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD} x 0.2	V

Notes:

1. All specifications guaranteed by qualification. Qualification test conditions are listed under “Qualification Test Conditions” in "1.1. Definition of Test Conditions" on page 11.
2. GPIO output current measured at 3.3 VDC VDD with V_{OH} = 2.64 VDC and V_{OL} = 0.66 VDC.

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Max Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	30	°C/W
Junction Temperature	T_J		92	°C

Table 9. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.

1.1. Definition of Test Conditions

Production Test Conditions:

- T_A = +25 °C
- V_{DD} = +3.3 VDC
- Sensitivity measured at 434 MHz using a PN15 modulated input signal and with packet handler mode enabled.
- External reference signal (XIN) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC
- RF input and output levels can typically be achieved at the antenna port after filtering components.

Qualification Test Conditions:

- T_A = –40 to +85 °C (typical = 25 °C)
- V_{DD} = +1.8 to +3.6 VDC (typical = 3.3 VDC)
- Use TX/RX Split Antenna reference design or production test schematic
- RF input and output levels can typically be achieved at the antenna port after filtering components.

2. Typical Applications Schematic

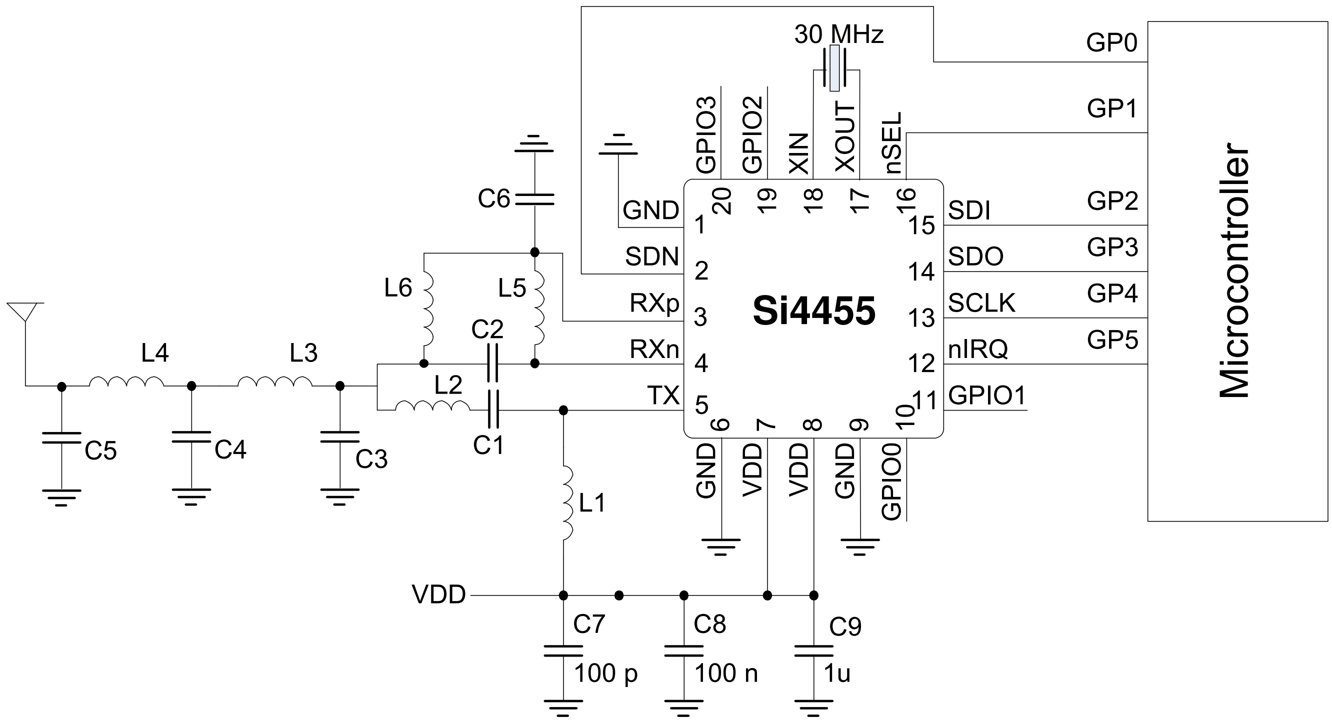


Figure 1. Si4455 Application Circuit

3. Functional Description

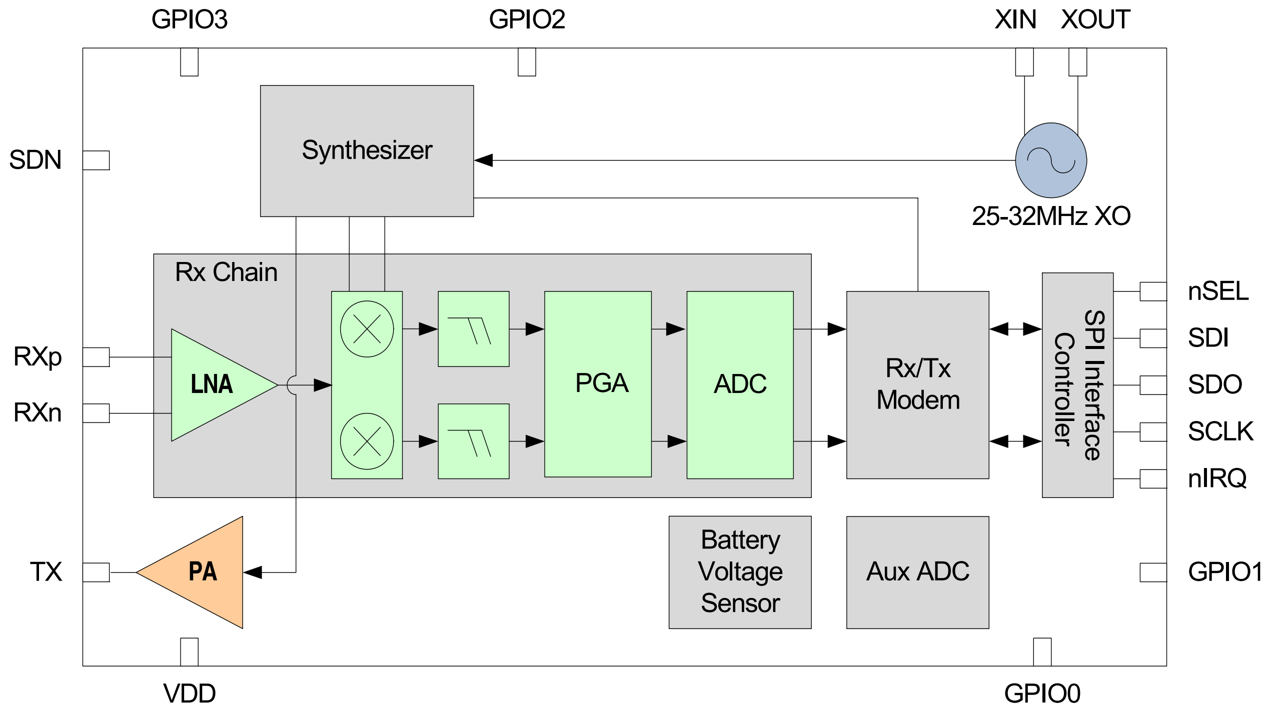


Figure 2. Si4455 Functional Block Diagram

The Si4455 is an easy-to-use, size efficient, low current wireless ISM transceiver that covers the sub-GHz bands. The wide operating voltage range of 1.8–3.6 V and low current consumption make the Si4455 an ideal solution for battery powered applications. The Si4455 operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the FSK/GFSK or OOK/ASK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA), the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in digital modem, increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte Rx FIFO.

A single high-precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO signal is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates up to 500 kbps. The Si4455 operates in the frequency bands of 283–350, 425–525, and 850–960 MHz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The Si4455 contains a power amplifier (PA) that supports output powers up to +13 dBm and is designed to support single coin cell operation with current consumption of 18 mA for +10 dBm output power. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. Additional system features, such as 64-byte TX/RX FIFOs, preamble detection, sync word detector, and CRC, reduce overall current consumption and allow for the use of lower-cost system MCUs. Power-on-reset (POR) and GPIOs further reduce overall system cost and size. The Si4455 is designed to work with an MCU, crystal, and a few passives to create a very compact and low-cost system.

3.1. Receiver Chain

The internal low-noise amplifier (LNA) is designed to be a wideband LNA that can be matched with three external discrete components to cover any common range of frequencies in the sub-GHz band. The LNA has extremely low noise to suppress the noise of the following stages and achieve optimal sensitivity; therefore, no external gain or front-end modules are necessary. The LNA has gain control, which is controlled by the internal automatic gain control (AGC) algorithm. The LNA is followed by an I-Q mixer, filter, programmable gain amplifier (PGA), and ADC. The I-Q mixers downconvert the signal to an intermediate frequency. The PGA then boosts the gain to be within dynamic range of the ADC. The ADC rejects out-of-band blockers and converts the signal to the digital domain where filtering, demodulation, and processing is performed. Peak detectors are integrated at the output of the LNA and PGA for use in the AGC algorithm.

The RX and TX pins can be directly tied externally.

3.2. Receiver Modem

Using high-performance ADCs allows channel filtering, image rejection, and demodulation to be performed in the digital domain, which allows for flexibility in optimizing the device for particular applications. The digital modem performs the following functions:

- Channel selection filter
- Preamble detection
- Invalid preamble detection
- TX modulation
- RX demodulation
- Automatic Gain Control (AGC)
- Automatic frequency compensation (AFC)
- Radio signal strength indicator (RSSI)
- Cyclic redundancy check (CRC)

The digital channel filter and demodulator are optimized for ultra-low-power consumption and are highly configurable. Supported modulation types are GFSK, FSK, and OOK. The channel filter can be configured to support bandwidths ranging from 850 kHz down to 40 kHz. A large variety of data rates are supported ranging from 0.5 kbps up to 500 kbps. The configurable preamble detector is used with the synchronous demodulator to improve the reliability of the sync-word detection. Preamble detection can be skipped using only sync detection, which is a valuable feature of the asynchronous demodulator when very short preambles are used. The received signal strength indicator (RSSI) provides a measure of the signal strength received on the tuned channel. The resolution of the RSSI is 0.5 dB. This high-resolution RSSI enables accurate channel power measurements for clear channel assessment (CCA), carrier sense (CS), and listen before talk (LBT) functionality. A wireless communication channel can be corrupted by noise and interference, so it is important to know if the received data is free of errors. A cyclic redundancy check (CRC) is used to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the end of each transmitted packet and verified by the receiver to confirm that no errors have occurred. The packet handler and CRC can significantly reduce the load on the system microcontroller, allowing for a simpler and cheaper microcontroller. The digital modem includes the TX modulator, which converts the TX data bits into the corresponding stream of digital modulation values to be summed with the fractional input to the sigma-delta modulator. This modulation approach results in highly accurate resolution of the frequency deviation. A Gaussian filter is implemented to support GFSK, considerably reducing the energy in adjacent channels. The default bandwidth-time (BT) product is 0.5 for all programmed data rates.

3.2.1. Received Signal Strength Indicator

The received signal strength indicator (RSSI) is an estimate of the signal strength in the channel to which the receiver is tuned. The RSSI measurement is done after the channel filter, so it is only a measurement of the desired or undesired in-band signal power. The Si4455 uses a fast response register to read RSSI and so can complete the read in 16 SPI clock cycles with no requirement to wait for CTS. The RSSI value reported by this API command can be converted to dBm using the following equation:

$$RSSI_{dBm} = \frac{RSSI\_value}{2} - 130$$

The value of 130 in the above formula is based on bench characterization of the EZRadio RF Pico boards (evaluation boards). The RSSI value is latched at sync word detection and can be read via the fast response register. The latched value of RSSI is available until the device re-enters Rx mode. In addition, the current value of RSSI can be read out using the GET_MODEM_STATUS command. This can be used to implement CCA (clear channel assessment) functionality. The user can set up an RSSI threshold value using the WDS Radio Configuration Application GUI.

3.3. Synthesizer

The Si4455 includes an integrated Sigma Delta ($\Sigma\Delta$) Fractional-N PLL synthesizer capable of operating over the bands from 283–350, 425–525, and 850–960 MHz. The synthesizer has many advantages; it provides flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider, which results in very precise accuracy and control over the transmit deviation. The frequency resolution is (2/3)Freq_xo/(2^{19}) for 283–350 MHz, Freq_xo/(2^{19}) for 425–525 MHz, and Freq_xo/(2^{18}) for 850–960 MHz. The nominal reference frequency to the PLL is 30 MHz, but any XTAL frequency from 25 to 32 MHz may be used. The modem configuration calculator in WDS will automatically account for the XTAL frequency being used. The PLL utilizes a differential LC VCO with integrated on-chip inductors. The output of the VCO is followed by a configurable divider, which will divide the signal down to the desired output frequency band.

3.3.1. Synthesizer Frequency Control

The frequency is set by changing the integer and fractional settings to the synthesizer. The WDS calculator will automatically provide these settings, but the synthesizer equation is shown below for convenience. Initial frequency settings are configured in the EZConfig setup and can also be modified using the API commands: FREQ_CONTROL_INTE, FREQ_CONTROL_FRAC2, FREQ_CONTROL_FRAC1, and FREQ_CONTROL_FRAC0.

$$RF\ frequency = \left(fc\_inte + \frac{fc\_frac}{2^{19}}\right) \times \frac{4 \times freq\_xo}{outdiv}(Hz)$$

Note: The fc_frac/2^{19} value in the above formula must be a number between 1 and 2. The LSB of fc_frac must be "1".

Table 10. Output Divider (Outdiv) Values

Outdiv	Lower (MHz)	Upper (MHz)
12	284	350
8	425	525
4	850	960

3.3.1.1. EZ Frequency Programming

EZ frequency programming allows for easily changing radio frequency using a single API command. The base frequency is first set using the EZConfig setup. This base frequency will correspond to channel 0. Next, a channel step size is also programmed within the EZConfig setup. The resulting frequency will be:

$$RF\ Frequency = Base\ Frequency + Channel \times Step\ Size$$

The second argument of the START_RX or START_TX is CHANNEL, which sets the channel number for EZ frequency programming. For example, if the channel step size is set to 1 MHz, the base frequency is set to 900 MHz, and a CHANNEL number of 5 is programmed during the START_TX command, the resulting frequency will be 905 MHz. If no CHANNEL argument is written as part of the START_RX/TX command, it will default to the previous value. The initial value of CHANNEL is 0 and so will be set to the base frequency if this argument is never used.

3.4. Transmitter

The Si4455 contains a +13 dBm power amplifier that is capable of transmitting from –40 to +13 dBm. The output power set size is dependent on the power level and can be seen in Figure 3. The PA power level is set using the API command: PA_PWR_LVL. The power amplifier is single-ended to allow for easy antenna matching and low BOM cost. For detailed matching values, BOM, and performance expectations, refer to "AN686: Antennas for the Si4455/4355 RF ICs". Power ramp-up and ramp-down is automatically performed to reduce unwanted spectral spreading.

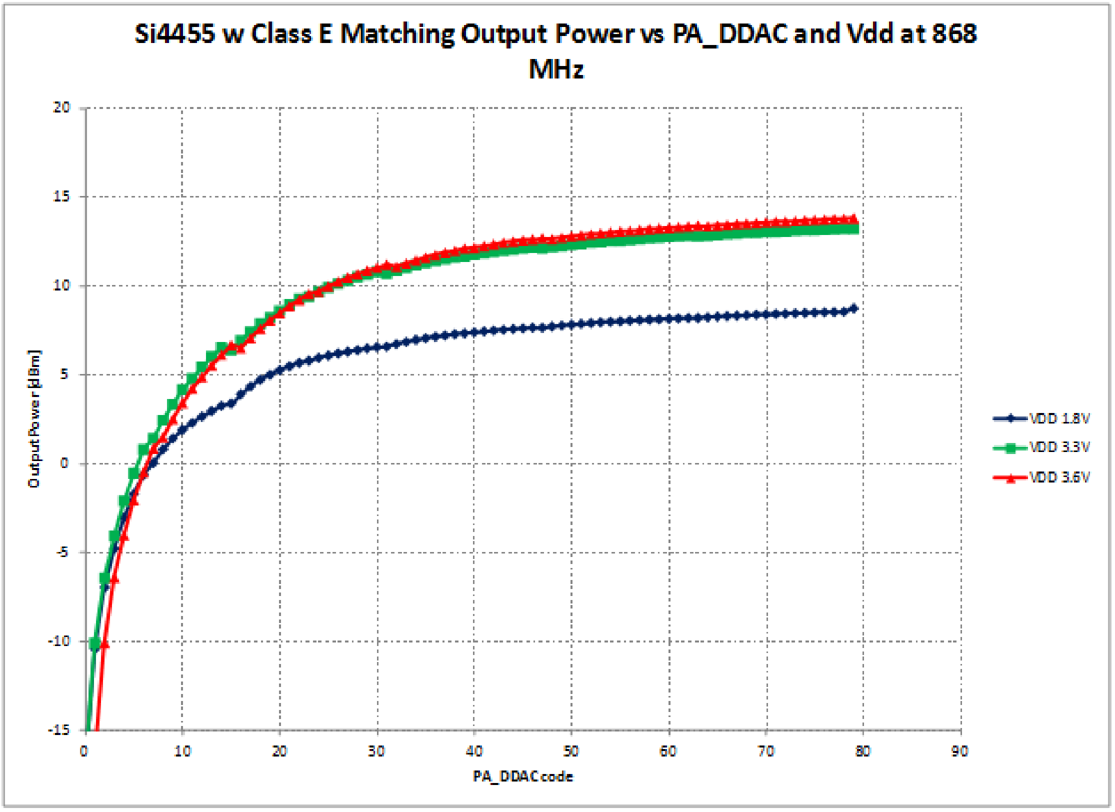


Figure 3. Tx Power vs PA_PWR_LVL and VDD

3.5. Crystal Oscillator

The Si4455 includes an integrated crystal oscillator with a fast start-up time of less than 250 µs. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the crystal. The default crystal is 30 MHz, but the circuit is designed to handle any XTAL from 25 to 32 MHz, set in the EZConfig setup. The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance and to adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the GLOBAL_XO_TUNE API property. The total internal capacitance is 11 pF and is adjustable in 127 steps (70 fF/step). The crystal frequency adjustment can be used to compensate for crystal production tolerances. The frequency offset characteristics of the capacitor bank are demonstrated in Figure 4.

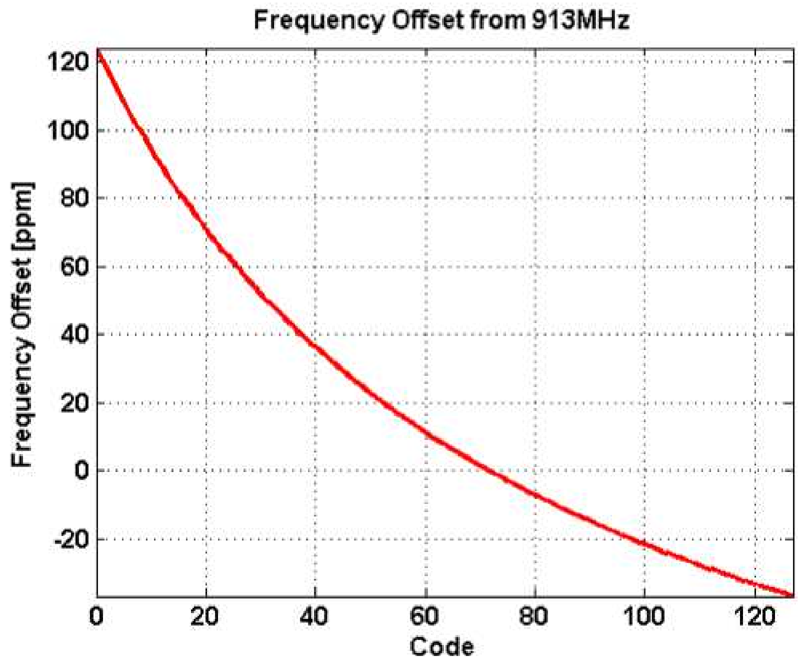


Figure 4. Capacitor Bank Frequency Offset Characteristics

An external signal source can easily be used in lieu of a conventional XTAL and should be connected to the XIN pin. The incoming clock signal is recommended to be ac-coupled to the XIN pin since the dc bias is controlled by the internal crystal oscillator buffering circuitry. The input swing range should be between 600 mV–1.8 V peak-to-peak. If external drive is desired, the incoming signal amplitude should not go below 0 V or exceed 1.8 V. The best dc bias should be approximately 0.7 V. However, if the signal swing exceeds 1.4 Vpp, the dc bias can be set to 1/2 the peak-to-peak voltage swing. The XO capacitor bank should be set to 0 whenever an external drive is used on the XIN pin. In addition, the POWER_UP command should be invoked with the TCXO option whenever external drive is used.

3.6. Battery Voltage and Auxiliary ADC

The Si4455 contains an integrated auxiliary 11-bit ADC used for the internal battery voltage detector or an external component via GPIO. The Effective Number of Bits (ENOB) is 9 bits. When measuring external components, the input voltage range is 1 V, and the conversion rate is between 300 Hz to 2.44 kHz. The ADC value is read by first sending the GET_ADC_READING command and enabling the desired inputs. When the conversion is finished and all the data is ready, CTS will go high, and the data can be read out. For details on this command and the formulas needed to interpret the results, refer to the EZRadio API documentation zip file available from www.silabs.com.

4. Configuration Options and User Interface

4.1. Radio Configuration Application (RCA) GUI

The Radio Configuration Application (RCA) GUI is part of the Wireless Development Suite (WDS) program. This setup interface provides an easy path to quickly selecting and loading the desired configuration for the device. The RCA allows for two different methods for device setup. One option is the configuration table, which provides a list of preloaded, common configurations. A second option allows for custom configurations to be loaded. After the desired configuration is selected, the RCA automatically creates the EZConfig configuration array that will be passed to the chip for setup. The program then gives the option to load a sample project with the selected configuration onto the evaluation board or launch IDE with the new configuration array preloaded into the user program. For more information on EZConfig usage, refer to application note, “AN692: Si4355/Si4455 Programming Guide”.

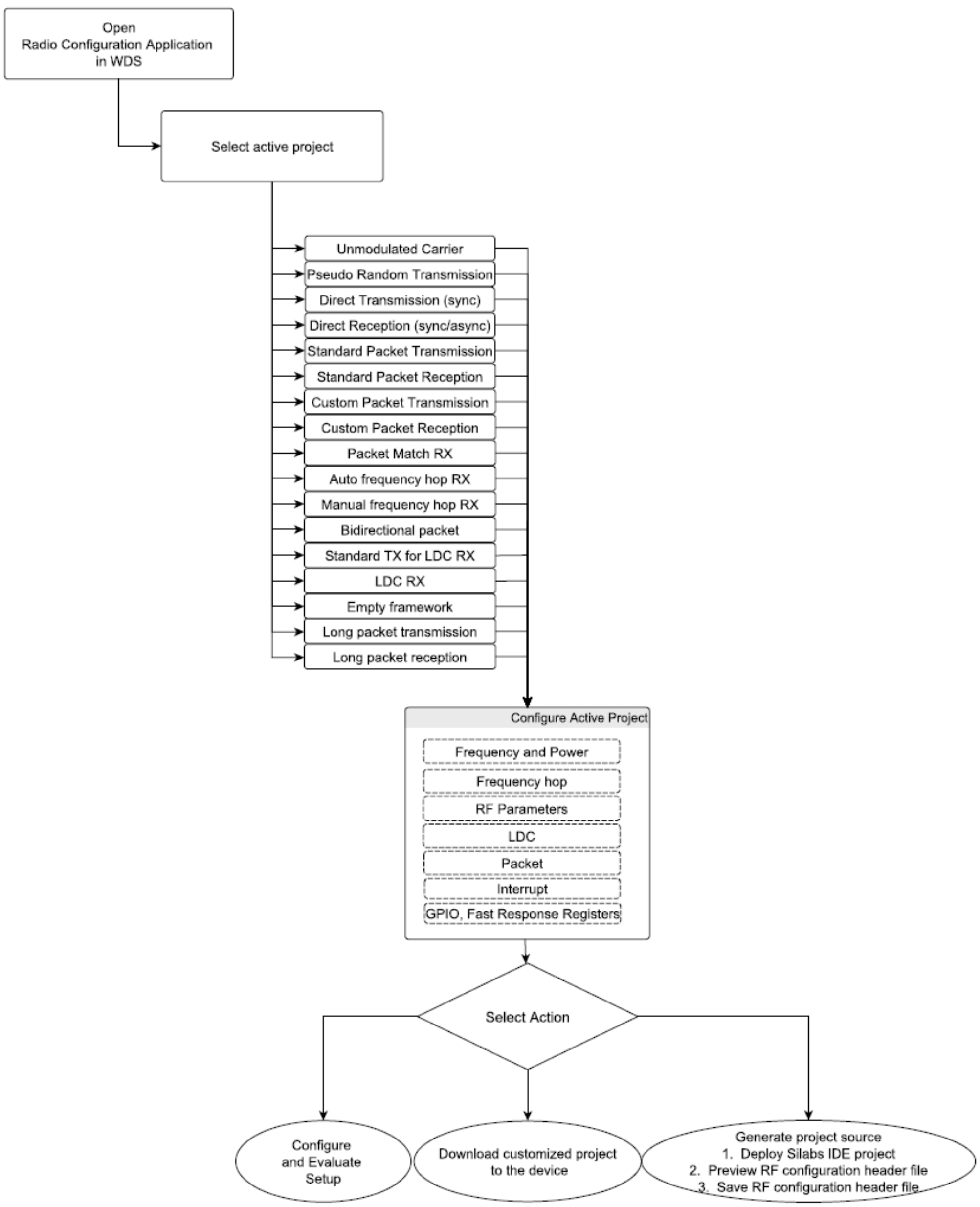


Figure 5. Device Configuration Options

4.1.1. Configuration Table

The configuration table is a list of predefined configurations that have been optimized for performance and validated by Silicon Labs. These configurations are listed for many common application conditions and so most users will be able to find the configuration they need in this table. These configurations are set to provide optimized performance for a given application and can be implemented with low design risk. Once the list item is selected, the specific frequency, power level, and packet handler features can also be applied.

4.1.2. Radio Configuration Application

The Radio Configuration Application provides an intuitive interface for directly modifying the device configuration. Using this control panel, the device parameters such as modulation type, data rate, frequency deviation, and any packet related settings can be set. The program then takes these parameters and automatically determines the appropriate device settings. This method allows the user to have complete flexibility in determining the configuration of the device without the need to translate the system requirements into device specific properties. The resulting configuration array is automatically generated and available for use in the user's program. The resulting configuration array is obfuscated; therefore, its content changes every time a new array is generated, even if the input parameters are the same.

4.2. Configuration Options

4.2.1. Frequency Band

The Si4455 can operate in the 283–350 MHz, 425–525 MHz, or 850–960 MHz bands. One of these three bands will be selected during the configuration setup and then the specific transmission frequency that will be used within this band can be selected.

4.2.2. Modulation Type

The Si4455 can operate using On/Off Keying (OOK), Frequency Shift Keying (FSK), or Gaussian Frequency Shift Keying (GFSK). OOK modulation is the most basic modulation type available. It is the most power-efficient method and does not require as high oscillator accuracy as FSK. FSK provides the best sensitivity and range performance, but generally requires more precision from the oscillator used. GFSK is a version of FSK where the signal is passed through a Gaussian filter, limiting its spectral width. As a result, the out-of-band components of the signal are reduced.

The Si4455 also has an option for Manchester coding. This method provides a state transition at each bit and so allows for more reliable clock recovery. Manchester code is available only when using the packet handler option and, if selected, will be applied to the entire packet (the preamble pattern is set to continuous “1” if the Manchester mode is enabled; therefore, the chip rate of the resulting preamble pattern is the same as for the rest of the packet). The polarity can be configured to a “10” or “01”.

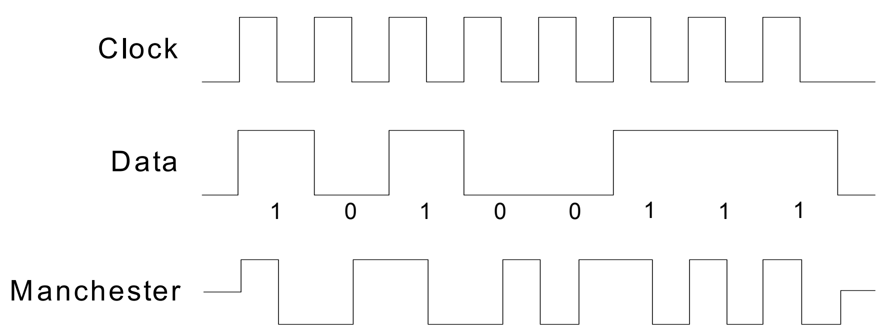


Figure 6. Manchester Code Example

4.2.3. Frequency Deviation

If FSK or GFSK modulation is selected, then a frequency deviation will also need to be selected. The frequency deviation is the maximum instantaneous difference between the FM modulated frequency and the nominal carrier frequency. The Si4455 can operate across a wide range of data rates and frequency deviations. If a frequency deviation needs to be selected, the following guideline might be helpful to build a robust link. A proper frequency deviation is linked to the frequency error between transmitter and receiver. The frequency error can be calculated using the crystal tolerance parameters and the RF operating frequency: (ppm_tx+ppm_rx)*Frf/1E-6. For frequency errors below 50 kHz, the deviation can be about the same as the frequency error. For frequency errors exceeding 50 kHz, the frequency deviation can be set to about 0.75 times the frequency error. It is advised to position the modulation index (= 2*freq_dev/data_rate) into a range between 1 and 100 for Packet Handling mode and 2 to 100 for direct mode (non-standard preamble). For example, when in Packet Handling mode and the frequency error is smaller than data_rate/2, the frequency deviation is set to about data_rate/2. When the frequency error exceeds 100xdata_rate/2, the frequency deviation is preferred to be set to 100xdata_rate/2.

4.2.4. Data Rate

The Si4455 can be set to communicate at between 1 to 500 kbps in (G)FSK mode and between 0.5 to 120 kbps in OOK mode. Higher data rates allow for faster data transfer while lower data rates result in improved sensitivity and range performance.

4.2.5. Channel Bandwidth

The channel bandwidth sets the bandwidth for the receiver. Since the receiver bandwidth is directly proportional to the noise allowed in the system, this will normally be set as low as possible. The specific channel bandwidth used will usually be determined based upon the precision of the oscillator and the frequency deviation of the transmitted signal. The RCA can provide the recommended channel bandwidth based upon these two parameters to help optimize the system.

4.2.6. Preamble Length

A preamble is a defined simple bit sequence used to notify the receiver that a data transmission is imminent. The length of this preamble will normally be set as short as possible to minimize power while insuring that it will be reliably detected given the receiver characteristics, such as duty cycling and packet error rate performance. The Si4455 allows the preamble length to be set between 0 to 255 bytes in length with a default length of 4 bytes. The preamble pattern for the Si4455 will always be 55h with a first bit of "0" if the packet handler capability is used.

4.2.7. Sync Word Length and Pattern

The sync word follows the preamble in the packet structure and is used to identify the start of the payload data and to synchronize the receiver to the transmitted bit stream. The Si4455 allows for sync word lengths of 1 to 4 bytes and the specific pattern can be set within the RCA program. The default is a 2 byte length 2d d4 pattern.

4.2.8. Cyclic Redundancy Check

Cyclic Redundancy Check (CRC) is used to verify that no errors have occurred during transmission and the received packet has exactly the same data as it did when transmitted. If this function is enabled in the Si4455, the last byte of transmitted data must include the CRC generated by the transmitter. The Si4455 then performs a CRC calculation on the received packet and compares that to the transmitted CRC. If these two values are the same, the Si4455 will set an interrupt indicating a valid packet has been received and is waiting in the Rx FIFO. If these two CRC values differ, the Si4455 will flag an interrupt indicating that a packet error occurred. The Si4455 uses CRC(16)-IBM: x16+x15+x2+1 with a seed of 0xFFFF.

4.3. Configuration Commands

The RCA provides all of the code needed for basic radio configuration. Once the setup is completed in the GUI, the program outputs configuration array(s) that can be sent to the radio via the SPI interface. No additional setup coding is needed. The configuration command process is shown in Figure 7. As shown below, the configuration is sent to the device in two EZCONFIG_ARRAY_WRITE commands with a NOP between them. The second EZCONFIG_ARRAY_WRITE can be sent after CTS is received for the NOP command. The NOP can be sent immediately after the first EZCONFIG_ARRAY_WRITE command. EZCONFIG_ARRAY_WRITE uses the same command code as WRITE_TX_FIFO (0x66). The EZCONFIG_SETUP passes the configuration array to the device and the EZCONFIG_CHECK insures that all of the configuration data was written correctly. For more information on the setup commands, refer to “AN692: Si4355/Si4455 Programming Guide” and the EZRadio API Documentation zip file available from www.silabs.com.

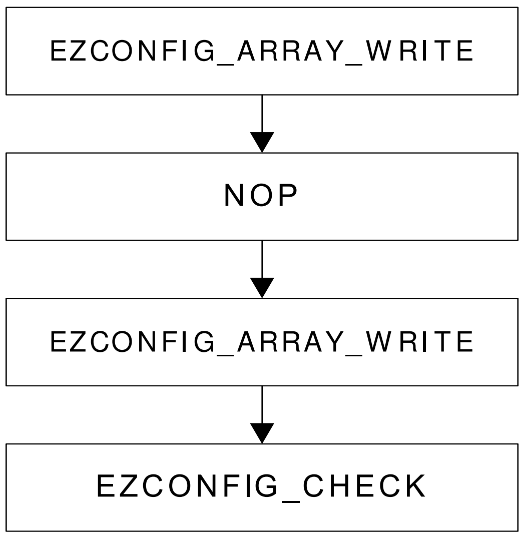


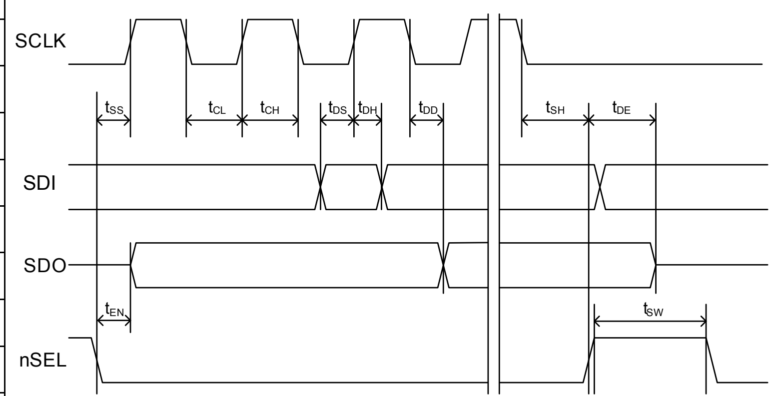
Figure 7. Configuration Command Flowchart

5. Controller Interface

5.1. Serial Peripheral Interface

The Si4455 communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are listed in Table 11. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 8 shows an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the API commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 11. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

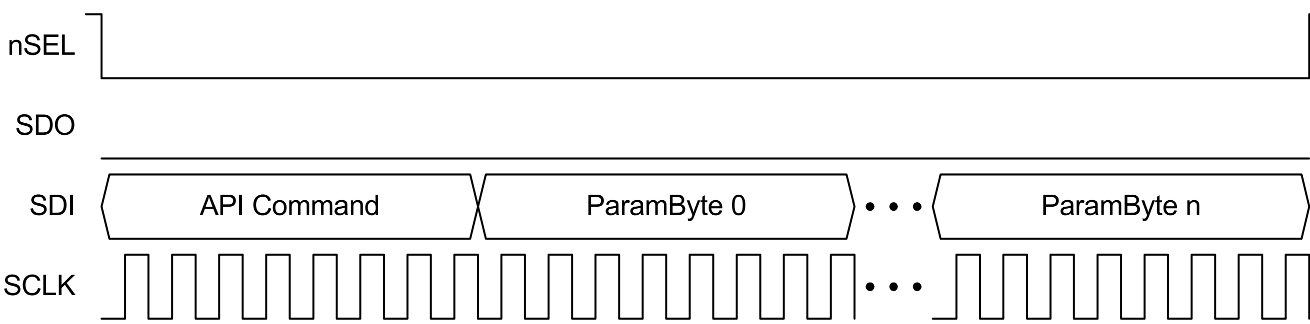


Figure 8. SPI Write Command

The Si4455 contains an internal MCU which controls all the internal functions of the radio. For SPI read commands, a typical communication flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 9 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh, then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 10 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

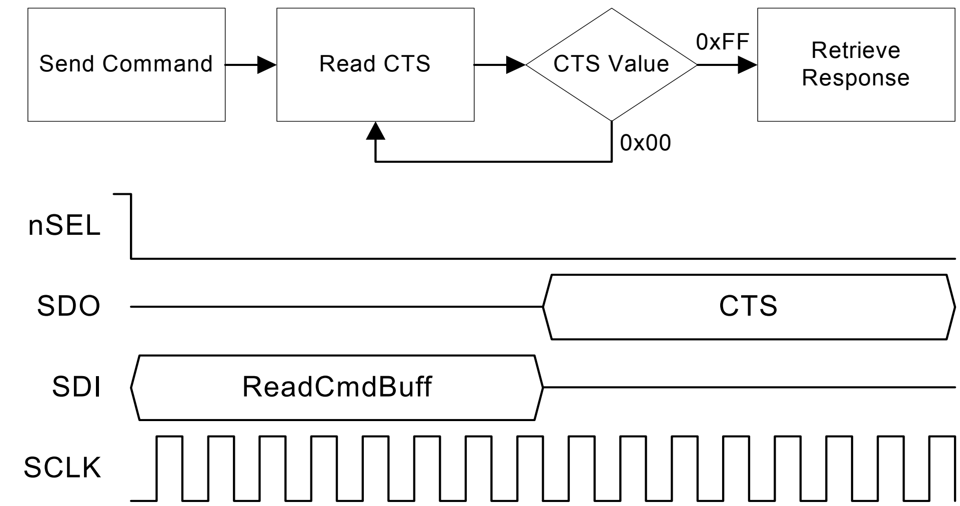


Figure 9. SPI Read Command—Check CTS Value

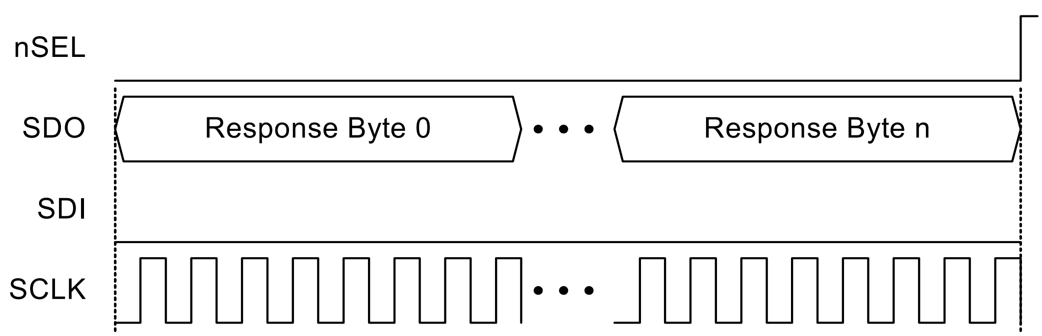


Figure 10. SPI Read Command—Clock Out Read Data

5.2. Operating Modes and Timing

The primary states of the Si4455 are shown in Figure 11. The shutdown state completely shuts down the radio, minimizing current consumption and is controlled using the SDN (pin 2). All other states are controlled using the API commands START_RX, START_TX and CHANGE_STATE. Table 12 shows each of the operating modes with the time required to reach either RX or TX state as well as the current consumption of each state. The times in Table 12 are measured from the rising edge of nSEL until the chip is in the desired state. This information is included for reference only since an automatic sequencer moves the chip from one state to another and so it is not necessary to manually step through each state. Figure 12 and Figure 13 demonstrate this timing and the current consumption for each radio state as the chip moves from shutdown or standby to TX and back. Most applications will utilize the standby mode since this provides the fastest transition response time, maintains all register values, and results in nearly the same current consumption as shutdown.

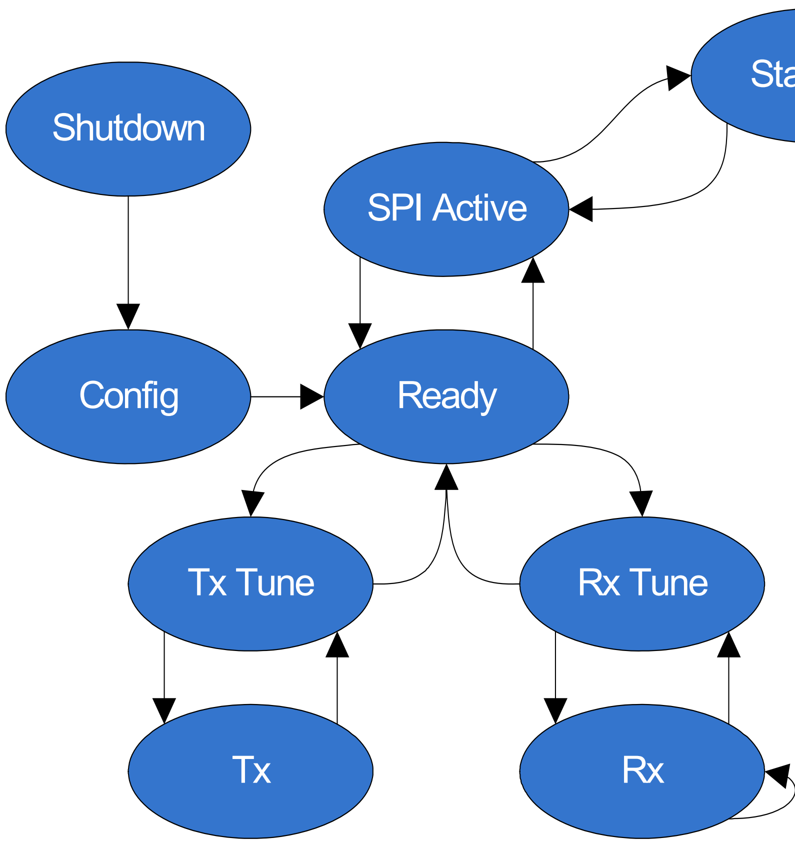


Figure 11. State Machine Diagram

Table 12. Operating State Response Time and Current Consumption

State / Mode	Response Time to		Current in State / Mode
	Tx	Rx	
Shutdown	30 ms	30 ms	30 nA
Standby	500 µs	460 µs	50 nA
SPI Active	500 µs	330 µs	1.35 mA
Ready	150 µs	130 µs	1.8 mA
Tx Tune	75 µs		6.9 mA
Rx Tune		75 µs	6.5 mA
Tx		150 µs	18 mA @ +10 dBm
Rx	150 µs	150 µs	10 mA

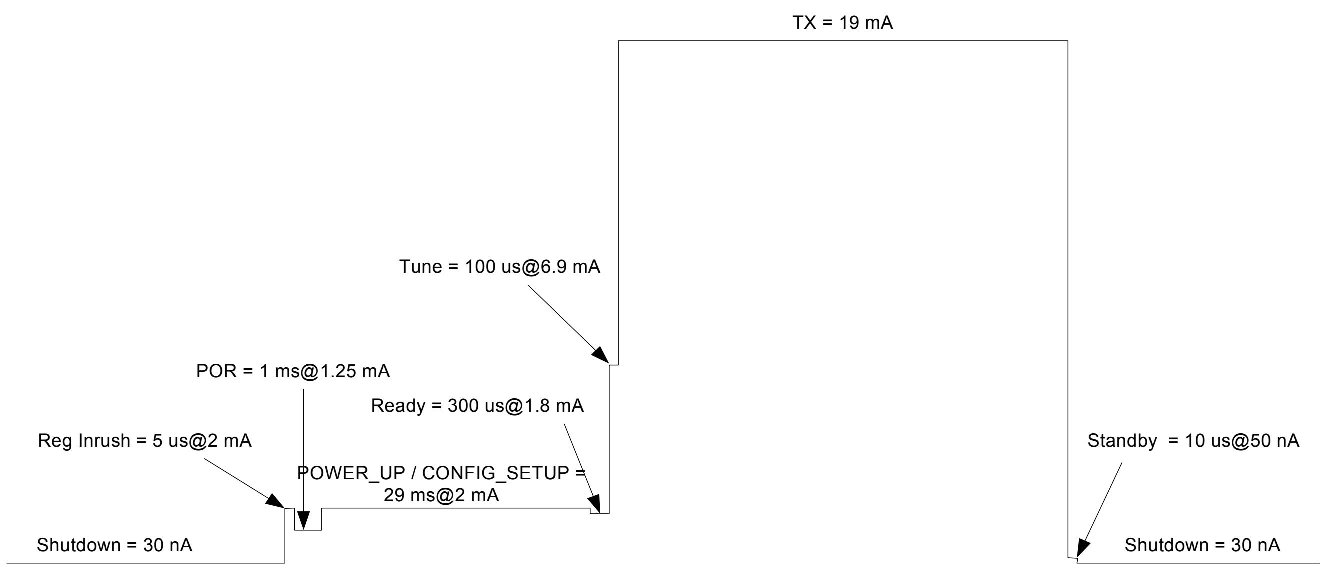


Figure 12. Start-Up Timing and Current Consumption using Shutdown State