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Si4464/63/61/60

HIGH-PERFORMANCE, LOW-CURRENT TRANSCEIVER

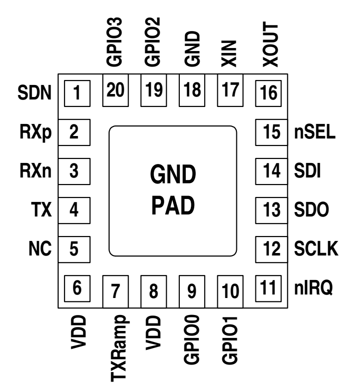
Features

- Frequency range = 119–1050 MHz
- Receive sensitivity = –126 dBm
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK
  - OOK
- Max output power
  - +20 dBm (Si4464/63)
  - +16 dBm (Si4461)
  - +13 dBm (Si4460)
- PA support for +27 or +30 dBm
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm (Si4460)
- Ultra low current powerdown modes
  - 30 nA shutdown, 50 nA standby
- Data rate = 100 bps to 1 Mbps
- Fast wake and hop times
- Power supply = 1.8 to 3.6 V
- Excellent selectivity performance
  - 60 dB adjacent channel
  - 75 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- Low BOM
- Low battery detector
- Temperature sensor
- 20-Pin QFN package
- IEEE 802.15.4g compliant
- FCC Part 90 Mask D, FCC part 15.247, 15,231, 15,249, ARIB T-108, T-96, T-67, RCR STD-30, China regulatory
- ETSI Class-I Operation with SAW

Applications

- Smart metering (802.15.4g & MBus)
- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Electronic shelf labels

Pin Assignments

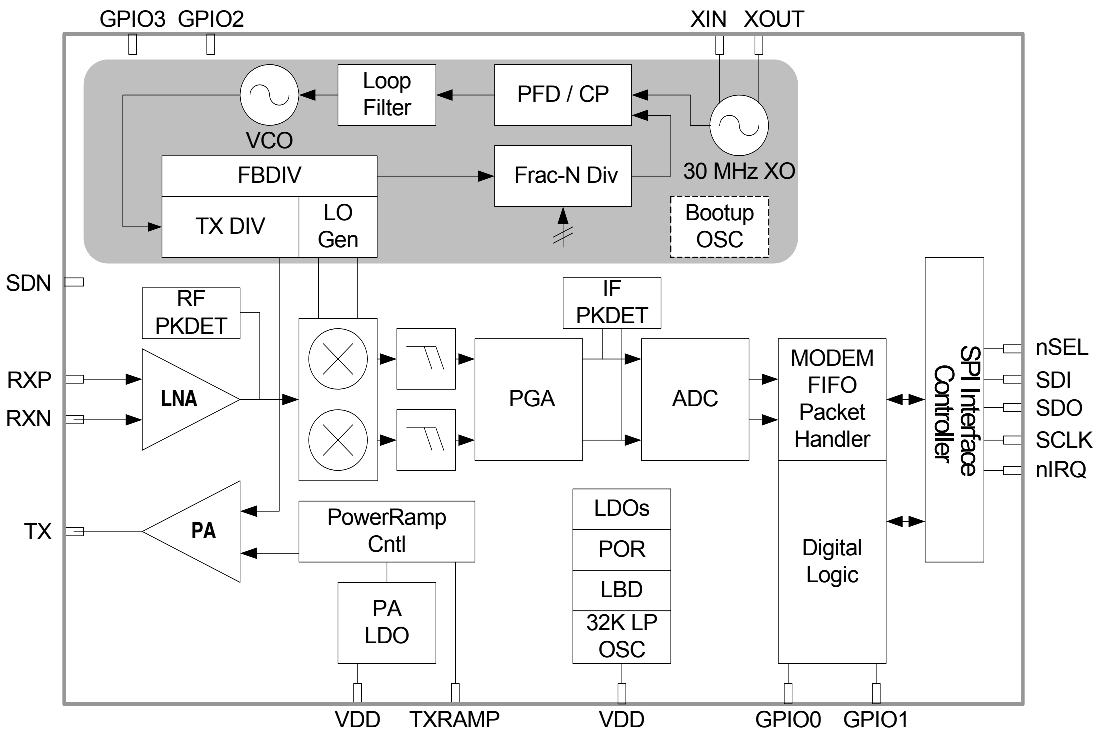


Patents pending

Description

Silicon Laboratories' Si446x devices are high-performance, low-current transceivers covering the sub-GHz frequency bands from 119 to 1050 MHz. The radios are part of the EZRadioPRO® family, which includes a complete line of transmitters, receivers, and transceivers covering a wide range of applications. All parts offer outstanding sensitivity of –126 dBm while achieving extremely low active and standby current consumption. The Si4463/61/60 offers frequency coverage in all major bands. The Si4464 offers frequency coverage in bands not covered by Si4463/61/60. Typically, these are non-standard frequencies or licensed frequency bands. The Si446x includes optimal phase noise, blocking, and selectivity performance for narrow band and licensed band applications, such as FCC Part90 and 169 MHz wireless Mbus. The 60 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The Si4464/63 offers exceptional output power of up to +20 dBm with outstanding TX efficiency. The high output power and sensitivity results in an industry-leading link budget of 146 dB allowing extended ranges and highly robust communication links. The Si4460 active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times ensure extended battery life in the most demanding applications. The Si4464/63 can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be configured via the Wireless Development Suite (WDS) available on the Silicon Labs web site.

Functional Block Diagram



Product	Freq. Range	Max Output Power	TX Current	RX Current	Narrow Band Support	Image Cal
Si4464	Banded 119–960 MHz	+20 dBm	915 MHz: 85 mA	10.6/13.6 mA	✓	✓
Si4463	Major bands 142-1050 MHz	+20 dBm	169 MHz: 70 mA 915 MHz: 85 mA	10/13 mA	✓	✓
Si4461	Major bands 142-1050 MHz	+16 dBm	+13 dBm: 29 mA +14 dBm: 33 mA	10/13 mA	✓	✓
Si4460	Major bands 142-1050 MHz	+13 dBm	+10 dBm: 18 mA +11 dBm: 20 mA	10/13 mA	✓	✓

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1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.8	3.3	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	—	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF	—	50	—	nA
	$I_{SleepRC}$	RC Oscillator/WUT ON and all register values maintained, and all other blocks OFF	—	900	—	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal.[2]	—	1.7	—	µA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
TUNE Mode Current	I_{Tune_RX}	RX Tune, High Performance Mode	—	7.2	—	mA
	I_{Tune_TX}	TX Tune, High Performance Mode	—	8	—	mA
RX Mode Current	I_{RXH}	High Performance Mode	—	13.7	—	mA
	I_{RXL}	Low Power Mode[2]	—	10.7	—	mA
TX Mode Current (Si4464/63)	I_{TX_+20}	+20 dBm output power, class-E match, 915 MHz, 3.3 V	—	85	—	mA
		+20 dBm output power, class-E match, 460 MHz, 3.3 V	—	75	—	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	70	—	mA
TX Mode Current (Si4461)	I_{TX_+16}	+16 dBm output power, class-E match, 868 MHz, 3.3 V[2]	—	43	—	mA
	I_{TX_+14}	+14 dBm output power, Switched-current match, 868 MHz, 3.3 V[2]	—	37	—	mA
	I_{TX_+13}	+13 dBm output power, switched-current match, 868 MHz, 3.3 V[2]	—	29	—	mA
TX Mode Current (Si4460)	I_{TX_+10}	+10 dBm output power, Class-E match, 868 MHz, 3.3 V[2]	—	18	—	mA

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section of "1.1. Definition of Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in the “Qualification Test Conditions” section in "1.1. Definition of Test Conditions" on page 14.

Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range (Si4463/61/60)	F_{SYN}		850	—	1050	MHz
			420	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Range (Si4464)	F_{SYN}		705	—	960	MHz
			353	—	639	MHz
			177	—	319	MHz
			119	—	159	MHz
Synthesizer Frequency Resolution[3]	$F_{RES\text{-}960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES\text{-}525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES\text{-}350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES\text{-}175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Frequency Resolution (Si4464)[3]	$F_{RES\text{-}960}$	705–960 MHz	—	28.6	—	Hz
	$F_{RES\text{-}639}$	470–639 MHz	—	19.1	—	Hz
	$F_{RES\text{-}479}$	353–479 MHz	—	14.3	—	Hz
	$F_{RES\text{-}319}$	235–319 MHz	—	9.5	—	Hz
	$F_{RES\text{-}239}$	177–239 MHz	—	7.1	—	Hz
	$F_{RES\text{-}159}$	119–159 MHz	—	4.7	—	Hz
Synthesizer Settling Time[4]	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	µs
Phase Noise[4]	$L\phi(f_M)$	ΔF = 10 kHz, 460 MHz, High Perf Mode	—	–106	—	dBc/Hz
		ΔF = 100 kHz, 460 MHz, High Perf Mode	—	–110	—	dBc/Hz
		ΔF = 1 MHz, 460 MHz, High Perf Mode	—	–123	—	dBc/Hz
		ΔF = 10 MHz, 460 MHz, High Perf Mode	—	–130	—	dBc/Hz

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section in "1.1. Definition of Test Conditions" on page 14.
2. For applications that use the major bands covered by Si4463/61/60, customers should use those parts instead of Si4464.
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.

Table 3. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range (Si4463/61/60)	F_{RX}		850	—	1050	MHz
			420	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
RX Frequency Range (Si4464)	F_{RX}		705	—	960	MHz
			353	—	639	MHz
			177	—	319	MHz
			119	—	159	MHz

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. For applications that use the major bands covered by Si4463/61/60, customers should use those parts instead of Si4464.
3. Guaranteed by qualification. BER is specified for the 450–470 MHz band. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
4. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used. PER and BER tested in the 450–470 MHz band.
5. Guaranteed by bench characterization.

Table 3. Receiver AC Electrical Characteristics[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)[3]	—	–126	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)[3]	—	–110	—	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)[1]	—	–106	—	dBm
	P_{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, Δf = ±62.5 kHz)[3]	—	–105	—	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)[3]	—	–97	—	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)[3,4]	—	–110	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)[3,4]	—	–88	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)[3]	—	–110	—	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)[3]	—	–104	—	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)[3]	—	–99	—	dBm
RX Channel Bandwidth[5]	BW		1.1	—	850	kHz
BER Variation vs Power Level[3]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. For applications that use the major bands covered by Si4463/61/60, customers should use those parts instead of Si4464.
3. Guaranteed by qualification. BER is specified for the 450–470 MHz band. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
4. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used. PER and BER tested in the 450–470 MHz band.
5. Guaranteed by bench characterization.

Table 3. Receiver AC Electrical Characteristics[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
±1-Ch Offset Selectivity, 169 MHz[3]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz, channel spacing = 12.5 kHz	—	–60	—	dB
±1-Ch Offset Selectivity, 450 MHz[3]	$C/I_{1\text{-}CH}$		—	–58	—	dB
±1-Ch Offset Selectivity, 868 / 915 MHz[3]	$C/I_{1\text{-}CH}$		—	–53	—	dB
Blocking 1 MHz Offset[3]	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER = 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps, ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz	—	–75	—	dB
Blocking 8 MHz Offset[3]	$8M_{BLOCK}$		—	–84	—	dB
Image Rejection[3]	Im_{REJ}	No image rejection calibration. Rejection at the image frequency. IF = 468 kHz	—	35	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. IF = 468 kHz	—	55	—	dB

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. For applications that use the major bands covered by Si4463/61/60, customers should use those parts instead of Si4464.
3. Guaranteed by qualification. BER is specified for the 450–470 MHz band. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
4. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used. PER and BER tested in the 450–470 MHz band.
5. Guaranteed by bench characterization.

Table 4. Transmitter AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range (Si4463/61/60)	F_{TX}		850	—	1050	MHz
			420	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
TX Frequency Range (Si4464)	F_{TX}		705	—	960	MHz
			353	—	639	MHz
			177	—	319	MHz
			119	—	159	MHz
(G)FSK Data Rate[3,4]	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate[3,4]	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate[3,4]	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range[3]	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{350}	283–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Range (Si4464)[3]	Δf_{960}	705–960 MHz	—	1.5	—	MHz
	Δf_{639}	470–639 MHz	—	1	—	MHz
	Δf_{479}	353–479 MHz	—	750	—	kHz
	Δf_{319}	235–319 MHz	—	500	—	kHz
	Δf_{239}	177–239 MHz	—	375	—	kHz
	Δf_{159}	119–159 MHz	—	250	—	kHz

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. For applications that use the major bands covered by Si4463/61/60, customers should use those parts instead of Si4464.
3. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
4. The maximum data rate is dependant on the XTAL frequency and is calculated as per the formula:
   Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
5. Default API setting for modulation deviation resolution is double the typical value specified.
6. Output power is dependent on matching components and board layout.

Table 4. Transmitter AC Electrical Characteristics[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Modulation Deviation Resolution[2,5]	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Modulation Deviation Resolution (Si4464)[3]	$F_{RES-960}$	705–960 MHz	—	28.6	—	Hz
	$F_{RES-639}$	470–639 MHz	—	19.1	—	Hz
	$F_{RES-479}$	353–479 MHz	—	14.3	—	Hz
	$F_{RES-319}$	235–319 MHz	—	9.5	—	Hz
	$F_{RES-239}$	177–239 MHz	—	7.1	—	Hz
	$F_{RES-159}$	119–159 MHz	—	4.7	—	Hz
Output Power Range (Si4464/63)[6]	P_{TX}		–20	—	+20	dBm
Output Power Range (Si4461)[6]	P_{TX61}		–40	—	+16	dBm
Output Power Range (Si4460)[6]	P_{TX60}		–40	—	+13	dBm
TX RF Output Steps[3]	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.1	—	dB
TX RF Output Level[3] Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	1	—	dB
TX RF Output Level Variation vs. Frequency[3]	ΔP_{RF_FREQ}	Measured across 902–928 MHz	—	0.5	—	dB
Transmit Modulation Filtering[3]	B*T	Gaussian Filtering Bandwith Time Product	—	0.5	—	

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. For applications that use the major bands covered by Si4463/61/60, customers should use those parts instead of Si4464.
3. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
4. The maximum data rate is dependant on the XTAL frequency and is calculated as per the formula:
   Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
5. Default API setting for modulation deviation resolution is double the typical value specified.
6. Output power is dependent on matching components and board layout.

Table 5. Auxiliary Block Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Sensor Sensitivity[2]	TS_S		—	4.5	—	ADC Codes/ °C
Low Battery Detector Resolution	LBD_{RES}		—	50	—	mV
Microcontroller Clock Output Frequency Range[3]	F_{MC}	Configurable to Fxtal or Fxtal divided by 2, 3, 7.5, 10, 15, or 30 where Fxtal is the reference XTAL frequency. In addition, 32.768 kHz is also supported.	32.768K	—	Fxtal	Hz
Temperature Sensor Conversion[2]	$TEMP_{CT}$	Programmable setting	—	3	—	ms
XTAL Range[4]	$XTAL_{Range}$		25		32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	250	—	µs
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	70	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	2	—	sec
32 kHz Accuracy using Internal RC Oscillator[2]	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	—	5	ms

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
3. Microcontroller clock frequency tested in production at 1 MHz, 30 MHz and 32.768 kHz. Other frequencies tested in bench characterization.
4. XTAL Range tested in production using an external clock source (similar to using a TCXO).

Table 6. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ, SDN)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time[2,3]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = HH	—	2.3	—	ns
Fall Time[3,4]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = HH	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	$0<V_{IN}<V_{DD}$	–10	—	10	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	10	µA
Drive Strength for Output Low Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	1.13	—	mA
Drive Strength for Output High Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.96	—	mA
Drive Strength for Output High Level for GPIO0	I_{OmaxLL}	DRV[1:0] = LL[3]	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	1.7	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD} x 0.2	V

Notes:
1. All specifications guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 14.
2. 8 ns is typical for GPIO0 rise time.
3. Assuming VDD = 3.3 V, drive strength is specified at Voh (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.
4. 2.4 ns is typical for GPIO0 fall time.

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
Instantaneous $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +8.0	V
Sustained $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +6.5	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.

1.1. Definition of Test Conditions

Production Test Conditions:

- T_A = +25 °C.
- V_{DD} = +3.3 VDC.
- TX output power measured at 915 MHz.
- External reference signal (XOUT) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC.
- Production test schematic (unless noted otherwise).
- All TX output levels are referred to the pins of the Si4464/63/61/60 (not the output of the RF module).
- All RX input levels are referred to the input of a tuned balun connected to the RX input pins of the Si4464/63/61/60.

Qualification Test Conditions:

- T_A = –40 to +85 °C (Typical T_A = 25 °C).
- V_{DD} = +1.8 to +3.6 VDC (Typical V_{DD} = 3.3 VDC).
- Using TX/RX Split Antenna reference design or production test schematic.
- All RF input and output levels referred to the pins of the Si4464/63/61/60 (not the RF module).

2. Functional Description

The Si446x devices are high-performance, low-current, wireless ISM transceivers that cover the sub-GHz bands. The wide operating voltage range of 1.8–3.6 V and low current consumption make the Si446x an ideal solution for battery powered applications. The Si446x operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2/4-level FSK/GFSK or OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance $\Delta\Sigma$ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and $\Delta\Sigma$ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 100 bps to 1 Mbps. The Si4463/61/60 operate in the frequency bands of 142–175, 283–350, 420–525, and 850–1050 MHz with a maximum frequency accuracy step size of 28.6 Hz. The Si4464 offers frequency coverage in bands not supported by Si4463/61/60. The transmit FSK data is modulated directly into the $\Delta\Sigma$ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The Si4464/63 contains a power amplifier (PA) that supports output power up to +20 dBm with very high efficiency, consuming only 70 mA at 169 MHz and 85 mA at 915 MHz. The integrated +20 dBm power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. Competing solutions require large and expensive external PAs to achieve comparable performance. The Si4461 supplies output power up to +16 dBm. The Si4460 is designed to support single coin cell operation with current consumption below 18 mA for +10 dBm output power. Two match topologies are available for the Si4461 and Si4460, class-E and switched-current. Class-E matching provides optimal current consumption, while switched-current matching demonstrates the best performance over varying battery voltage and temperature with slightly higher current consumption. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The Si446x family supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. Antenna diversity is completely integrated into the Si446x and can improve the system link budget by 8–10 dB, resulting in substantial range increases under adverse environmental conditions. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure. Additional system features, such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, and preamble detection, reduce overall current consumption and allows for the use of lower-cost system MCUs. An integrated temperature sensor, power-on-reset (POR), and GPIOs further reduce overall system cost and size. The Si446x is designed to work with an MCU, crystal, and a few passive components to create a very low-cost system.

The application shown in Figure 1 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most applications with output power less than 17 dBm will use this configuration. Figure 2 demonstrates an application for +20 dBm using an external T/R-switch.

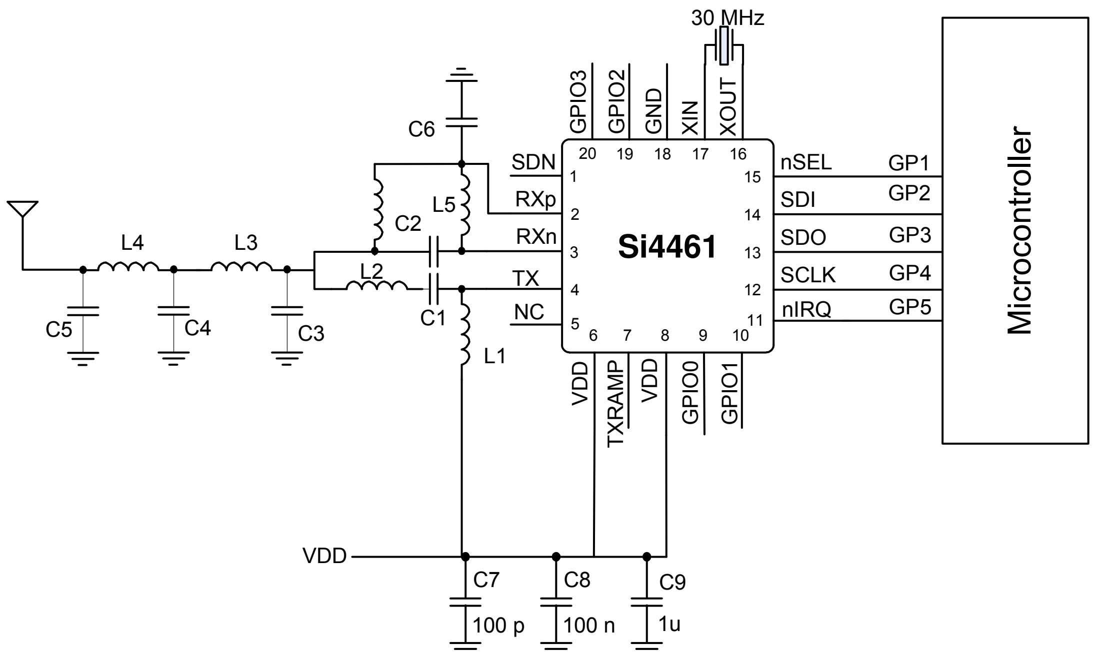


Figure 1. Si4461 Direct-Tie Application Example

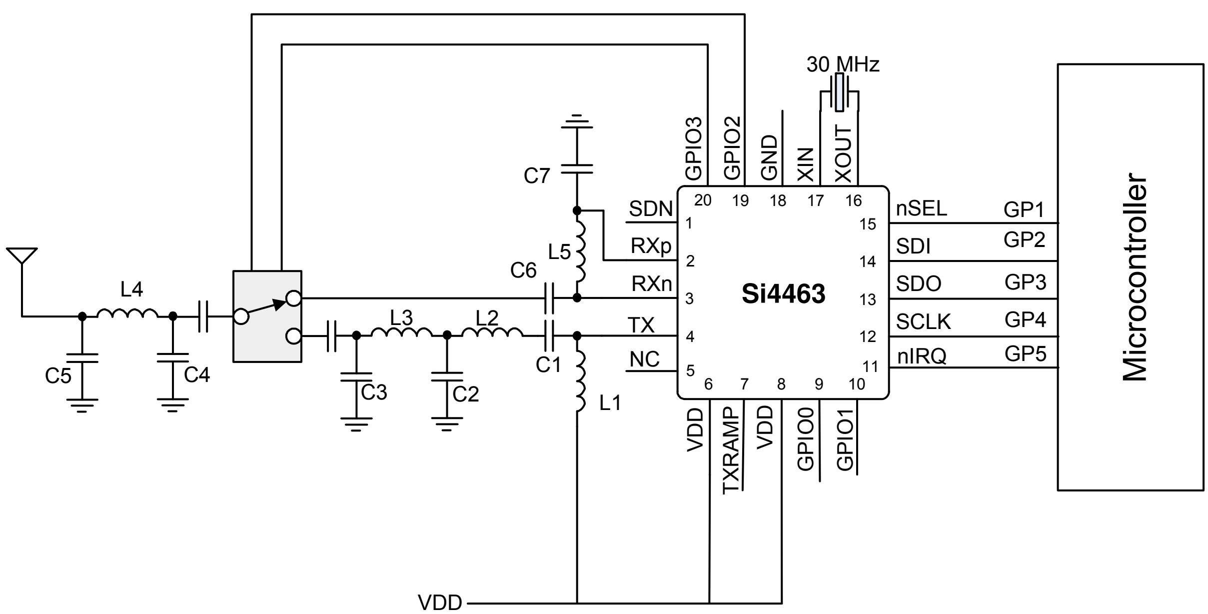


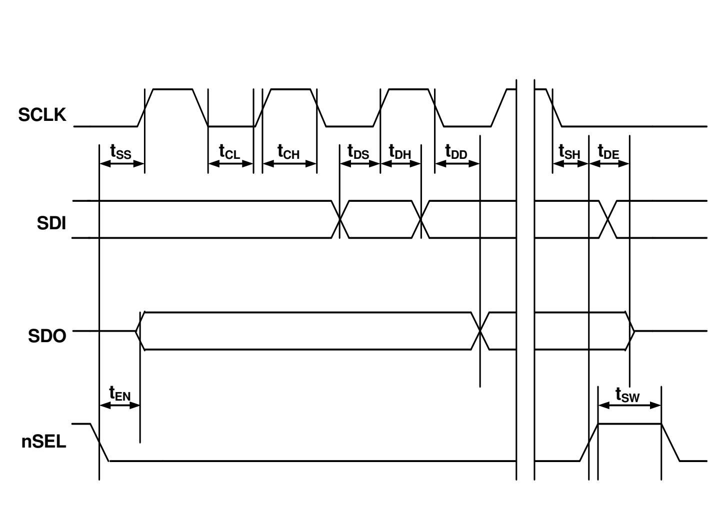
Figure 2. Si4463 Single Antenna with RF Switch Example

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si446x communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are demonstrated in Table 8. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 3 demonstrates an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the firmware commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 8. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

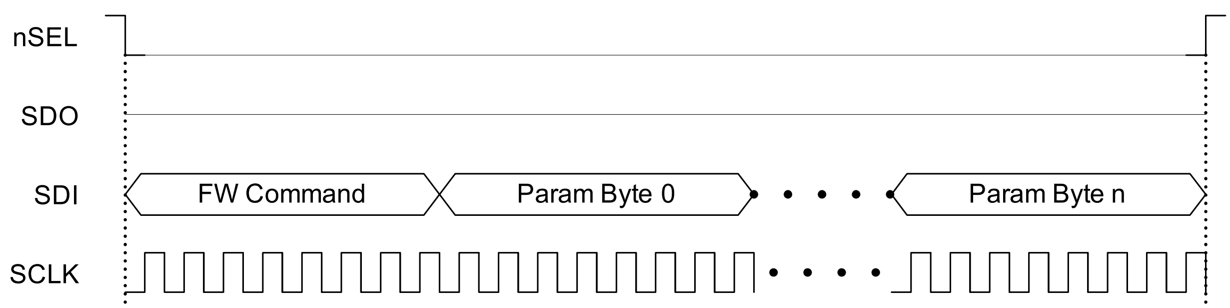
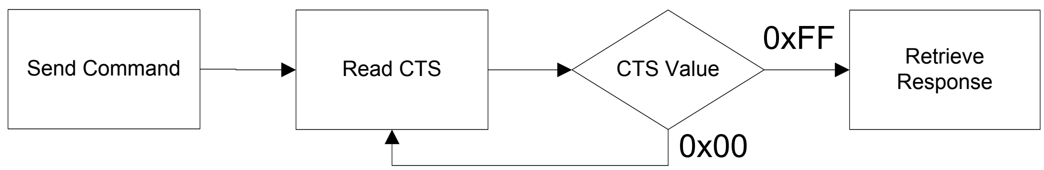


Figure 3. SPI Write Command

The Si446x contains an internal MCU which controls all the internal functions of the radio. For SPI read commands a typical MCU flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 4 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 5 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

Firmware Flow



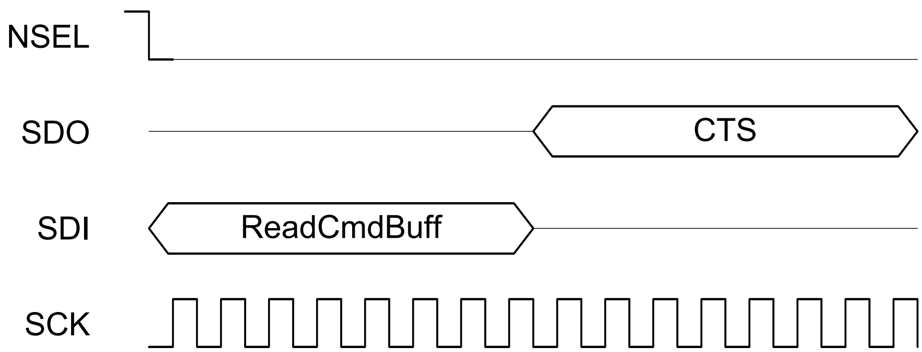


Figure 4. SPI Read Command—Check CTS Value

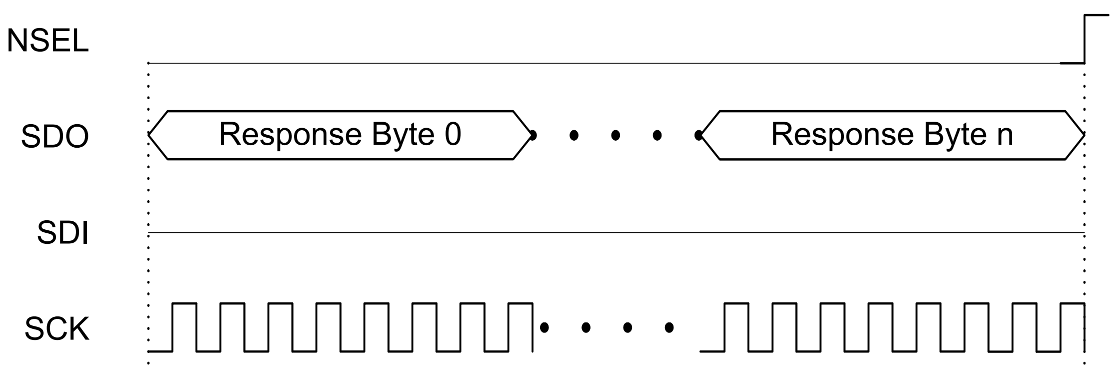


Figure 5. SPI Read Command—Clock Out Read Data

3.2. Fast Response Registers

The fast response registers are registers that can be read immediately without the requirement to monitor and check CTS. There are four fast response registers that can be programmed for a specific function. The fast response registers can be read through API commands, 0x50 for Fast Response A, 0x51 for Fast Response B, 0x53 for Fast Response C, and 0x57 for Fast Response D. The fast response registers can be configured by the "FRR_CTL_X_MODE" properties.

The fast response registers may be read in a burst fashion. After the initial 16 clock cycles, each additional eight clock cycles will clock out the contents of the next fast response register in a circular fashion. The value of the FRRs will not be updated unless NSEL is toggled.

3.3. Operating Modes and Timing

The primary states of the Si446x are shown in Figure 6. The shutdown state completely shuts down the radio to minimize current consumption. Standby/Sleep, SPI Active, Ready, TX Tune, and RX tune are available to optimize the current consumption and response time to RX/TX for a given application. API commands START_RX, START_TX, and CHANGE_STATE control the operating state with the exception of shutdown which is controlled by SDN, pin 1. Table 9 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode. The times in Table 9 are measured from the rising edge of nSEL until the chip is in the desired state. Note that these times are indicative of state transition timing but are not guaranteed and should only be used as a reference data point. An automatic sequencer will put the chip into RX or TX from any state. It is not necessary to manually step through the states. To simplify the diagram it is not shown but any of the lower power states can be returned to automatically after RX or TX.

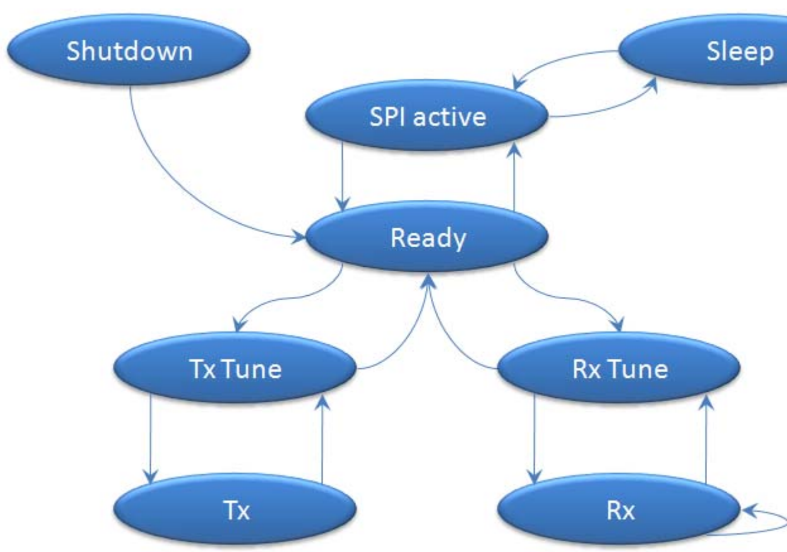


Figure 6. State Machine Diagram

Table 9. Operating State Response Time and Current Consumption*

State/Mode	Response Time to		Current in State /Mode
	TX	RX	
Shutdown State	15 ms	15 ms	30 nA
Standby State Sleep State SPI Active State Ready State TX Tune State RX Tune State	440 µs 440 µs 340 µs 126 µs 58 µs —	440 µs 440 µs 340 µs 122 µs — 74 µs	50 nA 900 nA 1.35 mA 1.8 mA 8 mA 7.2 mA
TX State	—	138 µs	18 mA @ +10 dBm
RX State	130 µs	75 µs	10 or 13 mA

***Note:** TX→RX and RX→TX state transition timing can be reduced to 70 µs if using Zero-IF mode.

Figure 7 shows the POR timing and voltage requirements. The power consumption (battery life) depends on the duty cycle of the application or how often the part is in either Rx or Tx state. In most applications the utilization of the standby state will be most advantageous for battery life but for very low duty cycle applications shutdown will have an advantage. For the fastest timing the next state can be selected in the START_RX or START_TX API commands to minimize SPI transactions and internal MCU processing.

3.3.1. Power on Reset (POR)

A Power On Reset (POR) sequence is used to boot the device up from a fully off or shutdown state. To execute this process, VDD must ramp within 1ms and must remain applied to the device for at least 10ms. If VDD is removed, then it must stay below 0.15V for at least 10ms before being applied again. Please see Figure x and Table x for details.

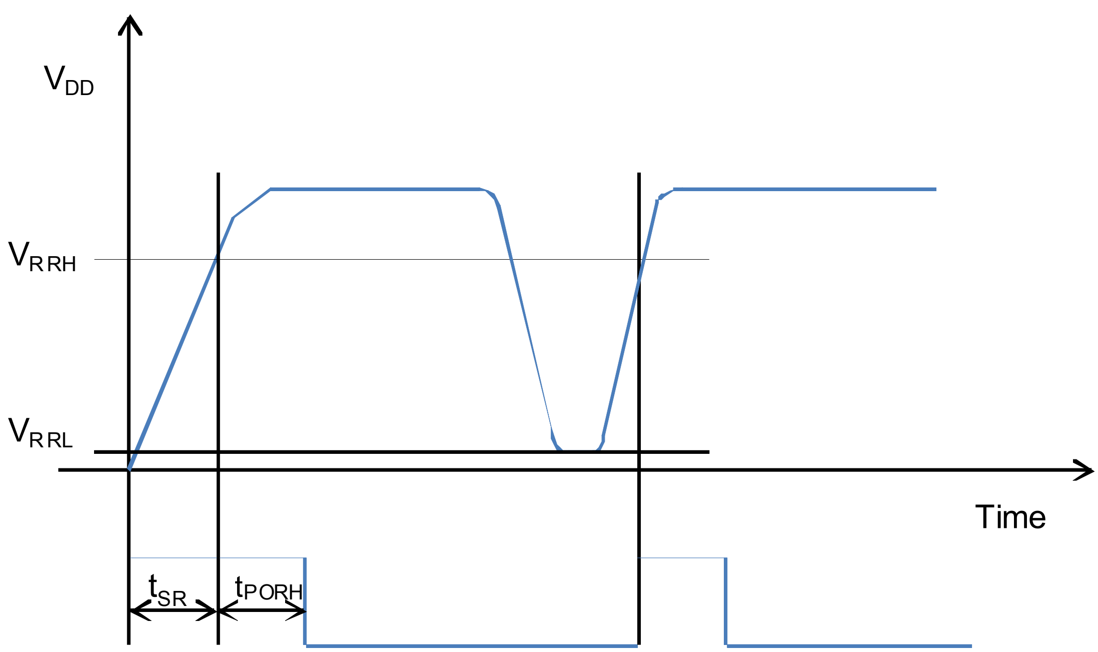


Figure 7. POR Timing Diagram

Table 10. POR Timing

Variable	Description	Min	Typ	Max	Units
t_{PORH}	High time for VDD to fully settle POR circuit	10			ms
t_{PORL}	Low time for VDD to enable POR	10			ms
V_{RRH}	Voltage for successful POR	90%*Vdd			V
V_{RRL}	Starting Voltage for successful POR	0		150	mV
t_{SR}	Slew rate of VDD for successful POR			1	ms

3.3.2. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 30 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 1) high. The SDN pin should be held low in all states except the shutdown state. In the shutdown state, the contents of the registers are lost and there is no SPI access. When coming out of the shutdown state a power on reset (POR) will be initiated along with the internal calibrations. After the POR the POWER_UP command is required to initialize the radio. The SDN pin needs to be held high for at least 10us before driving low again so that internal capacitors can discharge. Not holding the SDN high for this period of time may cause the POR to be missed and the device to boot up incorrectly. If POR timing and voltage requirements cannot be met, it is highly recommended that SDN be controlled using the host processor rather than tying it to GND on the board.

3.3.3. Standby State

Standby state has the lowest current consumption with the exception of shutdown but has much faster response time to RX or TX mode. In most cases standby should be used as the low power state. In this state the register values are maintained with all other blocks disabled. The SPI is accessible during this mode but any SPI event, including FIFO R/W, will enable an internal boot oscillator and automatically move the part to SPI active state. After an SPI event the host will need to re-command the device back to standby through the “Change State” API command to achieve the 50 nA current consumption. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.4. Sleep State

Sleep state is the same as standby state but the wake-up-timer and a 32 kHz clock source are enabled. The source of the 32 kHz clock can either be an internal 32 kHz RC oscillator which is periodically calibrated or a 32 kHz oscillator using an external XTAL.The SPI is accessible during this mode but an SPI event will enable an internal boot oscillator and automatically move the part to SPI active mode. After an SPI event the host will need to re-command the device back to sleep. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.5. SPI Active State

In SPI active state the SPI and a boot up oscillator are enabled. After SPI transactions during either standby or sleep the device will not automatically return to these states. A “Change State” API command will be required to return to either the standby or sleep modes.

3.3.6. Ready State

Ready state is designed to give a fast transition time to TX or RX state with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time.

3.3.7. TX State

The TX state may be entered from any of the state with the “Start TX” or “Change State” API commands. A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The following sequence of events will occur automatically when going from standby to TX state.

1. Enable internal LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).

3. Enable PLL.
4. Calibrate VCO/PLL.
5. Wait until PLL settles to required transmit frequency (controlled by an internal timer).
6. Activate power amplifier and wait until power ramping is completed (controlled by an internal timer).
7. Transmit packet.

Steps in this sequence may be eliminated depending on which state the chip is configured to prior to commanding to TX. By default, the VCO and PLL are calibrated every time the PLL is enabled. When the START_TX API command is utilized the next state may be defined to ensure optimal timing and turnaround.

Figure 8 shows an example of the commands and timing for the START_TX command. CTS will go high as soon as the sequencer puts the part into TX state. As the sequencer is stepping through the events listed above, CTS will be low and no new commands or property changes are allowed. If the Fast Response (FRR) or nIRQ is used to monitor the current state there will be slight delay caused by the internal hardware from when the event actually occurs to when the transition occurs on the FRR or nIRQ. The time from entering TX state to when the FRR will update is 5 µs and the time to when the nIRQ will transition is 13 µs. If a GPIO is programmed for TX state or used as control for a transmit/receive switch (TR switch) there is no delay.

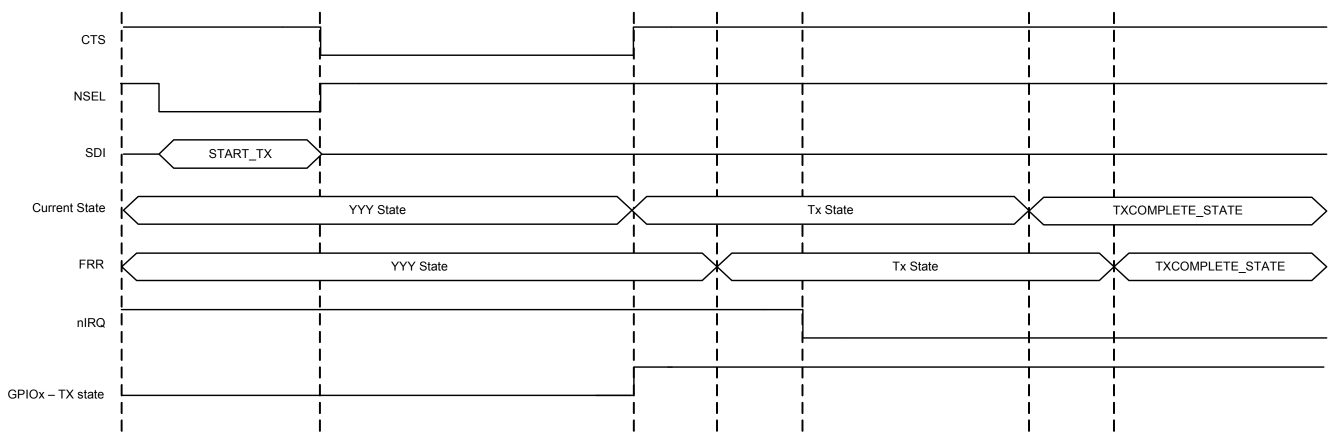


Figure 8. Start_TX Commands and Timing

3.3.8. RX State

The RX state may be entered from any of the other states by using the “Start RX” or “Change State” API command. A built-in sequencer takes care of all the actions required to transition between states. The following sequence of events will occur automatically to get the chip into RX mode when going from standby to RX state:

1. Enable the digital LDO and the analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO
5. Wait until PLL settles to required receive frequency (controlled by an internal timer).
6. Enable receiver circuits: LNA, mixers, and ADC.
7. Enable receive mode in the digital modem.

Depending on the configuration of the radio, all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC. Similar to the TX state, the next state after RX may be defined in the “Start RX” API command. The START_RX commands and timing will be equivalent to the timing shown in Figure 8.

3.4. Application Programming Interface (API)

An application programming interface (API), which the host MCU will communicate with, is embedded inside the device. The API is divided into two sections, commands and properties. The commands are used to control the chip and retrieve its status. The properties are general configurations which will change infrequently. The API descriptions can be found in“AN625: Si446x API Descriptions”.

3.5. Interrupts

The Si446x is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Registers. The nIRQ output signal will then be reset until the next change in status is detected.

The interrupts sources are grouped into three groups: packet handler, chip status, and modem. The individual interrupts in these groups can be enabled/disabled in the interrupt property registers, 0101, 0102, and 0103. An interrupt must be enabled for it to trigger an event on the nIRQ pin. The interrupt group must be enabled as well as the individual interrupts in API property 0100.

Number	Command	Summary
0x20	GET_INT_STATUS	Returns the interrupt status—packet handler, modem, and chip
0x21	GET_PH_STATUS	Returns the packet handler status.
0x22	GET_MODEM_STATUS	Returns the modem status byte.
0x23	GET_CHIP_STATUS	Returns the chip status.

Number	Property	Default	Summary
0x0100	INT_CTL_ENABLE	0x04	Enables interrupt groups for PH, Modem, and Chip.
0x0101	INT_CTL_PH_ENABLE	0x00	Packet handler interrupt enable property.
0x0102	INT_CTL_MODEM_ENABLE	0x00	Modem interrupt enable property.
0x0103	INT_CTL_CHIP_ENABLE	0x04	Chip interrupt enable property.

Once an interrupt event occurs and the nIRQ pin is low there are two ways to read and clear the interrupts. All of the interrupts may be read and cleared in the “GET_INT_STATUS” API command. By default all interrupts will be cleared once read. If only specific interrupts want to be read in the fastest possible method the individual interrupt groups (Packet Handler, Chip Status, Modem) may be read and cleared by the “GET_MODEM_STATUS”, “GET_PH_STATUS” (packet handler), and “GET_CHIP_STATUS” API commands.

The instantaneous status of a specific function maybe read if the specific interrupt is enabled or disabled. The status results are provided after the interrupts and can be read with the same commands as the interrupts. The status bits will give the current state of the function whether the interrupt is enabled or not.

The fast response registers can also give information about the interrupt groups but reading the fast response registers will not clear the interrupt and reset the nIRQ pin.

3.6. GPIO

Four general purpose IO pins are available to utilize in the application. The GPIO are configured by the GPIO_PIN_CFG command in address 13h. For a complete list of the GPIO options please see the API guide. GPIO pins 0 and 1 should be used for active signals such as data or clock. GPIO pins 2 and 3 have more susceptibility to generating spurious in the synthesizer than pins 0 and 1. The drive strength of the GPIOs can be adjusted with the GEN_CONFIG parameter in the GPIO_PIN_CFG command. By default the drive strength is set to minimum. The default configuration for the GPIOs and the state during SDN is shown below in Table 11.The state of the IO during shutdown is also shown inTable 11. As indicated previously in Table 6, GPIO 0 has lower drive strength than the other GPIOs.

Table 11. GPIOs

Pin	SDN State	POR Default
GPIO0	0	POR
GPIO1	0	CTS
GPIO2	0	POR
GPIO3	0	POR
nIRQ	resistive VDD pull-up	nIRQ
SDO	resistive VDD pull-up	SDO
SDI	High Z	SDI

4. Modulation and Hardware Configuration Options

The Si446x supports different modulation options and can be used in various configurations to tailor the device to any specific application or legacy system for drop in replacement. The modulation and configuration options are set in API property, MODEM_MOD_TYPE.

4.1. MODEM_MOD_TYPE

- Summary: Modulation Type
- Purpose:
  - This property selects between OOK, FSK, 4FSK and GFSK modulation, modulation source, and tx direct mode control.
  - The modulator must be configured for one mode through the entire packet. If portions of the packet alternate between FSK and 4FSK modes, the modem should be programmed to 4FSK mode.
- Property: 0x2000
- Default: 0x02
- Fields:
  - TX_DIRECT_MODE_TYPE - default:0

    0 = Direct mode operates in synchronous mode, applies to TX only.

    1 = Direct mode operates in asynchronous mode, applies to TX only. GFSK is not supported.
  - TX_DIRECT_MODE_GPIO[1:0] - default:0x0

    0 = TX direct mode uses gpio0 as data source, applies to TX only.

    1 = TX direct mode uses gpio1 as data source, applies to TX only.

    2 = TX direct mode uses gpio2 as data source, applies to TX only.

    3 = TX direct mode uses gpio3 as data source, applies to TX only.
  - MOD_SOURCE[1:0] - default:0x0

    0 = Modulation source is packet handler fifo

    1 = Modulation source is direct mode pin

    2 = Modulation source is pseudo-random generator
  - MOD_TYPE[2:0] - default:0x2

    0 = CW

    1 = OOK

    2 = 2FSK

    3 = 2GFSK

    4 = 4FSK

    5 = 4GFSK
- Register View

<table>
<tr><th colspan="8">MODEM_MOD_TYPE</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
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<tr><td>0</td><td colspan="2">0x0</td><td colspan="2">0x0</td><td colspan="3">0x2</td></tr>
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