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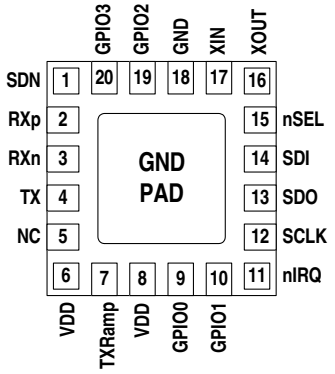
Si4463/61/60-C

HIGH-PERFORMANCE, LOW-CURRENT TRANSCEIVER

Features

- Frequency range = 142–1050 MHz
- Receive sensitivity = –129 dBm
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK
  - OOK
- Max output power
  - +20 dBm (Si4463)
  - +16 dBm (Si4461)
  - +13 dBm (Si4460)
- PA support for +27 or +30 dBm
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm (Si4460)
- Ultra low current powerdown modes
  - 30 nA shutdown, 40 nA standby
- Preamble sense mode
  - 6 mA average RX current at 1.2 kbps
  - 10 µA average RX current at 50 kbps and 1 sec sleep interval
- Fast preamble detection
  - 1 byte preamble detection
- Data rate = 100 bps to 1 Mbps
- Fast wake and hop times
- Power supply = 1.8 to 3.8 V
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
  - 129 bytes dedicated Tx or Rx
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- Low BOM
- Low battery detector
- Temperature sensor
- 20-Pin QFN package
- IEEE 802.15.4g and WMBus compliant
- Suitable for FCC Part 90 Mask D, FCC part 15.247, 15,231, 15,249, ARIB T-108, T-96, T-67, RCR STD-30, China regulatory
- ETSI Category I Operation EN300 220

Pin Assignments



Patents pending

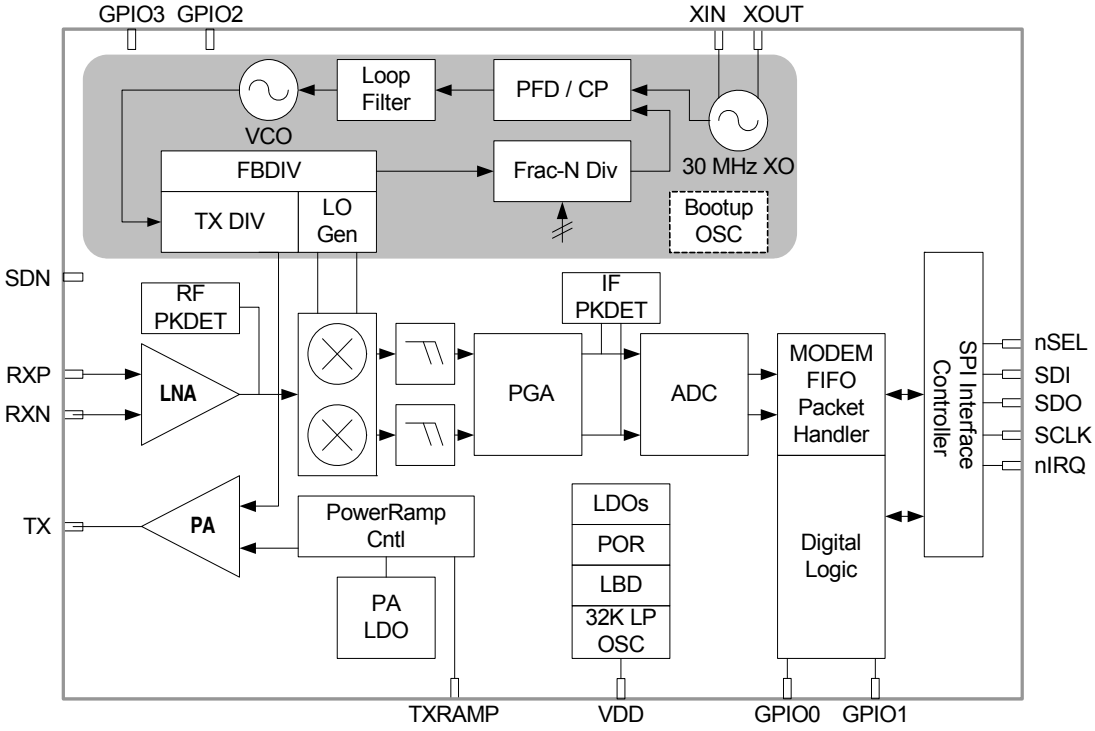
Applications

- Smart metering (802.15.4g and WMBus)
- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Electronic shelf labels

Description

Silicon Laboratories' Si446x devices are high-performance, low-current transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. The radios are part of the EZRadioPRO® family, which includes a complete line of transmitters, receivers, and transceivers covering a wide range of applications. All parts offer outstanding sensitivity of –129 dBm while achieving extremely low active and standby current consumption. The Si4463/61/60 offers frequency coverage in all major bands. The Si446x includes optimal phase noise, blocking, and selectivity performance for narrow band and wireless MBus licensed band applications, such as FCC Part90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The Si4463 offers exceptional output power of up to +20 dBm with outstanding TX efficiency. The high output power and sensitivity results in an industry-leading link budget of 146 dB allowing extended ranges and highly robust communication links. The Si4460 active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times ensure extended battery life in the most demanding applications. The Si4463 can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, wireless MBus, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be configured via the Wireless Development Suite (WDS) available on the Silicon Labs website.

Functional Block Diagram



Product	Freq. Range	Max Output Power	TX Current at Max Power and 868 MHz	Narrow Band Support	IEEE 802.15.4g PHY
Si4463	Major bands 142-1050 MHz	+20 dBm	85 mA	✓	✓
Si4461	Major bands 142-1050 MHz	+16 dBm	43 mA	✓	✓
Si4460	Major bands 142-1050 MHz	+13 dBm	24 mA	✓	✓

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.8	3.3	3.8	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	1300	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF	—	40	2900	nA
	$I_{SleepRC}$	RC Oscillator/WUT ON and all register values maintained, and all other blocks OFF	—	740	3800	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal	—	1.7	—	µA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
Preamble Sense Mode Current	I_{psm}	Duty cycling during preamble search, 1.2 kbps, 4 byte preamble	—	6	—	mA
	I_{psm}	Fixed 1 s wakeup interval, 50 kbps, 5 byte preamble	—	10	—	µA
TUNE Mode Current	I_{Tune_RX}	RX Tune, High Performance Mode	—	7.6	—	mA
	I_{Tune_TX}	TX Tune, High Performance Mode	—	7.8	—	mA
RX Mode Current	I_{RXH}	High Performance Mode (measured at 915 MHz and 40 kbps data rate)	—	13.7	22	mA
	I_{RXL}	Low Power Mode (measured at 315 MHz and 40 kbps data rate)	—	10.9	—	mA
TX Mode Current (Si4463)	I_{TX_+20}	+20 dBm output power, Class-E match, 915 MHz, 3.3 V	—	88	108	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	68.5	80	mA
		+13 dBm output power, Class-E match, 915 MHz, 3.3 V	—	44.5	60	mA
TX Mode Current (Si4460)	I_{TX_+10}	+10 dBm output power, Class-E match, 915/868 MHz, 3.3 V[2]	—	19.7	—	mA
	I_{TX_+10}	+10 dBm output power, Class-E match, 169 MHz, 3.3 V[2]	—	18	—	mA
	I_{TX_+13}	+13 dBm output power, Class-E match, 915/868 MHz, 3.3 V	—	24	—	mA
TX Mode Current (Si4461)	I_{TX_+16}	+16 dBm output power, class-E match, 868 MHz, 3.3 V	—	43	55	mA
	I_{TX_+13}	+13 dBm output power, switched-current match, 868 MHz, 3.3 V	—	33.5	40	mA

Notes:
1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. Measured on direct-tie RF evaluation board.

Table 2. Synthesizer AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Resolution	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	µs
Phase Noise	$L\phi(f_M)$	ΔF = 10 kHz, 169 MHz, High Perf Mode	—	–117	–108	dBc/Hz
		ΔF = 100 kHz, 169 MHz, High Perf Mode	—	–120	–115	dBc/Hz
		ΔF = 1 MHz, 169 MHz, High Perf Mode	—	–138	–135	dBc/Hz
		ΔF = 10 MHz, 169 MHz, High Perf Mode	—	–148	–143	dBc/Hz
		ΔF = 10 kHz, 915 MHz, High Perf Mode	—	–102	–94	dBc/Hz
		ΔF = 100 kHz, 915 MHz, High Perf Mode	—	–105	–97	dBc/Hz
		ΔF = 1 MHz, 915 MHz, High Perf Mode	—	–125	–122	dBc/Hz
		ΔF = 10 MHz, 915 MHz, High Perf Mode	—	–138	–135	dBc/Hz

Note: All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.

Table 3. Receiver AC Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
RX Sensitivity 169 MHz[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)	—	–129	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–110	–108	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–106	–104	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–98	–96	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–89	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–110	–107	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–103	–100	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–97	–93	dBm

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 3. Receiver AC Electrical Characteristics[1,2] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity 915/868 MHz[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)	—	–127	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109	–107	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–104	–102	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–97	–92	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–109	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–88	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–108	–104	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–101	–97	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–96	–91	dBm
RX Channel Bandwidth	BW		1.1	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from –110 dBm to –90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity, 169 MHz[3]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz, channel spacing = 12.5 kHz	—	–69	–59	dB
±1-Ch Offset Selectivity, 450 MHz[3]	$C/I_{1\text{-}CH}$		—	–60	–50	dB
±1-Ch Offset Selectivity, 868 / 915 MHz[3]	$C/I_{1\text{-}CH}$		—	–55	–45	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER = 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps, ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz	—	–79	–68	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	–86	–75	dB

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 3. Receiver AC Electrical Characteristics[1,2] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image Rejection (IF = 468.75 kHz)	Im_{REJ}	No image rejection calibration. Rejection at the image frequency. RF = 460 MHz	30	40	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. RF = 460 MHz	40	55	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 915 MHz	30	45	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. RF = 915 MHz	40	52	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 169 MHz	35	45	—	dB
		With image rejection calibration in Si446x. Rejection at the image frequency. RF = 169 MHz	45	60	—	dB

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 4. Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
(G)FSK Data Rate	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{420}	350–420 MHz	—	600	—	kHz
	Δf_{350}	283–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Resolution	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Output Power Range (Si4463)	P_{TX63}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency	–20	—	+20	dBm
Output Power Range (Si4461)	P_{TX61}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency	–40	—	+16	dBm
Output Power Range (Si4460)	P_{TX60}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency. Efficiency can be traded off for higher Tx output power up to +13 dBm	–20	—	+12.5	dBm

Notes:
1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 4. Transmitter AC Electrical Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Power Variation (Si4463)		At 20 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	19	20	21	dBm
Output Power Variation (Si4460)		At 10 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	9	10	11	dBm
Output Power Variation (Si4463)		At 20 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	18.5	20	21	dBm
Output Power Variation (Si4460)		At 10 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	9.5	10	10.5	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power using CLE match within 6 dB of max power	—	0.25	0.4	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2.3	3	dB
TX RF Output Level Variation vs. Frequency	ΔP_{RF_FREQ}	Measured across 902–928 MHz	—	0.6	1.7	dB
Transmit Modulation Filtering	BT	Gaussian Filtering Bandwith Time Product	—	0.5	—	

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 5. Auxiliary Block Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Sensor Sensitivity	TS_S		—	4.5	—	ADC Codes/ °C
Low Battery Detector Resolution	LBD_{RES}		—	50	—	mV
Microcontroller Clock Output Frequency Range[2]	F_{MC}	Configurable to Fxtal or Fxtal divided by 2, 3, 7.5, 10, 15, or 30 where Fxtal is the reference XTAL frequency. In addition, 32.768 kHz is also supported.	32.768K	—	Fxtal	Hz
Temperature Sensor Conversion	$TEMP_{CT}$	Programmable setting	—	3	—	ms
XTAL Range[3]	$XTAL_{Range}$		25	—	32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Start-up time will vary with XTAL type and board layout.	—	300	—	µs
30 MHz XTAL Cap Resolution	$30M_{RES}$		—	70	—	fF
32 kHz XTAL Start-Up Time	t_{32k}		—	2	—	sec
32 kHz Accuracy using Internal RC Oscillator	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	—	6	ms

Notes:
1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –45 to +85 °C unless otherwise stated. All typical values apply at Vdd=3.3V and 25C unless otherwise stated.
2. Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested by bench characterization.
3. XTAL Range tested in production using an external clock source (similar to using a TCXO).

Table 6. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ, SDN)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time[2,3]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2.3	—	ns
Fall Time[3,4]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–1	—	1	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	4	µA
Drive Strength for Output Low Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	1.13	—	mA
Drive Strength for Output High Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.96	—	mA
Drive Strength for Output High Level for GPIO0	I_{OmaxLL}	DRV[1:0] = LL[3]	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	1.70	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD} x 0.2	V

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. 6.7 ns is typical for GPIO0 rise time.
3. Assuming VDD = 3.3 V, drive strength is specified at Voh (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.
4. 2.4 ns is typical for GPIO0 fall time.

Table 7. Thermal Characteristics

Parameter	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Thermal Impedance Junction to Ambient*	θ_{JA}	25	°C/w
Junction Temperature Maximum Value*	T_j	+105	°C
Storage Temperature Range	T_{STG}	–55 to +150	°C
***Note:** θ_{JA} and T_j are based on RF evaluation board measurements.			

Table 8. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.8	V
Instantaneous $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +8.0	V
Sustained $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +6.5	V
Voltage on Analog Inputs	–0.7, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.		

2. Functional Description

The Si446x devices are high-performance, low-current, wireless ISM transceivers that cover the sub-GHz bands. The wide operating voltage range of 1.8–3.8 V and low current consumption make the Si446x an ideal solution for battery powered applications. The Si446x operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2/4-level FSK/GFSK or OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 100 bps to 1 Mbps. The Si4463/61/60 operate in the frequency bands of 142–175, 283–350, 350–525, and 850–1050 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The Si4463 contains a power amplifier (PA) that supports output power up to +20 dBm with very high efficiency, consuming only 70 mA at 169 MHz and 85 mA at 915 MHz. The integrated +20 dBm power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. Competing solutions require large and expensive external PAs to achieve comparable performance. The Si4461 supplies output power up to +16 dBm. The Si4460 is designed to support single coin cell operation with current consumption below 18 mA for +10 dBm output power. Two match topologies are available for the Si4461 and Si4460, class-E and switched-current. Class-E matching provides optimal current consumption, while switched-current matching demonstrates the best performance over varying battery voltage and temperature with slightly higher current consumption. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The Si446x family supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. Antenna diversity is completely integrated into the Si446x and can improve the system link budget by 8–10 dB, resulting in substantial range increases under adverse environmental conditions. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure. Additional system features, such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, and preamble detection, reduce overall current consumption and allows for the use of lower-cost system MCUs. An integrated temperature sensor, power-on-reset (POR), and GPIOs further reduce overall system cost and size. The Si446x is designed to work with an MCU, crystal, and a few passive components to create a very low-cost system.

The application shown in Figure 1 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most applications with output power less than 17 dBm will use this configuration. Figure 2 demonstrates an application for +20 dBm using an external T/R-switch.

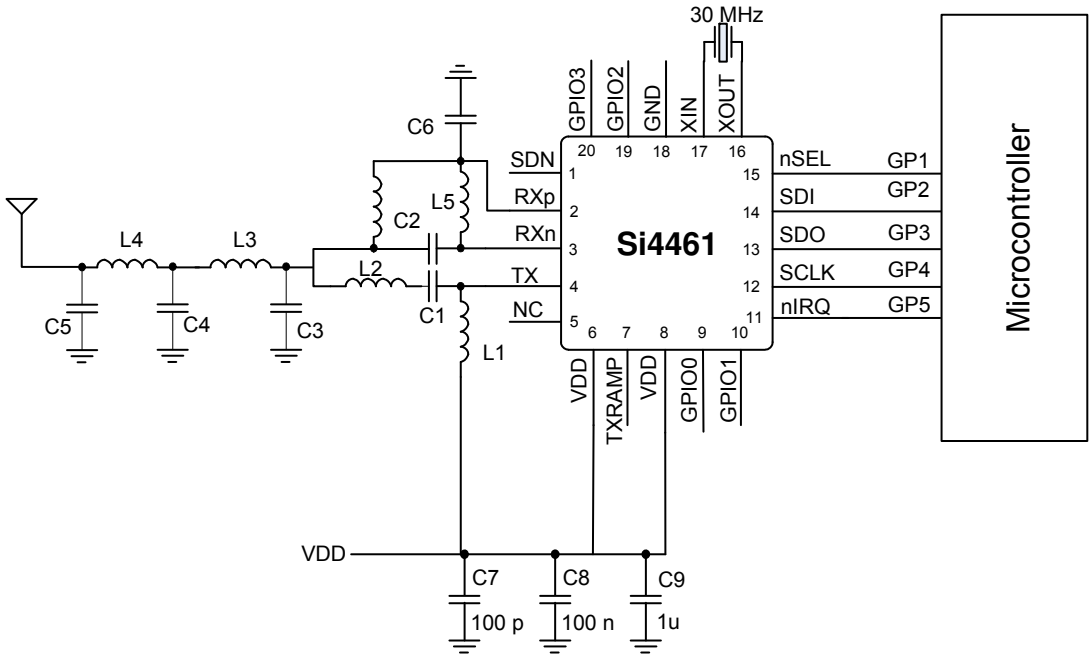


Figure 1. Si4461 Direct-Tie Application Example

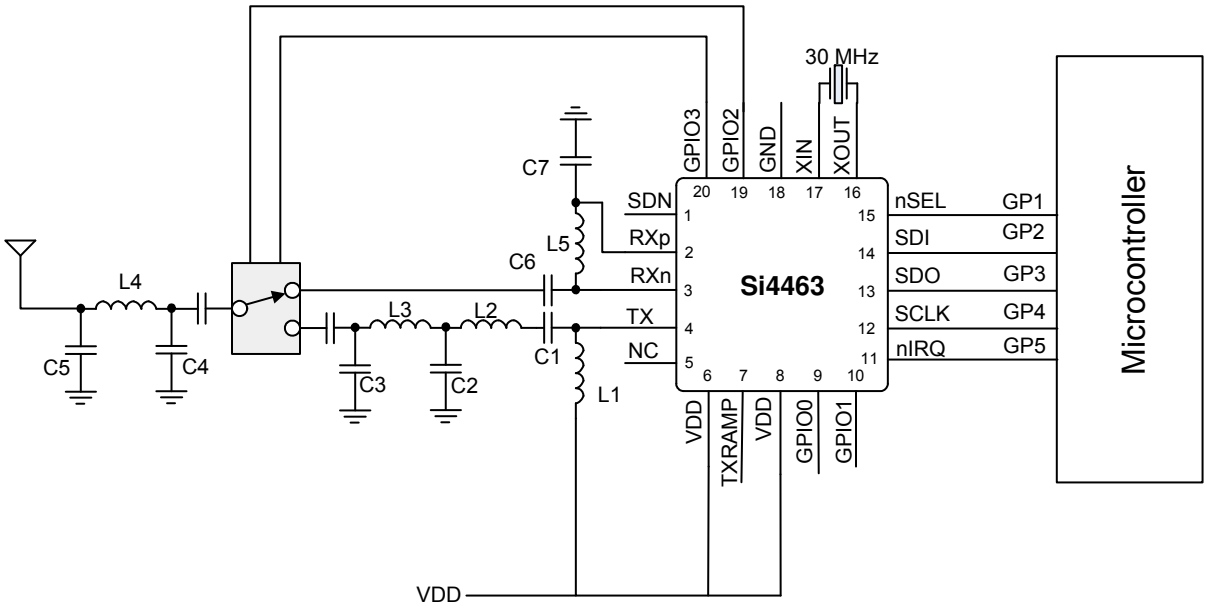


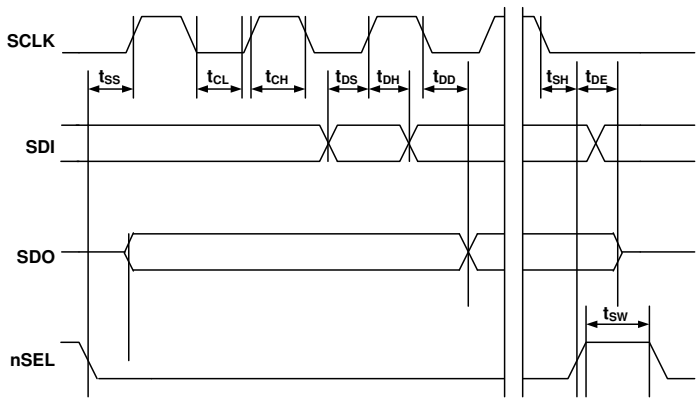
Figure 2. Si4463 Single Antenna with RF Switch Example

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si446x communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are demonstrated in Table 9. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 3 demonstrates an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the firmware commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Max (ns)	Diagram
t_{CH}	Clock high time	40		
t_{CL}	Clock low time	40		
t_{DS}	Data setup time	20		
t_{DH}	Data hold time	20		
t_{DD}	Output data delay time		43	
t_{DE}	Output disable time		45	
t_{SS}	Select setup time	20		
t_{SH}	Select hold time	50		
t_{SW}	Select high period	80		

***Note:** CL = 10 pF; VDD = 1.8 V; SDO Drive strength setting = 10.

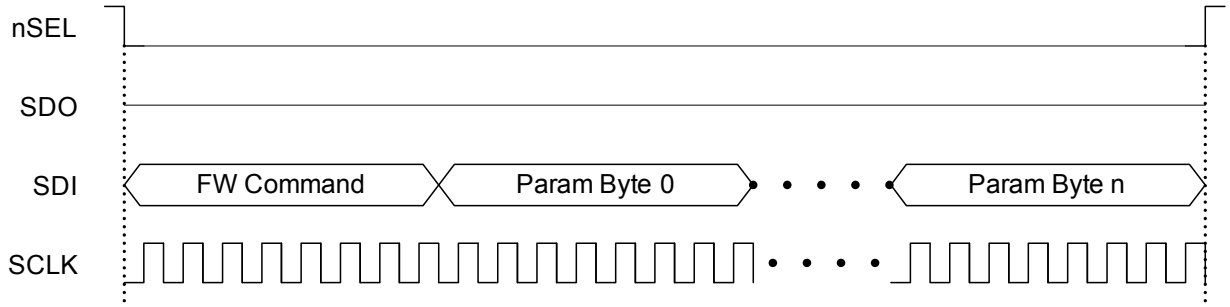
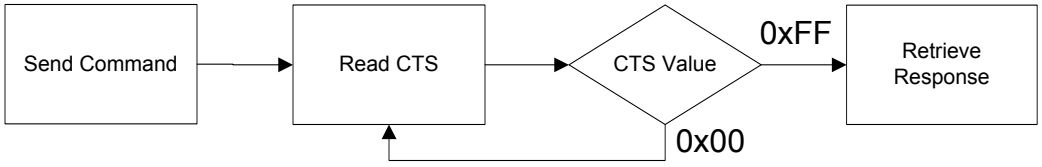


Figure 3. SPI Write Command

The Si446x contains an internal MCU which controls all the internal functions of the radio. For SPI read commands a typical MCU flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 4 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 5 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

Firmware Flow



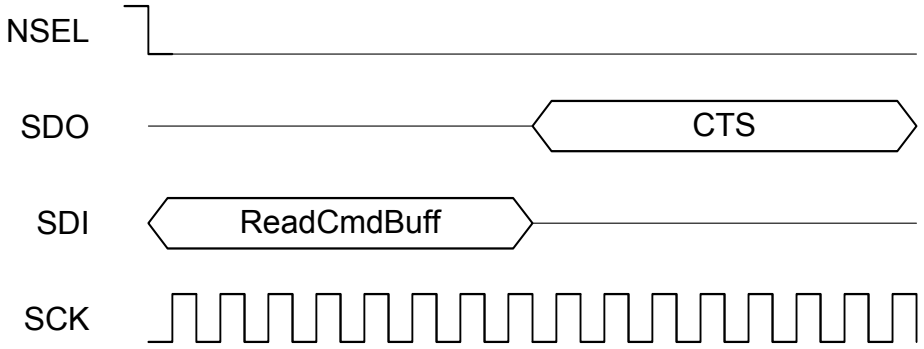


Figure 4. SPI Read Command—Check CTS Value

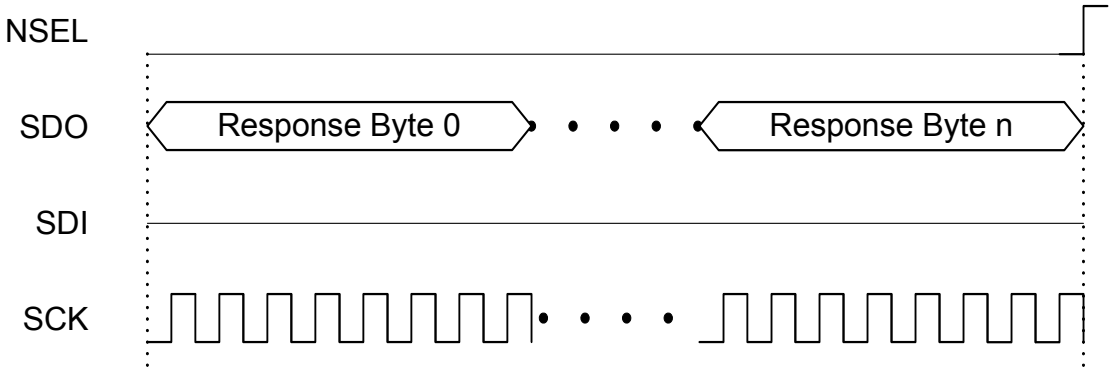


Figure 5. SPI Read Command—Clock Out Read Data

3.2. Fast Response Registers

The fast response registers are registers that can be read immediately without the requirement to monitor and check CTS. There are four fast response registers that can be programmed for a specific function. The fast response registers can be read through API commands, 0x50 for Fast Response A, 0x51 for Fast Response B, 0x53 for Fast Response C, and 0x57 for Fast Response D. The fast response registers can be configured by the "FRR_CTL_X_MODE" properties.

The fast response registers may be read in a burst fashion. After the initial 16 clock cycles, each additional eight clock cycles will clock out the contents of the next fast response register in a circular fashion. The value of the FRRs will not be updated unless NSEL is toggled.

3.3. Operating Modes and Timing

The primary states of the Si446x are shown in Figure 6. The shutdown state completely shuts down the radio to minimize current consumption. Standby/Sleep, SPI Active, Ready, TX Tune, and RX tune are available to optimize the current consumption and response time to RX/TX for a given application. API commands START_RX, START_TX, and CHANGE_STATE control the operating state with the exception of shutdown which is controlled by SDN, pin 1. Table 10 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode. The times in Table 9 are measured from the rising edge of nSEL until the chip is in the desired state. Note that these times are indicative of state transition timing but are not guaranteed and should only be used as a reference data point. An automatic sequencer will put the chip into RX or TX from any state. It is not necessary to manually step through the states. To simplify the diagram it is not shown but any of the lower power states can be returned to automatically after RX or TX.

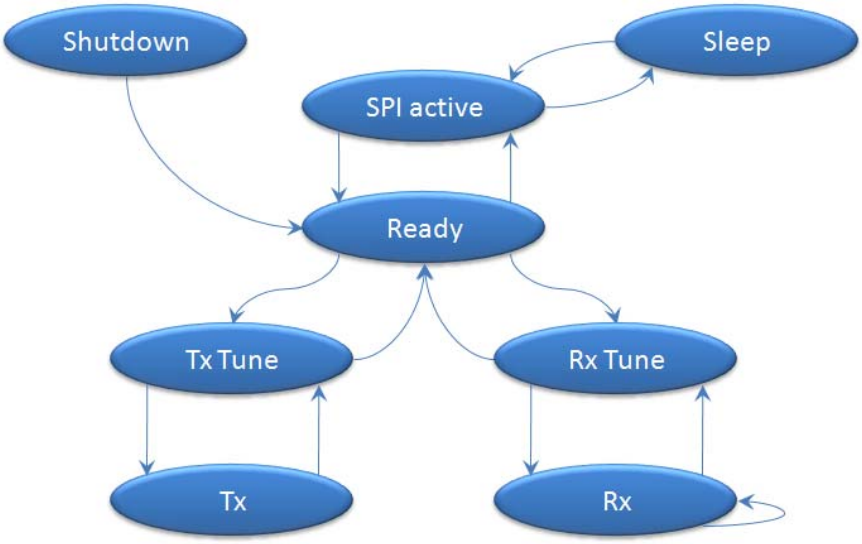


Figure 6. State Machine Diagram

Table 10. Operating State Response Time and Current Consumption

State/Mode	Response Time to		Current in State /Mode
	TX	RX	
Shutdown State	15 ms	15 ms	30 nA
Standby State	440 µs	440 µs	40 nA
Sleep State	440 µs	440 µs	740 nA
SPI Active State	340 µs	340 µs	1.35 mA
Ready State	100 µs	100 µs	1.8 mA
TX Tune State	58 µs	—	7.8 mA
RX Tune State	—	60 µs	7.6 mA
TX State	—	100 µs	18 mA @ +10 dBm
RX State	100 µs	75 µs	10.9 or 13.7 mA
Note: TX→RX and RX→TX state transition timing can be reduced to 70 µs if using Zero-IF mode.			

Figure 7 shows the POR timing and voltage requirements. The power consumption (battery life) depends on the duty cycle of the application or how often the part is in either Rx or Tx state. In most applications the utilization of the standby state will be most advantageous for battery life but for very low duty cycle applications shutdown will have an advantage. For the fastest timing the next state can be selected in the START_RX or START_TX API commands to minimize SPI transactions and internal MCU processing.

3.3.1. Power on Reset (POR)

A Power On Reset (POR) sequence is used to boot the device up from a fully off or shutdown state. To execute this process, VDD must ramp within 1ms and must remain applied to the device for at least 10 ms. If VDD is removed, then it must stay below 0.15 V for at least 10 ms before being applied again. See Figure 7 and Table 11 for details.

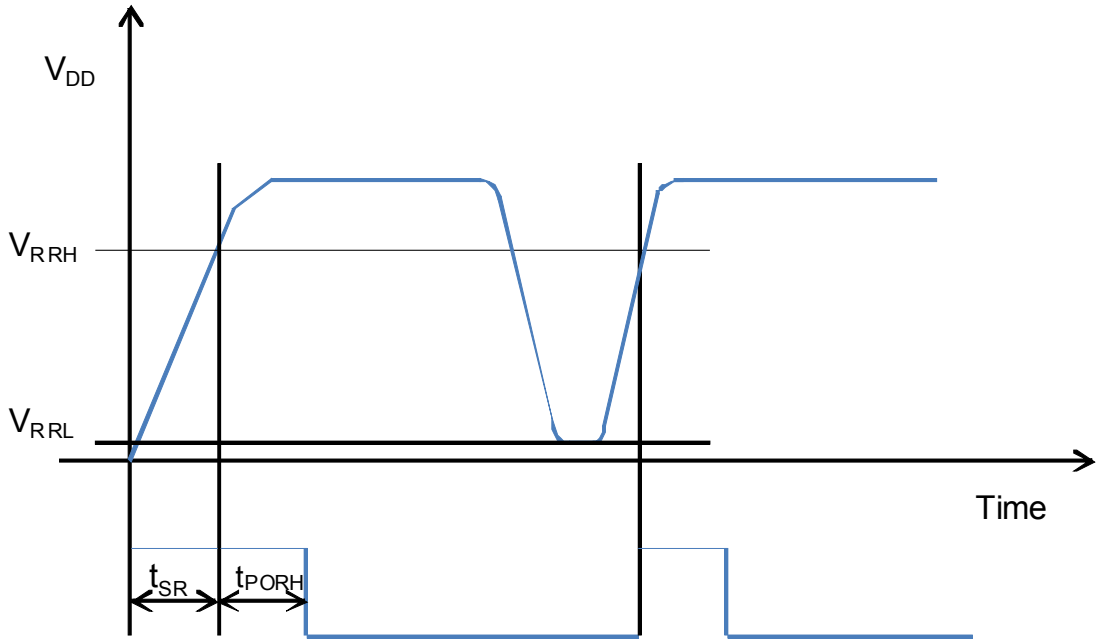


Figure 7. POR Timing Diagram

Table 11. POR Timing

Variable	Description	Min	Typ	Max	Units
t_{PORH}	High time for VDD to fully settle POR circuit	10			ms
t_{PORL}	Low time for VDD to enable POR	10			ms
V_{RRH}	Voltage for successful POR	90% x Vdd			V
V_{RRL}	Starting Voltage for successful POR	0		150	mV
t_{SR}	Slew rate of VDD for successful POR			1	ms

3.3.2. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 30 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 1) high. The SDN pin should be held low in all states except the shutdown state. In the shutdown state, the contents of the registers are lost and there is no SPI access. When coming out of the shutdown state a power on reset (POR) will be initiated along with the internal calibrations. After the POR the POWER_UP command is required to initialize the radio. The SDN pin needs to be held high for at least 10us before driving low again so that internal capacitors can discharge. Not holding the SDN high for this period of time may cause the POR to be missed and the device to boot up incorrectly. If POR timing and voltage requirements cannot be met, it is highly recommended that SDN be controlled using the host processor rather than tying it to GND on the board.

3.3.3. Standby State

Standby state has the lowest current consumption with the exception of shutdown but has much faster response time to RX or TX mode. In most cases standby should be used as the low power state. In this state the register values are maintained with all other blocks disabled. The SPI is accessible during this mode but any SPI event, including FIFO R/W, will enable an internal boot oscillator and automatically move the part to SPI active state. After an SPI event the host will need to re-command the device back to standby through the “Change State” API command to achieve the 40 nA current consumption. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.4. Sleep State

Sleep state is the same as standby state but the wake-up-timer and a 32 kHz clock source are enabled. The source of the 32 kHz clock can either be an internal 32 kHz RC oscillator which is periodically calibrated or a 32 kHz oscillator using an external XTAL.The SPI is accessible during this mode but an SPI event will enable an internal boot oscillator and automatically move the part to SPI active mode. After an SPI event the host will need to re-command the device back to sleep. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.5. SPI Active State

In SPI active state the SPI and a boot up oscillator are enabled. After SPI transactions during either standby or sleep the device will not automatically return to these states. A “Change State” API command will be required to return to either the standby or sleep modes.

3.3.6. Ready State

Ready state is designed to give a fast transition time to TX or RX state with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time.

3.3.7. TX State

The TX state may be entered from any of the state with the “Start TX” or “Change State” API commands. A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The following sequence of events will occur automatically when going from standby to TX state.

1. Enable internal LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).

3. Enable PLL.
4. Calibrate VCO/PLL.
5. Wait until PLL settles to required transmit frequency (controlled by an internal timer).
6. Activate power amplifier and wait until power ramping is completed (controlled by an internal timer).
7. Transmit packet.

Steps in this sequence may be eliminated depending on which state the chip is configured to prior to commanding to TX. By default, the VCO and PLL are calibrated every time the PLL is enabled. When the START_TX API command is utilized the next state may be defined to ensure optimal timing and turnaround.

Figure 8 shows an example of the commands and timing for the START_TX command. CTS will go high as soon as the sequencer puts the part into TX state. As the sequencer is stepping through the events listed above, CTS will be low and no new commands or property changes are allowed. If the Fast Response (FRR) or nIRQ is used to monitor the current state there will be slight delay caused by the internal hardware from when the event actually occurs to when the transition occurs on the FRR or nIRQ. The time from entering TX state to when the FRR will update is 5 µs and the time to when the nIRQ will transition is 13 µs. If a GPIO is programmed for TX state or used as control for a transmit/receive switch (TR switch) there is no delay.

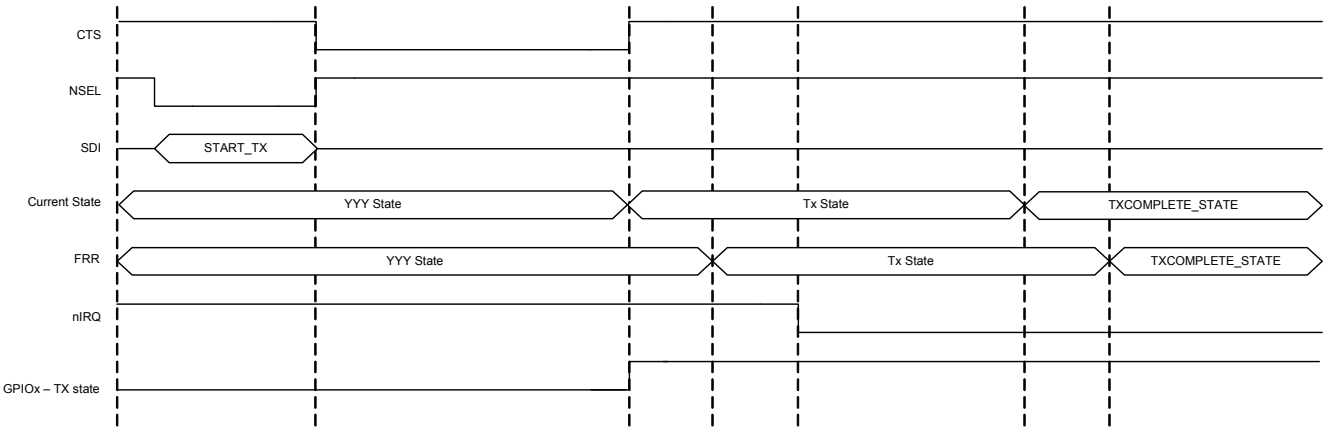


Figure 8. Start_TX Commands and Timing

3.3.8. RX State

The RX state may be entered from any of the other states by using the “Start RX” or “Change State” API command. A built-in sequencer takes care of all the actions required to transition between states. The following sequence of events will occur automatically to get the chip into RX mode when going from standby to RX state:

1. Enable the digital LDO and the analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO
5. Wait until PLL settles to required receive frequency (controlled by an internal timer).
6. Enable receiver circuits: LNA, mixers, and ADC.
7. Enable receive mode in the digital modem.

Depending on the configuration of the radio, all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC. Similar to the TX state, the next state after RX may be defined in the “Start RX” API command. The START_RX commands and timing will be equivalent to the timing shown in Figure 8.

3.4. Application Programming Interface (API)

An application programming interface (API), which the host MCU will communicate with, is embedded inside the device. The API is divided into two sections, commands and properties. The commands are used to control the chip and retrieve its status. The properties are general configurations which will change infrequently. The API descriptions can be found on the Silicon Labs website.

3.5. Interrupts

The Si446x is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Registers. The nIRQ output signal will then be reset until the next change in status is detected.

The interrupts sources are grouped into three groups: packet handler, chip status, and modem. The individual interrupts in these groups can be enabled/disabled in the interrupt property registers. An interrupt must be enabled for it to trigger an event on the nIRQ pin. The interrupt group must be enabled as well as the individual interrupts in API properties described in the API documentation.

Once an interrupt event occurs and the nIRQ pin is low there are two ways to read and clear the interrupts. All of the interrupts may be read and cleared in the “GET_INT_STATUS” API command. By default all interrupts will be cleared once read. If only specific interrupts want to be read in the fastest possible method the individual interrupt groups (Packet Handler, Chip Status, Modem) may be read and cleared by the “GET_MODEM_STATUS”, “GET_PH_STATUS” (packet handler), and “GET_CHIP_STATUS” API commands.

The instantaneous status of a specific function maybe read if the specific interrupt is enabled or disabled. The status results are provided after the interrupts and can be read with the same commands as the interrupts. The status bits will give the current state of the function whether the interrupt is enabled or not.

The fast response registers can also give information about the interrupt groups but reading the fast response registers will not clear the interrupt and reset the nIRQ pin.

3.6. GPIO

Four general purpose IO pins are available to utilize in the application. The GPIO are configured by the GPIO_PIN_CFG command in address 13h. For a complete list of the GPIO options please see the API guide. GPIO pins 0 and 1 should be used for active signals such as data or clock. GPIO pins 2 and 3 have more susceptibility to generating spurious in the synthesizer than pins 0 and 1. The drive strength of the GPIOs can be adjusted with the GEN_CONFIG parameter in the GPIO_PIN_CFG command. By default the drive strength is set to minimum. The default configuration for the GPIOs and the state during SDN is shown below in Table 12.The state of the IO during shutdown is also shown inTable 12. As indicated previously in Table 6, GPIO 0 has lower drive strength than the other GPIOs.

Table 12. GPIOs

Pin	SDN State	POR Default
GPIO0	0	POR
GPIO1	0	CTS
GPIO2	0	POR
GPIO3	0	POR
nIRQ	resistive VDD pull-up	nIRQ
SDO	resistive VDD pull-up	SDO
SDI	High Z	SDI
SCLK	High Z	SCLK
NSEL	High Z	NSEL

4. Modulation and Hardware Configuration Options

The Si446x supports different modulation options and can be used in various configurations to tailor the device to any specific application or legacy system for drop in replacement. The modulation and configuration options are set in API property, MODEM_MOD_TYPE. Refer to the API documentation for details on modem related properties.

4.1. Modulation Types

The Si446x supports five different modulation options: Gaussian frequency shift keying (GFSK), frequency-shift keying (FSK), four-level GFSK (4GFSK), four-level FSK (4FSK), and on-off keying (OOK). Minimum shift keying (MSK) can also be created by using GFSK with the appropriate modulation index (h = 0.5). GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. The modulation type is set by the “MOD_TYPE[2:0]” field in the “MODEM_MOD_TYPE” API property. A continuous-wave (CW) carrier may also be selected for RF evaluation purposes. The modulation source may also be selected to be a pseudo-random source for evaluation purposes.

4.2. Hardware Configuration Options

There are different receive demodulator options to optimize the performance and mutually-exclusive options for how the RX/TX data is transferred from the host MCU to the RF device.

4.2.1. Receive Demodulator Options

There are multiple demodulators integrated into the device to optimize the performance for different applications, modulation formats, and packet structures. The calculator built into WDS will choose the optimal demodulator based on the input criteria.

4.2.1.1. Synchronous Demodulator

The synchronous demodulator's internal frequency error estimator acquires the frequency error based on a 101010 preamble structure. The bit clock recovery circuit locks to the incoming data stream within four transactions of a “10” or “01” bit stream. The synchronous demodulator gives optimal performance for 2- or 4-level (G)FSK modulation that has a modulation index less than 2.

4.2.1.2. Asynchronous Demodulator

The asynchronous demodulator should be used for OOK modulation and for (G)FSK modulation under one or more of the following conditions:

- Modulation index $\geq$ 2
- Non-standard preamble (not 1010101... pattern)

When the modulation index exceeds 2, the asynchronous demodulator has better sensitivity compared to the synchronous demodulator. An internal deglitch circuit provides a glitch-free data output and a data clock signal to simplify the interface to the host. There is no requirement to perform deglitching in the host MCU. The asynchronous demodulator will typically be utilized for legacy systems and will have many performance benefits over devices used in legacy designs. Unlike the Si4432/31 solution for non-standard packet structures, there is no requirement to perform deglitching on the data in the host MCU. Glitch-free data is output from Si446x devices, and a sample clock for the asynchronous data can also be supplied to the host MCU; so, oversampling or bit clock recovery is not required by the host MCU. There are multiple detector options in the asynchronous demodulator block, which will be selected based upon the options entered into the WDS calculator. The asynchronous demodulator's internal frequency error estimator is able to acquire the frequency error based on any preamble structure.

4.2.2. RX/TX Data Interface With MCU

There are two different options for transferring the data from the RF device to the host MCU. FIFO mode uses the SPI interface to transfer the data, while direct mode transfers the data in real time over a GPIO pin.

4.2.2.1. FIFO Mode

In FIFO mode, the transmit and receive data is stored in integrated FIFO register memory. The TX FIFO is accessed by writing command 66h followed directly by the data/clk that the host wants to write into the TX FIFO. The RX FIFO is accessed by writing command 77h followed by the number of clock cycles of data the host would like to read out of the RX FIFO. The RX data will be clocked out onto the SDO pin.

In TX FIFO mode, the data bytes stored in FIFO memory are “packaged” together with other fields and bytes of information to construct the final transmit packet structure. These other potential fields include the Preamble, Sync word, and CRC checksum. In TX mode, the packet structure may be highly customized by enabling or disabling individual fields; for example, it is possible to disable both the Preamble and Sync Word fields and to load the entire packet structure into FIFO memory. For further information on the configuration of the FIFOs for a specific application or packet size, see "6. Data Handling and Packet Handler" on page 38. In RX mode, the Packet Handler must be enabled to allow storage of received data bytes into RX FIFO memory. The Packet Handler is required to detect the Sync Word, and proper detection of the Sync Word is required to determine the start of the Payload. All bytes after the Sync Word are stored in RX FIFO memory except the CRC checksum and (optionally) the variable packet length byte(s). When the FIFO is being used in RX mode, all of the received data may still be observed directly (in realtime) by properly programming a GPIO pin as the RXDATA output pin; this can be quite useful during application development. When in FIFO mode, the chip will automatically exit the TX or RX State when either the PACKET_SENT or PACKET_RX interrupt occurs. The chip will return to the state programmed in the argument of the “START TX” or “START RX” API command, TXCOMPLETE_STATE[3:0] or RXVALID_STATE[3:0]. For example, the chip may be placed into READY mode after a TX packet by sending the “START TX” command and by writing 30h to the TXCOMPLETE_STATE[3:0] argument. The chip will transmit all of the contents of the FIFO, and the PACKET_SENT interrupt will occur. When this event occurs, the chip will return to the READY state as defined by TXCOMPLETE_STATE[3:0] = 30h.

4.2.2.2. FIFO Direct Mode (Infinite Receive)

In some applications, there is a need to receive extremely long packets (greater than 40 kB) while relying on preamble and sync word detection from the on-chip packet handler. In these cases, the packet length is unknown, and the device will load the bits after the sync word into the RX FIFO forever. Other features, such as Data Whitening, CRC, Manchester, etc., are supported in this mode, but CRC calculation is not because the end of packet is unknown to the device. The RX data and clock are also available on GPIO pins. The host MCU will need to reset the packet handler by issuing a START_RX to begin searching for a new packet.

4.2.2.3. Automatic TX Packet Repeat

In TX mode, there is an option to send the FIFO contents repeatedly with a user-defined number of times to repeat. This is limited to the FIFO size, and the entire contents of the packet including preamble and sync word need to be loaded into the TX FIFO. This is selectable via the START_TX API, and packets will be sent without any gaps between them.

4.2.2.4. Direct Mode

For legacy systems that perform packet handling within the host MCU or other baseband chip, it may not be desirable to use the FIFO. For this scenario, a Direct mode is provided, which bypasses the FIFOs entirely. In TX Direct mode, the TX modulation data is applied to an input pin of the chip and processed in “real time” (i.e., not stored in a register for transmission at a later time). Any of the GPIOs may be configured for use as the TX Data input function. Furthermore, an additional pin may be required for a TX Clock output function if GFSK modulation is desired (only the TX Data input pin is required for FSK or OOK). To achieve direct mode, the desired GPIO pin must be configured as a digital input by setting the GPIO_PIN_CFG API command = enumeration 0x04 in addition to setting the MODEM_MOD_TYPE API property to source the TXDATA stream from that same GPIO pin. For GFSK, “TX_DIRECT_MODE_TYPE” must be set to synchronous. For 2FSK or OOK, the type can be set to asynchronous or synchronous. The MOD_SOURCE[1:0] field within the MODEM_MOD_TYPE property should be set = 0x01h for all Direct mode configurations. In RX Direct mode, the RX Data and RX Clock can be programmed for direct (real-time) output to GPIO pins. The microcontroller may then process the RX data without using the FIFO or packet handler functions of the RFIC.