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Si4703-B17

BROADCAST FM RADIO TUNER FOR PORTABLE APPLICATIONS

Features

- This data sheet applies to Si4703 Firmware 17 and greater
- Worldwide FM band support (76–108 MHz)
- Digital low-IF receiver
- Frequency synthesizer with integrated VCO
- Seek tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Excellent overload immunity
- Signal strength measurement
- Programmable de-emphasis (50/75 µs)
- Adaptive noise suppression
- Volume control
- Line-level analog output
- 32.768 kHz reference clock
- 2-wire and 3-wire control interface
- 2.7 to 5.5 V supply voltage
- Integrated LDO regulator allows direct connection to battery
- 3 x 3 mm 20-pin QFN package
  - Pb-free/RoHS compliant
- RDS/RBDS Processor
- Integrated crystal oscillator

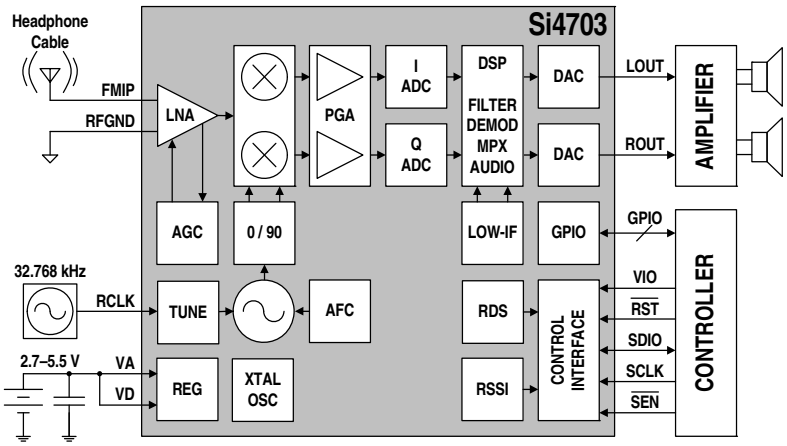
Applications

- Cellular handsets
- MP3 players
- Portable radios
- USB FM radio
- PDAs
- Notebook PCs
- Portable navigation
- Automotive
- Consumer electronics

Description

The Si4703 integrates the complete tuner function from antenna input to stereo audio output for FM broadcast radio reception.

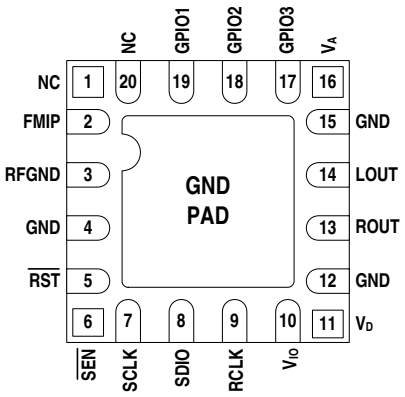
Functional Block Diagram



Ordering Information:
See page 35.

Pin Assignments (Top View)

Si4703-GM



Patents pending

Notes:

1. To ensure proper operation and FM receiver performance, follow the guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place Si4703 as close as possible to antenna jack and keep the FMIP trace as short as possible.

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	V_D		2.7	—	5.5	V
Analog Supply Voltage	V_A		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Digital Power Supply Power-Up Rise Time	V_{DRISE}		25	—	—	µs
Analog Power Supply Power-Up Rise Time	V_{ARISE}		25	—	—	µs
Interface Power Supply Power-Up Rise Time	V_{IORISE}		25	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_D = V_A = 3.3$ V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Digital Supply Voltage	V_D	–0.5 to 5.8	V
Analog Supply Voltage	V_A	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4703 device is a high-performance RF integrated circuit with an ESD rating of < 2 kV HBM. Handling and assembly of this device should only be done at ESD-protected workstations.
3. For input pins SCLK, $\overline{SEN}$, SDIO, $\overline{RST}$, RCLK, GPIO1, GPIO2, and GPIO3.
4. At RF input pins.

Table 3. DC Characteristics

(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Current[1]	I_A	ENABLE = 1	—	13.4	15.3	mA
Analog Supply Current[1,2,3,4]	I_A	ENABLE = 1 Low SNR level	—	14.2	15.9	mA
Analog Powerdown Current[1,5,6]	I_{PDA}	ENABLE = 0	—	2.4	5	µA
Digital Supply Current[1]	I_D	ENABLE = 1	—	5.3	8.5	mA
Digital Supply Current[1,2,3,4]	I_D	ENABLE = 1 Low SNR level	—	5.0	8.0	mA
Digital Powerdown Current[1,5,6]	I_{PDD}	ENABLE = 0	—	2.1	5	µA
Interface Supply Current[1]	I_{IO}	ENABLE = 1	—	400	650	µA
Interface Powerdown Current[1,5,6,7]	I_{IO}	SCLK, RCLK inactive ENABLE = 0	—	0.5	5	µA
High Level Input Voltage[8]	V_{IH}		0.7 x V_{IO}	—	V_{IO} + 0.3	V
Low Level Input Voltage[8]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[8]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[8]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[9]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[9]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:

1. Refer to Register 02h, "Power Configuration" on page 21 for ENABLE bit description.
2. The LNA is automatically switched to higher current mode for optimum sensitivity in low SNR conditions.
3. Analog and digital supply currents are simultaneously adjusted based on SNR level.
4. Stereo and RDS functionality are disabled at low SNR levels.
5. Specifications are guaranteed by characterization.
6. Refer to Section 4.9. "Reset, Powerup, and Powerdown" on page 17.
7. All GPIO pins are grounded.
8. For input pins SCLK, SEN, SDIO, RST, RCLK, GPIO1, GPIO2, and GPIO3.
9. For output pins SDIO, GPIO1, GPIO2, and GPIO3.

Table 4. Reset Timing Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
$\overline{RST}$↓, GPIO3 Input to $\overline{RST}$↑ Setup	t_{SRST}	Busmode Select Method 1*	100	—	—	µs
$\overline{SEN}$, SDIO Input to $\overline{RST}$↑ Setup	t_{SRST}		30	—	—	ns
$\overline{SEN}$, SDIO, GPIO3 Input to $\overline{RST}$↑ Hold	t_{HRST}		30	—	—	ns
GPIO1, GPIO3 Input to $\overline{RST}$↑ Setup	t_{SRST}	Busmode Select Method 2	30	—	—	ns
GPIO1, GPIO3 Input to $\overline{RST}$↑ Hold	t_{HRST}		30	—	—	ns

***Note:** In Busmode Select Method 1, GPIO3 may be left high-Z (minimum pullup 10 MΩ), be left floating, or pulled low to be backwards compatible with Si4700/01 silicon revision A. If GPIO3 is pulled low then the minimum t_{SRST} for $\overline{RST}$↓, GPIO3 input to $\overline{RST}$↑ setup is only 30 nS.

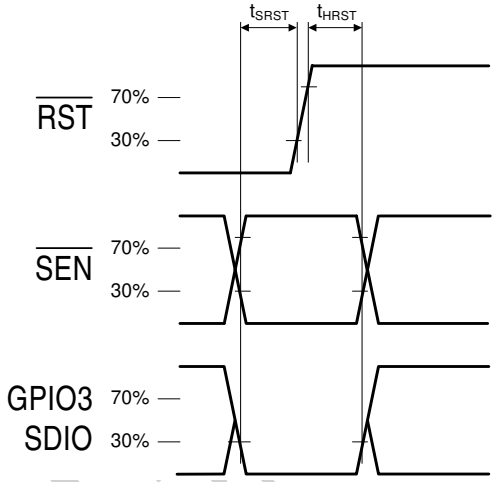


Figure 1. Reset Timing Parameters for Busmode Select Method 1

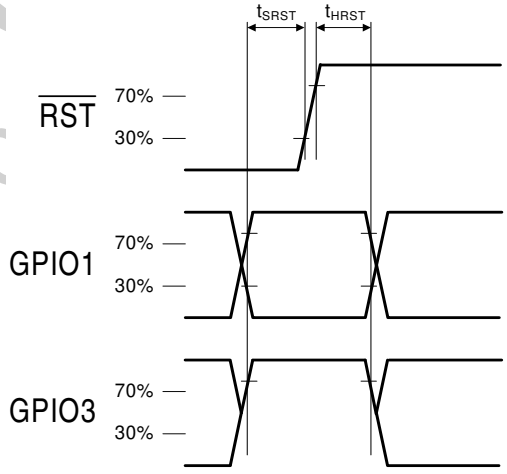


Figure 2. Reset Timing Parameters for Busmode Select Method 2

Table 5. 3-Wire Control Interface Characteristics

(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN1}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↑ Hold	t_{HSEN2}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns

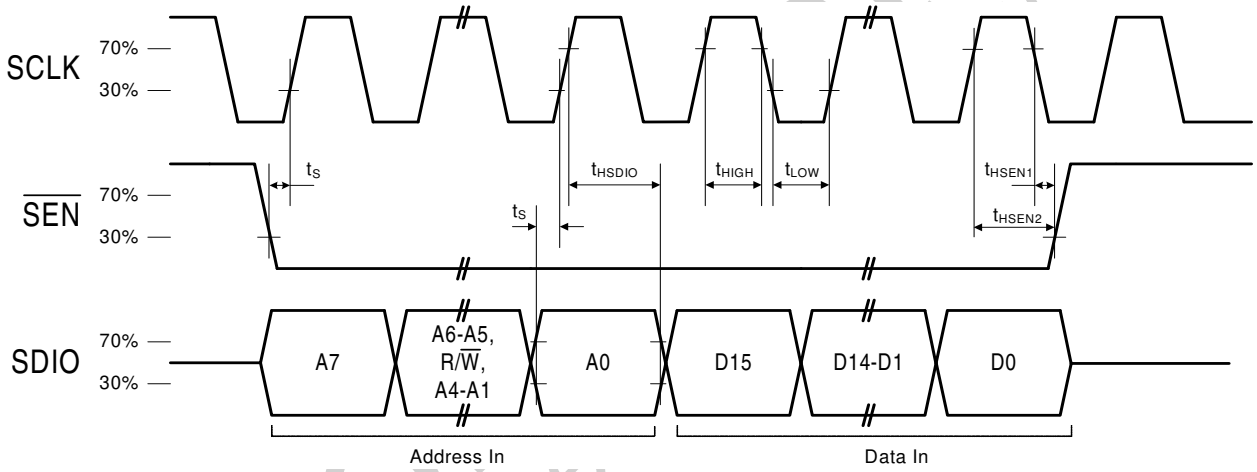


Figure 3. 3-Wire Control Interface Write Timing Parameters

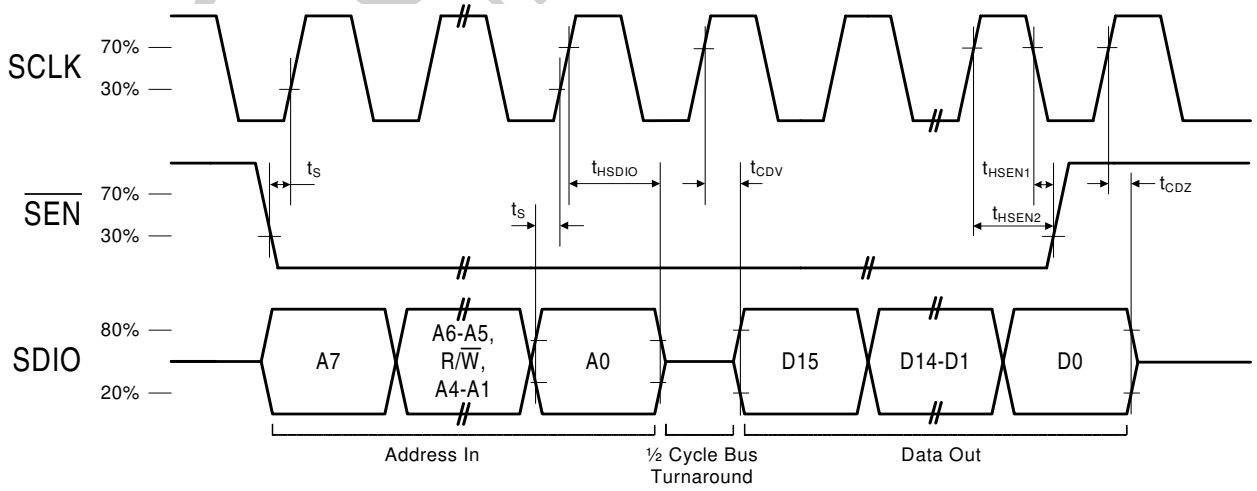


Figure 4. 3-Wire Control Interface Read Timing Parameters

Table 6. 2-Wire Control Interface Characteristics[1]

(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK↓ Hold[2,3]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		20 + 01.C_b	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		20 + 01.C_b	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. As a transmitter, the Si4703 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the 0 ns $t_{HD:DAT}$ specification.
3. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated so long as all other timing parameters are met.

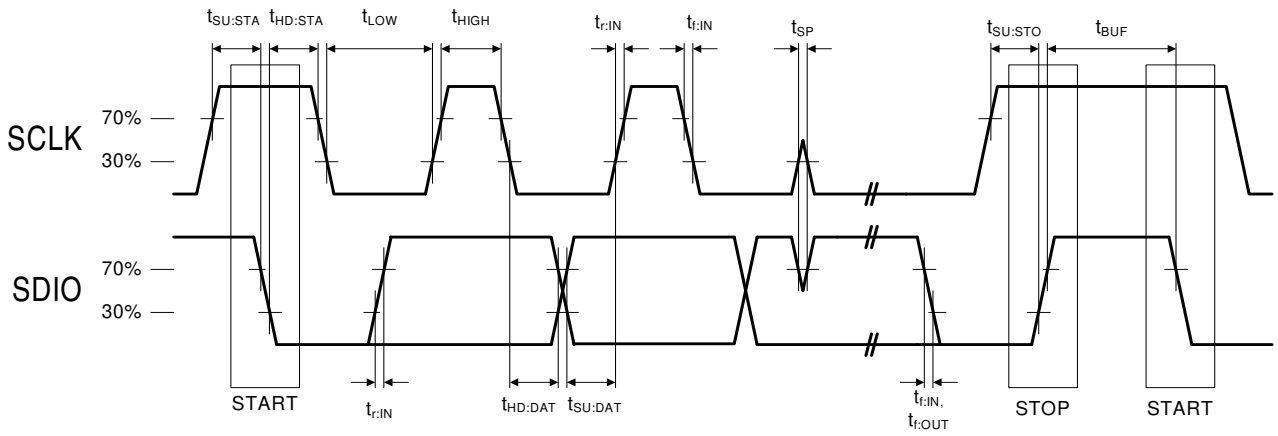


Figure 5. 2-Wire Control Interface Read and Write Timing Parameters

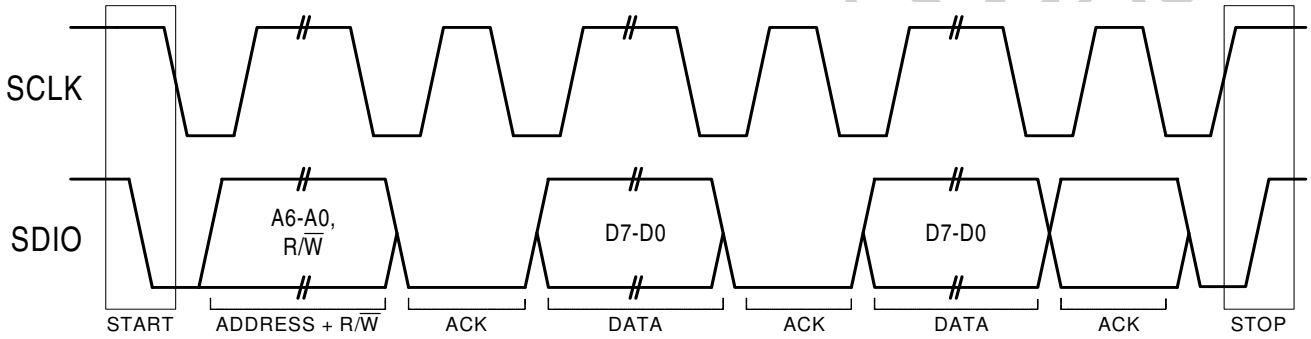


Figure 6. 2-Wire Control Interface Read and Write Timing Diagram

Table 7. FM Receiver Characteristics[1,2]

(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity[3,4,5,6,7]		(S+N)/N = 26 dB	—	2.2	3.5	µVEMF
RDS Sensitivity[8]		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µVEMF
RDS Sensitivity in Performance Mode[8,9]		Δf = 2 kHz, RDS BLER < 5% RDSPRF = 1	—	12	—	µVEMF
LNA Input Resistance[8,10]			3	4	5	kΩ
LNA Input Capacitance[8,10]			4	5	6	pF
Input IP3[8,11]			104	108	—	dBµVEMF
AM Suppression[3,4,5,8,10]		m = 0.3	40	55	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[8]		In-band	35	—	—	dB
RCLK Frequency			—	32.768	—	kHz
RCLK Frequency Tolerance[12]		SPACE[1:0] = 00 or 01	–200	—	200	ppm
		SPACE[1:0] = 10	–50	—	50	
Audio Output Voltage[3,4,5,10]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,4,10,13]			—	—	1	dB
Audio Band Limits[3,4,8,10]		±1.5 dB	30	—	15 k	Hz

Notes:

1. Additional testing information is available in Application Note AN234. Volume = maximum for all tests.
2. **Important Note:** To ensure proper operation and FM receiver performance, follow the guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis
4. MONO = 1, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. Typical sensitivity with matching network.
8. Guaranteed by characterization.
9. RDS high-performance mode enabled RDSPRF 06h[9] = 1. Refer to 6. "Register Descriptions" on page 20.
10. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
11. $|f_2 - f_1| > 1$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled by setting AGCD = 1. Refer to "6. Register Descriptions" on page 20.
12. The channel spacing is selected with the SPACE[1:0] bits. Refer to "6. Register Descriptions" on page 20. Seek/Tune timing is guaranteed for 100 and 200 kHz channel spacing.
13. Δf = 75 kHz.
14. The de-emphasis time constant is selected with the DE bit. Refer to "6. Register Descriptions" on page 20.
15. At LOUT and ROUT pins.
16. Min and Max at room temperature (25 C°).

Table 7. FM Receiver Characteristics[1,2] (Continued)

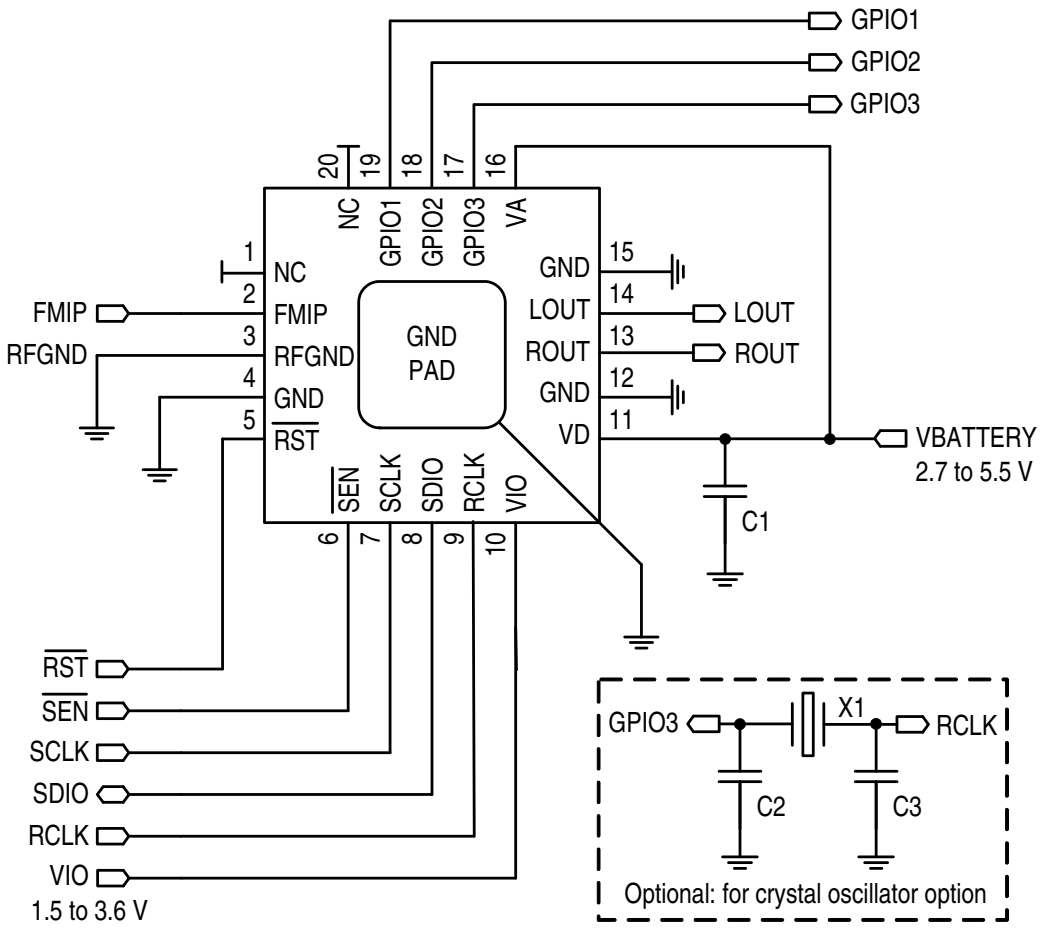
(V_D = V_A = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Stereo Separation[3,10,13]			25	—	—	dB
Mono/Stereo Switching Level[3,13]		BLNDADJ = 10 10 dB stereo separation	—	34	—	dBµVEMF
Audio Mono S/N[3,4,5,6,10]			55	63	—	dB
Audio Stereo S/N[5]		BLNDADJ = 10	—	58	—	dB
Audio THD[3,4,10,13]			—	0.1	0.5	%
De-emphasis Time Constant[14]		DE = 0	70	75	80	µs
		DE = 1	45	50	54	µs
Audio Common Mode Voltage[15]		ENABLE = 1	0.7	0.8	0.9	V
Audio Common Mode Voltage[15]		ENABLE = 0 AHIZEN = 1	—	0.5 x V_{IO}	—	V
Audio Output Load Resistance[8,15]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[8,15]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[8,12]		SPACE[1:0] = 0x, RCLK tolerance = 200 ppm, (x = 0 or 1)	—	—	60	ms/ channel
Powerup Time		From powerdown (Write ENABLE bit to 1)	—	—	110	ms
RSSI Offset[16]		Input levels of 8 and 60 dBµV at RF input	–3	—	3	dB

Notes:

1. Additional testing information is available in Application Note AN234. Volume = maximum for all tests.
2. **Important Note:** To ensure proper operation and FM receiver performance, follow the guidelines in “AN231: Si4700/01/02/03 Headphone and Antenna Interface.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis
4. MONO = 1, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. Typical sensitivity with matching network.
8. Guaranteed by characterization.
9. RDS high-performance mode enabled RDSPRF 06h[9] = 1. Refer to 6. "Register Descriptions" on page 20.
10. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
11. $|f_2 – f_1| > 1$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled by setting AGCD = 1. Refer to "6. Register Descriptions" on page 20.
12. The channel spacing is selected with the SPACE[1:0] bits. Refer to "6. Register Descriptions" on page 20. Seek/Tune timing is guaranteed for 100 and 200 kHz channel spacing.
13. Δf = 75 kHz.
14. The de-emphasis time constant is selected with the DE bit. Refer to "6. Register Descriptions" on page 20.
15. At LOUT and ROUT pins.
16. Min and Max at room temperature (25 C°).

2. Typical Application Schematic



Notes:

1. Place C1 close to V_D pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. **Important Note:** FM Receiver performance is subject to adherence to antenna design guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface." Failure to use these guidelines will negatively affect the performance of the Si4703, particularly in weak signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the antenna interface, refer to "AN231: Si4700/01/02/03 Headphone and Antenna Interface."
6. Place Si4703 as close as possible to antenna jack and keep the FMIP trace as short as possible.
7. Refer to Si4702/03 Internal Crystal Oscillator Errata.
8. Refer to "AN299: External 32.768 kHz Crystal Oscillator."

3. Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
U1	Si4703 FM Radio Tuner	Silicon Laboratories
C2, C3	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson

4. Functional Description

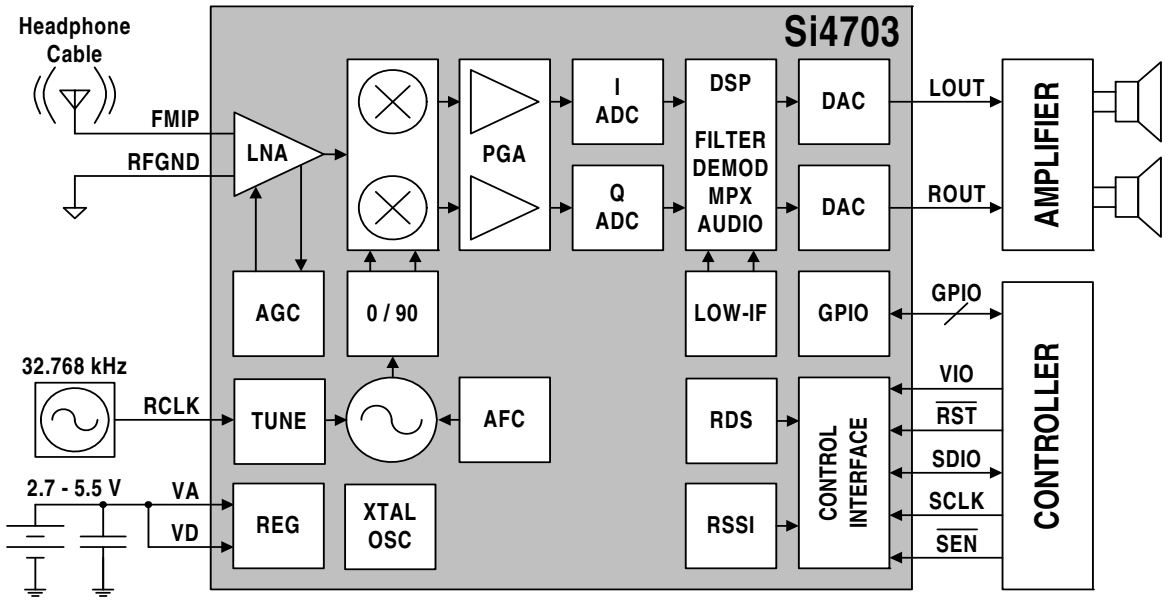


Figure 7. Si4703 FM Receiver Block Diagram

4.1. Overview

The Si4703 extends Silicon Laboratories Si4700 FM tuner family, and further increases the ease and attractiveness of adding FM radio reception to mobile devices through small size and board area, minimum component count, flexible programmability, and superior, proven performance. Si4703 software is backwards compatible to existing Si4701 FM Tuner designs and leverages Silicon Laboratories' highly successful and patented Si4701 FM tuner. The Si4703 benefits from proven digital integration and 100% CMOS process technology, resulting in a completely integrated solution. It is the industry's smallest footprint FM tuner IC requiring only 10 mm^2 board space and one external bypass capacitor.

The device offers significant programmability, and caters to the subjective nature of FM listeners and variable FM broadcast environments world-wide through a simplified programming interface and mature functionality.

The Si4703 incorporates a digital processor for the European Radio Data System (RDS) and the US Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions.

RDS enables data such as station identification and song name to be displayed to the user. The Si4703 offers a detailed RDS view and a standard view, allowing adopters to selectively choose granularity of RDS status, data, and block errors. Si4703 software is backwards compatible to the proven Si4701, adopted by leading cell-phone and MP3 manufacturers world-wide.

The Si4703 is based on the superior, proven performance of Silicon Laboratories' Aero architecture offering unmatched interference rejection and leading sensitivity. The device uses the same programming interface as the Si4701 and supports multiple bus-modes. Power management is also simplified with an integrated regulator allowing direct connection to a 2.7 to 5.5 V battery.

The Si4703 device's high level of integration and complete FM system production testing increases quality to manufacturers, improves device yields, and simplifies device manufacturing and final testing.

4.2. FM Receiver

The Si4703's patented digital low-IF architecture reduces external components and eliminates the need for factory adjustments. The receive (RX) section integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled with the AGCD bit. Refer to Section 6. "Register Descriptions" on page 20 for additional programming and configuration information.

The Si4703 architecture and antenna design increases

system performance. To ensure proper performance and operation, designers should refer to the guidelines in "AN231: Si4700/01/02/03 Headphone and Antenna Interface". Conformance to these guidelines will help to ensure excellent performance even in weak signal or noisy environments.

An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture achieves superior performance by using digital signal processing (DSP) to perform channel selection, FM demodulation, and stereo audio processing compared to traditional analog architectures.

4.3. General Purpose I/O Pins

The pins GPIO1–3 can serve multiple functions. GPIO1 and GPIO3 can be used to select between 2-wire and 3-wire modes for the control interface as the device is brought out of reset. See Section “4.9. Reset, Powerup, and Powerdown”. After powerup of the device, the GPIO1–3 pins can be used as general purpose inputs/outputs, and the GPIO2–3 pins can be used as interrupt request pins for the seek/tune or RDS ready functions and as a stereo/mono indicator respectively. See register 04h, bits [5:0] in Section “6. Register Descriptions” for information on the control of these pins. It is recommended that the GPIO2–3 pins not be used as interrupt request outputs until the powerup time has completed (see Section “4.9. Reset, Powerup, and Powerdown”). The GPIO3 pin has an internal, 1 MΩ, ±15% pull-down resistor that is only active while $\overline{RST}$ is low. General purpose input/output functionality is available regardless of the state of the V_A and V_D supplies, or the ENABLE and DISABLE bits.

4.4. RDS/RBDS Processor and Functionality

The Si4703 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction. RDS functionality is enabled by setting the RDS bit. The device offers two RDS modes, a standard mode and a verbose mode. The primary difference is increased visibility to RDS block-error levels and synchronization status with verbose mode.

Setting the RDS mode (RDSM) bit low places the device in standard RDS mode (default). The device will set the RDS ready (RDSR) bit for a minimum of 40 ms when a valid RDS group has been received. Setting the RDS interrupt enable (RDSIEN) bit and GPIO2[1:0] = 10 will configure GPIO2 to pulse low for a minimum of 5 ms when a valid RDS group has been received. If an invalid group is received, RDSR will not be set and GPIO2 will not pulse low. In standard mode RDS synchronization (RDSS) and block error rate A, B, C and D (BLERA, BLERB, BLERC, and BLERD) are unused and will read 0. This mode is backward compatible with earlier firmware revisions.

Setting the RDS mode bit high places the device in RDS verbose mode. The device sets RDSS high when synchronized and low when synchronization is lost. If the device is synchronized, RDS ready (RDSR) will be set for a minimum of 40 ms when a RDS group has been received. Setting the RDS interrupt enable (RDSIEN) bit and GPIO2[1:0] = 10 will configure GPIO2 to pulse low for a minimum of 5 ms if the device is synchronized and an RDS group has been received. BLERA, BLERB, BLERC and BLERD provide block-error levels for the RDS group. The number of bit errors in each block within the group is encoded as follows: 00 = no errors, 01 = one to two errors, 10 = three to five errors, 11 = six or more errors. Six or more errors in a block indicate the block is uncorrectable and should not be used.

The Si4703 offers an RDS high-performance mode for RDS-only applications such as TMC (traffic message channel) coupled with a GPS device. The RDS performance bit RDSPRF 06h[9] is disabled by default for backwards compatibility with previous RDS firmware releases. When RDSPRF is enabled the device increases power to the LNA, sets RDS to unconditionally remain enabled, and disables FM impulse detection, thereby avoiding RDS shutdown and allowing the device to continue to track and decode RDS in very poor SNR environments.

The Si4703-B17 device possesses an enhanced RDS/TMC algorithm to improve RDS/TMC reception.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

4.5. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961 and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 8.

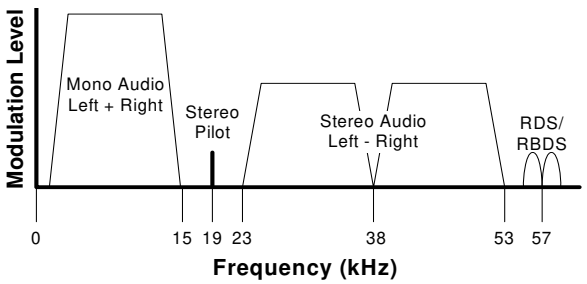


Figure 8. MPX Signal Spectrum

The Si4703's integrated stereo decoder automatically decodes the MPX signal. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L-R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L-R) signal. Separate left and right channels are obtained by adding and subtracting the (L+R) and (L-R) signals, respectively. The Si4703 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. The signal level range over which the stereo to mono blending occurs can be adjusted by setting the BLNDADJ[1:0] register. Stereo/mono status can be monitored with the ST register bit and mono operation can be forced with the MONO register bit.

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants, 50 or 75 µs, are used in various regions. The de-emphasis time constant is programmable with the DE bit.

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted with the DMUTE bit. Volume can be adjusted digitally with the VOLUME[3:0] bits. The volume dynamic range can be set to either –28 dBFS (default) or –58 dBFS by setting VOLEXT=1.

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in weak signal conditions. The soft mute attack and decay rate can be adjusted with the SMUTER[1:0] bits where 00 is the fastest setting. The soft mute attenuation level can be adjusted with the SMUTEA[1:0] bits where 00 is the most attenuated. The soft mute disable (DSMUTE) bit may be set high to disable this feature.

4.6. Tuning

The Si4703 uses Silicon Laboratories' patented and proven frequency synthesizer technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception.

The tuning frequency is defined as:

$$\text{Freq (MHz)} = \text{Spacing (kHz)} \times \text{Channel} + \text{Bottom of Band (MHz)}$$

Channel spacing of 50, 100 or 200 kHz is selected with bits SPACE[1:0]. The channel is selected with bits CHAN[9:0]. Band selection for Japan, Japan wideband, or Europe/U.S./Asia is set with BAND[1:0]. The tuning operation begins by setting the TUNE bit. After tuning completes, the seek/tune complete (STC) bit will be set and the RSSI level is available by reading bits RSSI[7:0]. The TUNE bit must be set low after the STC bit is set high in order to complete the tune operation and clear the STC bit.

Seek tuning searches up or down for a channel with an RSSI greater than or equal to the seek threshold set with the SEEKTH[7:0] bits. In addition, optional SNR and/or impulse noise detector criteria may be used to qualify valid stations. The SKSNR[3:0] bits set the SNR threshold required. The SKCNT[3:0] bits set the impulse noise threshold. Using the extra seek qualifiers can reduce false stops and, in combination with lowering the RSSI seek threshold, increase the number of found stations. The SNR and impulse noise detectors are disabled by default for backwards compatibility.

Two seek modes are available. When the seek mode (SKMODE) bit is low and a seek is initiated, the device seeks through the band, wraps from one band edge to the other, and continues seeking. If the seek operation is unable to find a valid channel, the seek failure/band limit (SF/BL) bit is set high and the device returns to the channel selected before the seek operation began. When the SKMODE bit is high and a seek is initiated, the device seeks through the band until the band limit is reached and the SF/BL bit is set high. A seek operation is initiated by setting the SEEK and SEEKUP bits. After the seek operation completes, the STC bit is set, and the RSSI level and tuned channel are available by reading bits RSSI[7:0] and bits READCHAN[9:0]. During a seek operation READCHAN[9:0] is also updated and may be read to determine and report seek progress.

The STC bit is set after the seek operation completes. The channel is valid if the seek operation completes and the SF/BL bit is set low. At other times, such as before a seek operation or after a seek completes and the SF/BL bit is set high, the channel is valid if the AFC Rail (AFCRL) bit is set low and the value of RSSI[7:0] is greater than or equal to SEEKTH[7:0]. Note that if a valid channel is found but the AFCRL bit is set, the audio output is muted as in the softmute case discussed in Section “4.5. Stereo Audio Processing”. The SEEK bit must be set low after the STC bit is set high in order to complete the seek operation. Setting the STC bit high clears STC status and SF/BL bits. The seek operation may be aborted by setting the SEEK bit low at any time.

The device can be configured to generate an interrupt on GPIO2 when a tune or seek operation completes. Setting the seek/tune complete (STCIEN) bit and GPIO2[1:0] = 01 will configure GPIO2 for a 5 ms low interrupt when the STC bit is set by the device.

For additional recommendations on optimizing the seek function, consult "AN284: Si4700/01/02/03 Seek Adjustability and Settings."

4.7. Reference Clock

The Si4703 accepts a 32.768 kHz reference clock to the RCLK pin. The reference clock is required whenever the ENABLE bit is set high. Refer to Table 3, “DC Characteristics,” on page 5 for switching voltage levels and Table 7, "FM Receiver Characteristics," on page 10 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to 2. "Typical Application Schematic" on page 12. The oscillator must be enabled or disabled while in powerdown (ENABLE = 0) as shown in Figure 9, “Initialization Sequence,” on page 18. Register 07h, bits [13:0], must be preserved as 0x0100 while in powerdown.

4.7.1. Si4703 Internal Crystal Oscillator Errata

The Si4703-B17 seek/tune performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4703-B17 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes and/or false stops. SDIO activity during all other operational states does not affect performance.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4703-B17 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The STC (seek/tune complete) interrupt should be used instead of polling to determine when a seek/tune operation is complete. Please refer to the Si4703-B17 data sheet for specified seek/tune times and register use guidelines.

The layout guidelines in Si4700/01/02/03 Evaluation Board User’s Guide, Section 8.3 Si4703 Daughter Card should be followed to help ensure robust FM performance.

Please refer to the posted Si4702/03 Internal Crystal Oscillator Errata for more information.

4.8. Control Interface

Two-wire slave-transceiver and three-wire interfaces are provided for the controller IC to read and write the control registers. Refer to “4.9. Reset, Powerup, and Powerdown” for a description of bus mode selection. Registers may be written and read when the V_{IO} supply is applied regardless of the state of the V_D or V_A supplies. RCLK is not required for proper register operation.

4.8.1. 3-Wire Control Interface

For three-wire operation, a transfer begins when the SEN pin is set low on a rising SCLK edge. The control word is latched internally on rising SCLK edges and is nine bits in length, comprised of a four bit chip address A7:A4 = 0110b, a read/write bit (write = 0 and read = 1), and a four bit register address, A3:A0. The ordering of the control word is A7:A5, R/W, A4:A0. Refer to Section 5. "Register Summary" on page 19 for a list of all registers and their addresses.

For write operations, the serial control word is followed by a 16-bit data word and is latched internally on rising SCLK edges.

For read operations, a bus turn-around of half a cycle is followed by a 16-bit data word shifted out on rising SCLK edges and is clocked into the system controller on falling SCLK edges. The transfer ends on the rising SCLK edge after SEN is set high. Note that 26 SCLK cycles are required for a transfer, however, SCLK may run continuously.

For details on timing specifications and diagrams, refer to Table 5, “3-Wire Control Interface Characteristics,” on page 7, Figure 3, “3-Wire Control Interface Write Timing Parameters,” on page 7, and Figure 4, “3-Wire Control Interface Read Timing Parameters,” on page 7.

4.8.2. 2-wire Control Interface

For two-wire operation, a transfer begins with the START condition. The control word is latched internally on rising SCLK edges and is eight bits in length, comprised of a seven bit device address equal to 0010000b and a read/write bit (write = 0 and read = 1). The device acknowledges the address by setting SDIO low on the next falling SCLK edge.

For write operations, the device acknowledge is followed by an eight bit data word latched internally on rising edges of SCLK. The device always acknowledges the data by setting SDIO low on the next falling SCLK edge. An internal address counter automatically increments to allow continuous data byte writes, starting with the upper byte of register 02h, followed by the lower byte of register 02h, and onward until the lower byte of the last register is reached. The internal address counter then automatically wraps around to the upper byte of register 00h and proceeds from there until continuous writes cease. Data transfer ceases with the STOP command. After every STOP command, the internal address counter is reset.

For read operations, the device acknowledge is followed by an eight bit data word shifted out on falling SCLK edges. An internal address counter automatically increments to allow continuous data byte reads, starting with the upper byte of register 0Ah, followed by the lower byte of register 0Ah, and onward until the lower byte of the last register is reached. The internal address counter then automatically wraps around to the upper byte of register 00h and proceeds from there until continuous reads cease. After each byte of data is read, the controller IC should return an acknowledge if an additional byte of data will be requested. Data transfer ceases with the STOP command. After every STOP command, the internal address counter is reset.

For details on timing specifications and diagrams, refer to Table 6, "2-Wire Control Interface Characteristics[1]," on page 8, Figure 5, "2-Wire Control Interface Read and Write Timing Parameters," on page 9 and Figure 6, "2-Wire Control Interface Read and Write Timing Diagram," on page 9.

4.9. Reset, Powerup, and Powerdown

Driving the $\overline{RST}$ pin low will disable the Si4703 and its control bus interface, and reset the registers to their default settings. Driving the $\overline{RST}$ pin high will bring the device out of reset. As the part is brought out of reset, one of two methods may be used to select between 2-wire and 3-wire control interface operation.

Busmode select method 1 requires the use of the GPIO3, $\overline{SEN}$, and SDIO pins. The GPIO3 pin should be externally driven low, set to hi-Z or left floating, and the SDIO pin should be externally driven low on the rising edge of $\overline{RST}$. The GPIO3 pin has an internal 1 MΩ pulldown resistor to ensure proper bus mode selection. To select 2-wire operation of the control interface, the $\overline{SEN}$ pin should be externally driven high on the rising edge of $\overline{RST}$. To select 3-wire operation of the control interface, the $\overline{SEN}$ pin should be externally driven low on the rising edge of $\overline{RST}$. Refer to Table 4, "Reset Timing Characteristics," on page 6 and Figure 1, "Reset Timing Parameters for Busmode Select Method 1," on page 6.

Busmode select method 2 only requires the use of the GPIO3 and GPIO1 pins. The GPIO3 pin should be driven high on the rising edge of $\overline{RST}$. Using this control interface bus selection method, a 100 kΩ or lower pull-up resistor should be used on the GPIO3 pin. To select 2-wire operation of the control interface, the GPIO1 and GPIO3 pins should be externally driven high on the rising edge of $\overline{RST}$. To select 3-wire operation of the control interface, the GPIO1 pin should be externally driven low on the rising edge of $\overline{RST}$. Refer to Table 4, "Reset Timing Characteristics," on page 6 and Figure 2, "Reset Timing Parameters for Busmode Select Method 2," on page 6. Table 8 below summarizes the two bus selection methods.

Table 8. Selecting 2-Wire or 3-Wire Control Interface Busmode Operation[1]

Busmode Select Method	$\overline{SEN}$	SDIO	GPIO1	GPIO3[2]	Bus mode
1	0	0	X	0[3]	3-wire
1	1	0	X	0[3]	2-wire
1 Xtal Oscillator	0	0	X	0[4]	3-wire
1 Xtal Oscillator	1	0	X	0[4]	2-wire
2	X	X	0	1[5]	3-wire
2	X	X	1	1[5]	2-wire
2 Xtal Oscillator	NA	NA	NA	NA	NA
2 Xtal Oscillator	NA	NA	NA	NA	NA

Notes:
1. All parameters applied on rising edge of $\overline{RST}$.
2. GPIO3 is internally pulled down with a 1 MΩ resistor.
3. GPIO3 should be externally driven low, set to high-Z (10 MΩ or greater pull-up) or float.
4. GPIO3 should be left floating.
5. GPIO3 should be externally driven high (100 kΩ or smaller pull-up).

When proper voltages are applied to the Si4703, the ENABLE and DISABLE bits in register 02h can be used to select between powerup and powerdown modes. When voltage is first applied to the device, ENABLE = 0 and DISABLE = 0. Setting ENABLE = 1 and DISABLE = 0 puts the device in powerup mode. To power down the device, the ENABLE and DISABLE bits should both be written to 1. After being written to 1, both bits will be cleared as part of the internal device powerdown sequence. To put the device back into powerup mode, set ENABLE = 1 and DISABLE = 0 as described above. The ENABLE bit should never be written to a 0.

4.10. Audio Output Summation

The audio outputs LOUT and ROUT may be capacitively summed with another device. Setting the audio high-Z enable (AHIZEN) bit maintains a dc bias of 0.5 x V_{IO} on the LOUT and ROUT pins to prevent the ESD diodes from clamping to the V_{IO} or GND rail in response to the output swing of the other device. The bias point is set with a 370 kΩ resistor to V_{IO} and GND. Register 07h containing the AHIZEN bit must not be written during the powerup sequence and only takes effect when in powerdown and V_{IO} is supplied. In powerup the LOUT and ROUT pins are set to the common mode voltage specified in Table 7, "FM Receiver Characteristics[1,2]," on page 10, regardless of the state of AHIZEN. Bits 13:0 of register 07h must be preserved as 0x0100 while in powerdown and as 0x3C04 while in powerup.

4.11. Initialization Sequence

Refer to Figure 9, "Initialization Sequence," on page 18.

To initialize the device:

1. Supply V_A and V_D.
2. Supply V_{IO} while keeping the $\overline{RST}$ pin low. Note that steps 1 and 2 may be reversed. Power supplies may be sequenced in any order.
3. Select 2-wire or 3-wire control interface bus mode operation as described in Section 4.9. "Reset, Powerup, and Powerdown" on page 17.
4. Provide RCLK. Steps 3 and 4 may be reversed when using an external oscillator. Wait 500 ms for oscillator startup when using internal oscillator.
5. Set the ENABLE bit high and the DISABLE bit low to powerup the device. Software should wait for the powerup time (as specified by Table 7, "FM Receiver Characteristics[1,2]," on page 10) before continuing with normal part operation.

To power down the device:

1. (Optional) Set the AHIZEN bit high to maintain a dc bias of 0.5 x V_{IO} volts at the LOUT and ROUT pins while in powerdown, but preserve the states of the other bits in Register 07h. Note that in powerup the LOUT and ROUT pins are set to the common mode voltage specified in Table 7 on page 10, regardless of the state of AHIZEN.
2. Set the ENABLE bit high and the DISABLE bit high to place the device in powerdown mode. Note that all register states are maintained so long as V_{IO} is supplied and the $\overline{RST}$ pin is high.
3. (Optional) Remove RCLK.
4. Remove V_A and V_D supplies as needed.

To power up the device (after power down):

1. Note that V_{IO} is still supplied in this scenario. If V_{IO} is not supplied, refer to device initialization procedure above.
2. (Optional) Set the AHIZEN bit low to disable the dc bias of 0.5 x V_{IO} volts at the LOUT and ROUT pins, but preserve the states of the other bits in Register 07h. Note that in powerup the LOUT and ROUT pins are set to the common mode voltage specified in Table 7 on page 10, regardless of the state of AHIZEN.
3. Supply V_A and V_D.
4. Provide RCLK. Wait 500 ms for oscillator startup when using internal oscillator.
5. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

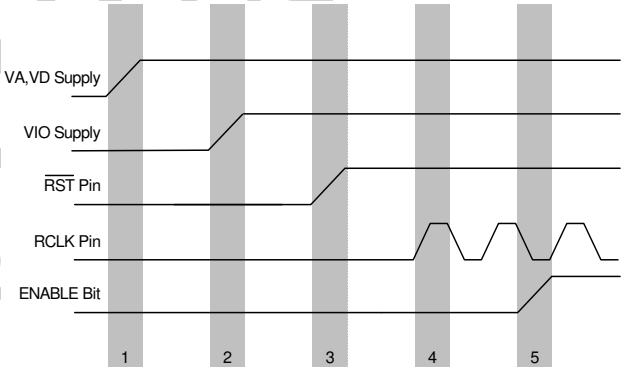


Figure 9. Initialization Sequence

4.12. Programming Guide

Refer to "AN230: Si4700/01 Programming Guide" for control interface programming information.

5. Register Summary

Reg[1]	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	DEVICEID	PN[3:0]				MFGID[11:0]											
01h	CHIPID	REV[5:0]						DEV[3:0]				FIRMWARE[5:0]					
02h	POWERCFG	DSMUTE	DMUTE	MONO	0	RDSM	SKMODE	SEEKUP	SEEK	0	DISABLE	0	0	0	0	0	ENABLE
03h	CHANNEL	TUNE	0	0	0	0	0	CHAN[9:0]									
04h	SYSCONFIG1	RDSIEN	STCIEN	0	RDS	DE	AGCD	0	0	BLNDADJ[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]	
05h	SYSCONFIG2	SEEKTH[7:0]								BAND[1:0]		SPACE[1:0]		VOLUME[3:0]			
06h	SYSCONFIG3	SMUTER[1:0]		SMUTEA[1:0]				RDSPRF	VOLEXT	SKSNR[3:0]				SKCNT[3:0]			
07h	TEST1	XOSCEN	AHIZEN														
08h	TEST2																
09h	BOOTCONFIG																
0Ah	STATUSRSSI	RDSR	STC	SF/BL	AFCRL	RDSS[2]	BLERA[1:0][2]		ST	RSSI[7:0]							
0Bh	READCHAN	BLERB[1:0][2]		BLERC[1:0][2]		BLERD[1:0][2]		READCHAN[9:0]									
0Ch	RDSA	RDSA[15:0]															
0Dh	RDSB	RDSB[15:0]															
0Eh	RDSC	RDSC[15:0]															
0Fh	RDSD	RDSD[15:0]															

Notes:

1. Any register not listed is reserved and should not be written. Writing to reserved registers may result in unpredictable behavior.
2. Available in RDS verbose mode only.

6. Register Descriptions

Register 00h. Device ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PN[3:0]				MFGID[11:0]											
Type	R				R											

Reset value = 0x1242

Bit	Name	Function
15:12	PN[3:0]	**Part Number.** 0x01 = Si4702/03
11:0	MFGID[11:0]	**Manufacturer ID.** 0x242

Register 01h. Chip ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REV[5:0]						DEV[3:0]				FIRMWARE[6:0]					
Type	R						R				R					

Reset value = 0x0800 for Si4703 Revision B.

Bit	Name	Function
15:10	REV[5:0]	**Chip Version.** 0x02 = Rev B
9:6	DEV[3:0]	**Device.** 0 before powerup. 0001 after powerup = Si4702. 1001 after powerup = Si4703.
5:0	FIRMWARE[6:0]	**Firmware Version.** 0 before powerup. Firmware version after powerup.

Register 02h. Power Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DSMUTE	DMUTE	MONO	0	RDSM	SKMODE	SEEKUP	SEEK	0	DISABLE	0	0	0	0	0	ENABLE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0x0000

Bit	Name	Function
15	DSMUTE	**Softmute Disable.** 0 = Softmute enable (default). 1 = Softmute disable.
14	DMUTE	**Mute Disable.** 0 = Mute enable (default). 1 = Mute disable.
13	MONO	**Mono Select.** 0 = Stereo (default). 1 = Force mono.
12	Reserved	**Reserved.** Always write to 0.
11	RDSM	**RDS Mode.** 0 = Standard (default). 1 = Verbose. Refer to “4.4. RDS/RBDS Processor and Functionality”.
10	SKMODE	**Seek Mode.** 0 = Wrap at the upper or lower band limit and continue seeking (default). 1 = Stop seeking at the upper or lower band limit.
9	SEEKUP	**Seek Direction.** 0 = Seek down (default). 1 = Seek up.
8	SEEK	**Seek.** 0 = Disable (default). 1 = Enable. **Notes:** **1.** Seek begins at the current channel, and goes in the direction specified with the SEEKUP bit. Seek operation stops when a channel is qualified as valid according to the seek parameters, the entire band has been searched (SKMODE = 0), or the upper or lower band limit has been reached (SKMODE = 1). **2.** The STC bit is set high when the seek operation completes and/or the SF/BL bit is set high if the seek operation was unable to find a channel qualified as valid according to the seek parameters. The STC and SF/BL bits must be set low by setting the SEEK bit low before the next seek or tune may begin. **3.** Seek performance for 50 kHz channel spacing varies according to RCLK tolerance. Silicon Laboratories recommends ±50 ppm RCLK crystal tolerance for 50 kHz seek performance. **4.** A seek operation may be aborted by setting SEEK = 0.

Bit	Name	Function
7	Reserved	**Reserved.** Always write to 0.
6	DISABLE	**Powerup Disable.** Refer to “4.9. Reset, Powerup, and Powerdown”. Default = 0.
5:1	Reserved	**Reserved.** Always write to 0.
0	ENABLE	**Powerup Enable.** Refer to “4.9. Reset, Powerup, and Powerdown”. Default = 0.

Register 03h. Channel

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TUNE	0	0	0	0	0	CHANNEL[9:0]									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

Reset value = 0x0000

Bit	Name	Function
15	TUNE	**Tune.** 0 = Disable (default). 1 = Enable. The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The STC bit must be set low by setting the TUNE bit low before the next tune or seek may begin.
14:10	Reserved	**Reserved.** Always write to 0.
9:0	CHAN[9:0]	**Channel Select.** Channel value for tune operation. If BAND 05h[7:6] = 00, then Freq (MHz) = Spacing (MHz) x Channel + 87.5 MHz. If BAND 05h[7:6] = 01, BAND 05h[7:6] = 10, then Freq (MHz) = Spacing (MHz) x Channel + 76 MHz. CHAN[9:0] is not updated during a seek operation. READCHAN[9:0] provides the current tuned channel and is updated during a seek operation and after a seek or tune operation completes. Channel spacing is set with the bits SPACE 05h[5:4].

Register 04h. System Configuration 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDSIEN	STCIEN	0	RDS	DE	AGCD	0	0	BLNDADJ[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W		R/W	

Reset value = 0x0000

Bit	Name	Function
15	RDSIEN	**RDS Interrupt Enable.** 0 = Disable Interrupt (default). 1 = Enable Interrupt. Setting RDSIEN = 1 and GPIO2[1:0] = 01 will generate a 5 ms low pulse on GPIO2 when the RDSR 0Ah[15] bit is set.
14	STCIEN	**Seek/Tune Complete Interrupt Enable.** 0 = Disable Interrupt (default). 1 = Enable Interrupt. Setting STCIEN = 1 and GPIO2[1:0] = 01 will generate a 5 ms low pulse on GPIO2 when the STC 0Ah[14] bit is set.
13	Reserved	**Reserved.** Always write to 0.
12	RDS	**RDS Enable.** 0 = Disable (default). 1 = Enable.
11	DE	**De-emphasis.** 0 = 75 µs. Used in USA (default). 1 = 50 µs. Used in Europe, Australia, Japan.
10	AGCD	**AGC Disable.** 0 = AGC enable (default). 1 = AGC disable.
9:8	Reserved	**Reserved.** Always write to 0.
6:7	BLNDADJ[1:0]	**Stereo/Mono Blend Level Adjustment.** Sets the RSSI range for stereo/mono blend. 00 = 31–49 RSSI dBµV (default). 01 = 37–55 RSSI dBµV (+6 dB). 10 = 19–37 RSSI dBµV (–12 dB). 11 = 25–43 RSSI dBµV (–6 dB). ST bit set for RSSI values greater than low end of range.
5:4	GPIO3[1:0]	**General Purpose I/O 3.** 00 = High impedance (default). 01 = Mono/Stereo indicator (ST). The GPIO3 will output a logic high when the device is in stereo, otherwise the device will output a logic low for mono. 10 = Low. 11 = High.

Bit	Name	Function
3:2	GPIO2[1:0]	**General Purpose I/O 2.** 00 = High impedance (default). 01 = STC/RDS interrupt. A logic high will be output unless an interrupt occurs as described below. 10 = Low. 11 = High. Setting STCIEN = 1 will generate a 5 ms low pulse on GPIO2 when the STC 0Ah[14] bit is set. Setting RDSIEN = 1 will generate a 5 ms low pulse on GPIO2 when the RDSR 0Ah[15] bit is set.
1:0	GPIO1[1:0]	**General Purpose I/O 1.** 00 = High impedance (default). 01 = Reserved. 10 = Low. 11 = High.

Register 05h. System Configuration 2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SEEKTH[7:0]								BAND[1:0]		SPACE[1:0]		VOLUME[3:0]			
Type	R/W								R/W		R/W		R/W			

Reset value = 0x0000

Bit	Name	Function
15:8	SEEKTH[7:0]	**RSSI Seek Threshold.** 0x00 = min RSSI (default). 0xFF = max RSSI. SEEKTH presents the logarithmic RSSI threshold for the seek operation. The Si4703 will not validate channels with RSSI below the SEEKTH value. SEEKTH is one of multiple parameters that can be used to validate channels. For more information, see "AN284: Si4700/01 Firmware 15 Seek Adjustability and Settings."
7:6	BAND[1:0]	**Band Select.** 00 = 87.5–108 MHz (USA,Europe) (Default). 01 = 76–108 MHz (Japan wide band). 10 = 76–90 MHz (Japan). 11 = Reserved.
5:4	SPACE[1:0]	**Channel Spacing.** 00 = 200 kHz (USA, Australia) (default). 01 = 100 kHz (Europe, Japan). 10 = 50 kHz.
3:0	VOLUME[3:0]	**Volume.** Relative value of volume is shifted –30 dBFS with the VOLEXT 06h[8] bit. VOLEXT = 0 (default). 0000 = mute (default). 0001 = –28 dBFS. : : 1110 = –2 dBFS. 1111 = 0 dBFS. VOLEXT = 1. 0000 = mute. 0001 = –58 dBFS. : : 1110 = –32 dBFS. 1111 = –30 dBFS. FS = full scale. Volume scale is logarithmic.