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Broadcast FM Radio Receiver for Consumer Electronics

Features

- Worldwide FM band support (64–108 MHz)
- Integrated antenna support
- EN55020 compliant
- Excellent real-world performance
- Freq synthesizer with integrated VCO
- Advanced FM seek tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Digital FM stereo decoder
- Minimal BOM
- Programmable de-emphasis
- Programmable reference clock
- Volume control
- Adjustable soft mute control
- RDS/RBDS processor (Si4705)
- Optional digital audio out (Si4705)
- 2-wire and 3-wire control interface
- Integrated LDO regulator
- Signal quality measurements
- 2.7 to 5.5 V supply voltage
- 3x3 mm 20-pin QFN package
  - RoHS compliant

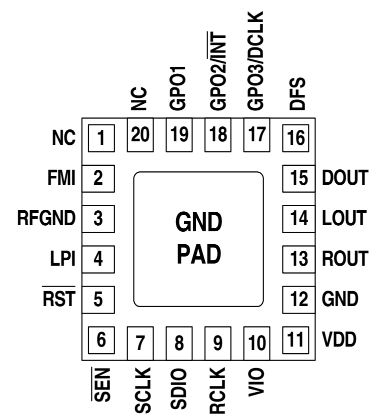
Ordering Information:
See page 28.

Applications

- Table and portable radios
- Stereos
- Mini/micro systems
- CD/DVD players
- Boom boxes
- Modules
- Clock radios
- Mini HiFi
- Entertainment systems

Pin Assignments

Si4704/05-GM (Top View)

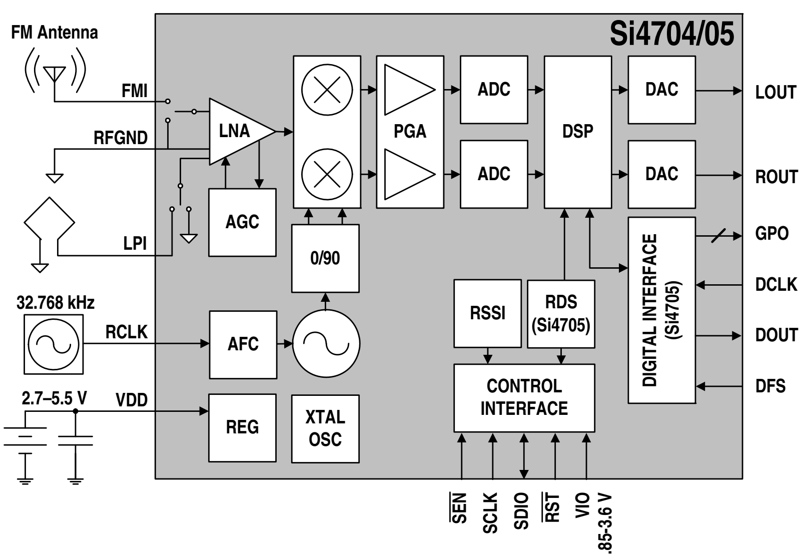


This product, its features, and/or its architecture is covered by one or more of the following patents, as well as other patents, pending and issued, both foreign and domestic: 7,127,217; 7,272,373; 7,272,375; 7,321,324; 7,355,476; 7,426,376; 7,471,940; 7,339,503; 7,339,504.

Description

The Si4704/05 integrates all functions required for an advanced broadcast FM radio receiver, from antenna input to stereo audio output.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.85	—	3.6	V
Digital Power Supply Powerup Rise Time	V_{DRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD}= 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4704/05 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should be done only at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. At RF input pin, FMI.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Receiver to Line Output						
Supply Current[1]	I_{FM}		—	19.2	22	mA
Supply Current[2]	I_{FM}	Low SNR level	—	19.9	23	mA
RDS Supply Current[1]	I_{FM}		—	19.2	23	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	320	600	µA
V_{DD} Powerdown Current	I_{DDPD}		—	10	20	µA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive	—	1	10	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	V_{IO} + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. Guaranteed by characterization.
2. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}\uparrow^4$	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:
1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is high impedance, then minimum t_{SRST} is 100 µs to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

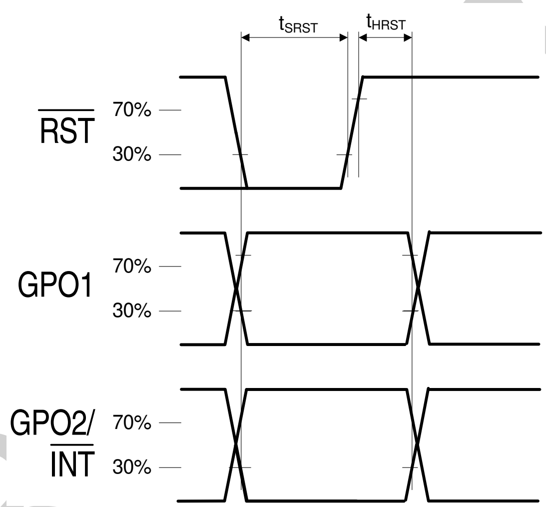


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1,2,3]
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold [4, 5]	$t_{HD:DAT}$		0	—	900	ns
SCLK Input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:
1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4704/05 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

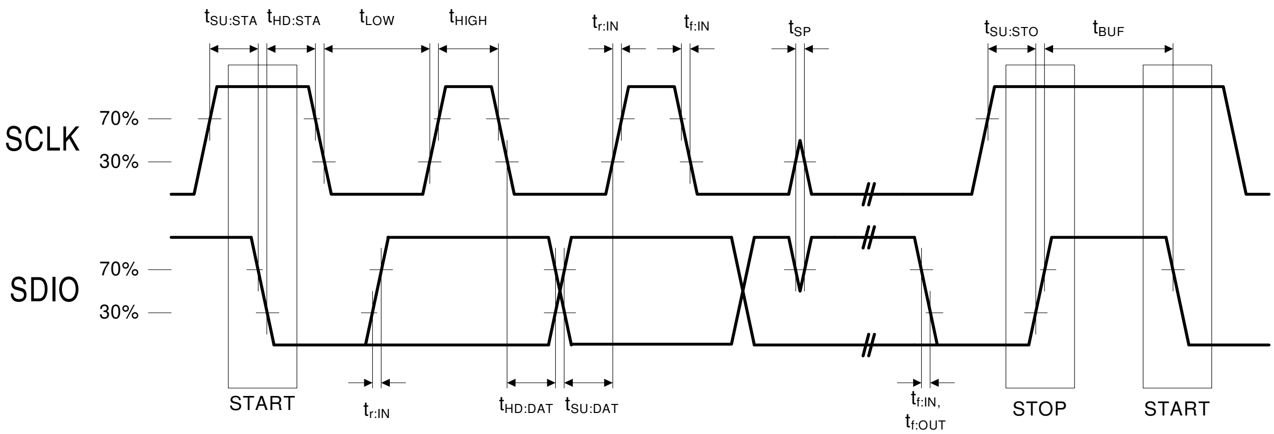


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

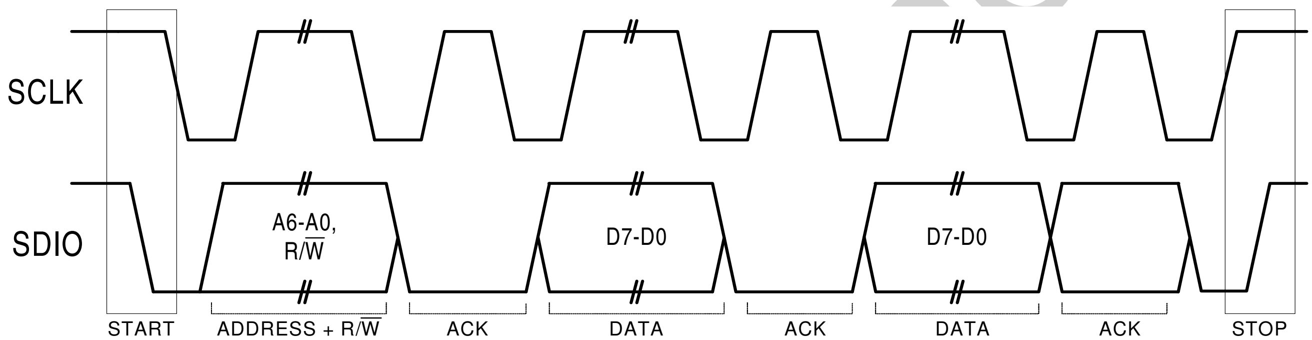


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

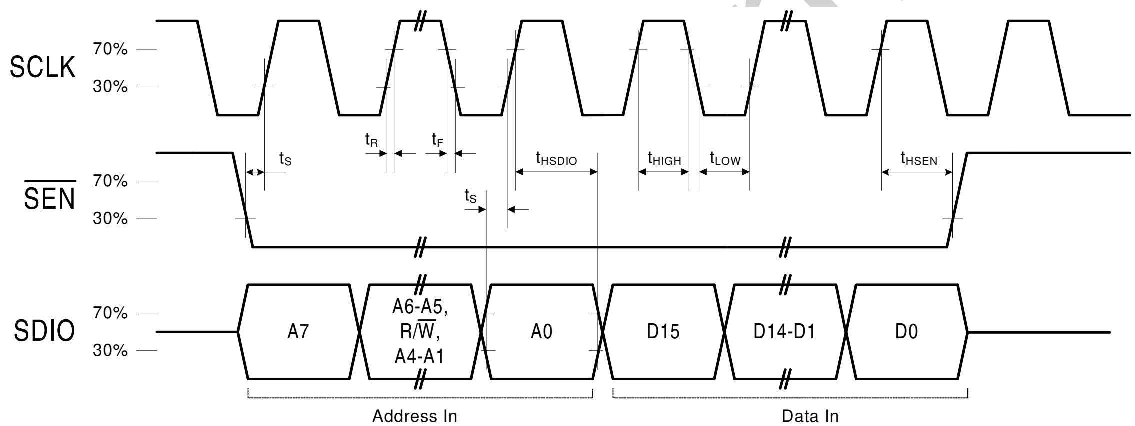


Figure 4. 3-Wire Control Interface Write Timing Parameters

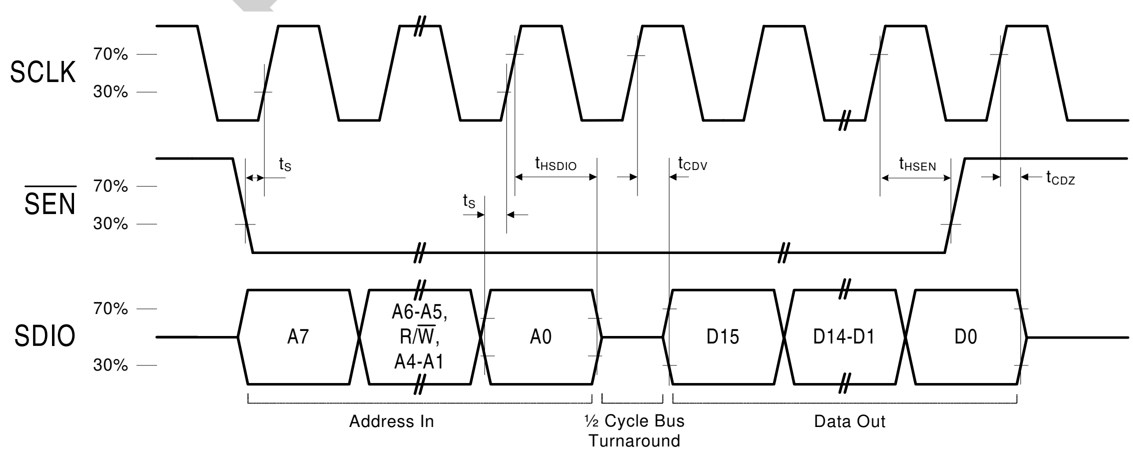


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

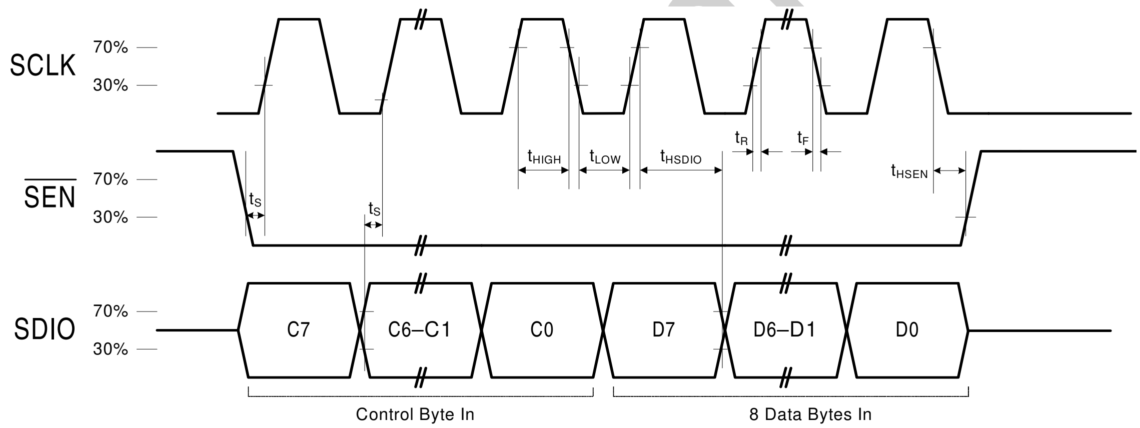


Figure 6. SPI Control Interface Write Timing Parameters

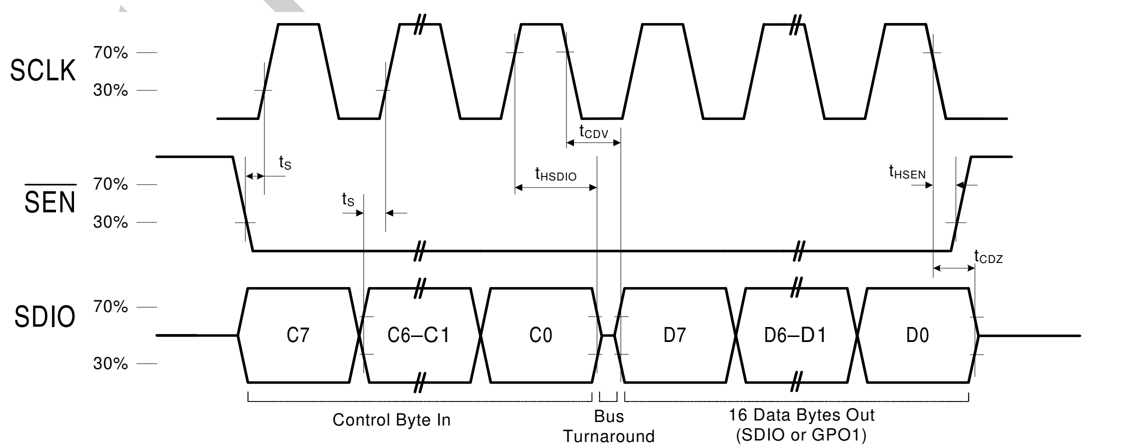


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

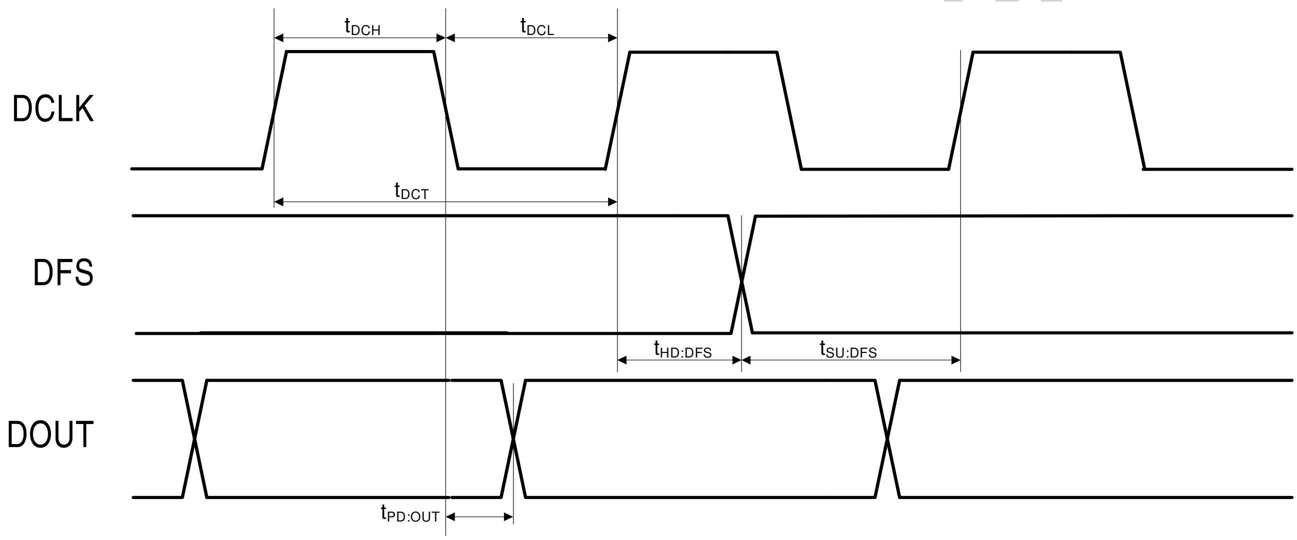


Figure 8. Digital Audio Interface Timing Parameters, I²S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity with Headphone Network[3,4,5]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
Sensitivity with 50 Ω Network[3,4,5,6]		(S+N)/N = 26 dB	—	1.1	—	µV EMF
RDS Sensitivity[6]		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
LPI Sensitivity[6]			—	3.5	—	µV EMF
LNA Input Resistance[6,7]			3	4	5	kΩ
LNA Input Capacitance[6,7]			4	5	6	pF
Input IP3[6,8]			100	105	—	dBµV EMF
AM Suppression[3,4,6,7]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[6]		In-band	35	—	—	dB
Audio Output Voltage[3,4,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,7,9]			—	—	1	dB
Audio Frequency Response Low[6]		–3 dB	—	—	30	Hz
Audio Frequency Response High[6]		–3 dB	15	—	—	kHz
Audio Stereo Separation[7,9]			32	42	—	dB
Audio Mono S/N[3,4,5,7,10]			55	63	—	dB
Audio Stereo S/N[4,5,6,7,10,11]			—	58	—	dB
Blocking Sensitivity[3,6,12,13]		Δf = ±400 kHz	—	32	—	dBµV
		Δf = ±4 MHz	—	38	—	dBµV

Notes:

1. Additional testing information is available in application note, "AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure." Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines" Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. Blocker Amplitude = 100 dBµV
13. Sensitivity measured at (S+N)/N = 26 dB.
14. At temperature 25°C.

Table 9. FM Receiver Characteristics[1,2] (Continued)
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermod Sensitivity[3,6,12,13]		Δf = ±400 kHz, ±800 kHz	—	40	—	dBµV
		Δf = ±4 MHz, ±8 MHz	—	35	—	dBµV
Audio THD[3,7,9]			—	0.1	0.5	%
De-emphasis Time Constant[6]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[6,10]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[6,10]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[6]		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time[6]		From powerdown	—	—	110	ms
RSSI Offset[14]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:
1. Additional testing information is available in application note, “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. Blocker Amplitude = 100 dBµV
13. Sensitivity measured at (S+N)/N = 26 dB.
14. At temperature 25°C.

Table 10. 64–75.9 MHz Input Frequency FM Receiver Characteristics[1,2,6]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		64	—	75.9	MHz
Sensitivity with Headphone Network[3,4,5]		(S+N)/N = 26 dB	—	4.0	—	µV EMF
LNA Input Resistance[7]			3	4	5	kΩ
LNA Input Capacitance[7]			4	5	6	pF
Input IP3[8]			100	105	—	dBµV EMF
AM Suppression[3,4,7]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	—	50	—	dB
Alternate Channel Selectivity		±400 kHz	—	70	—	dB
Audio Output Voltage[3,4,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,7,9]			—	—	1	dB
Audio Frequency Response Low		–3 dB	—	—	30	Hz
Audio Frequency Response High		–3 dB	15	—	—	kHz
Audio Mono S/N[3,4,5,7,10]			55	63	—	dB
Audio THD[3,7,9]			—	0.1	0.5	%
De-emphasis Time Constant		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[10]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[10]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time		From powerdown	—	—	110	ms
RSSI Offset[11]		Input levels of 8 and 60 dBµV EMF	–3	—	3	dB

Notes:

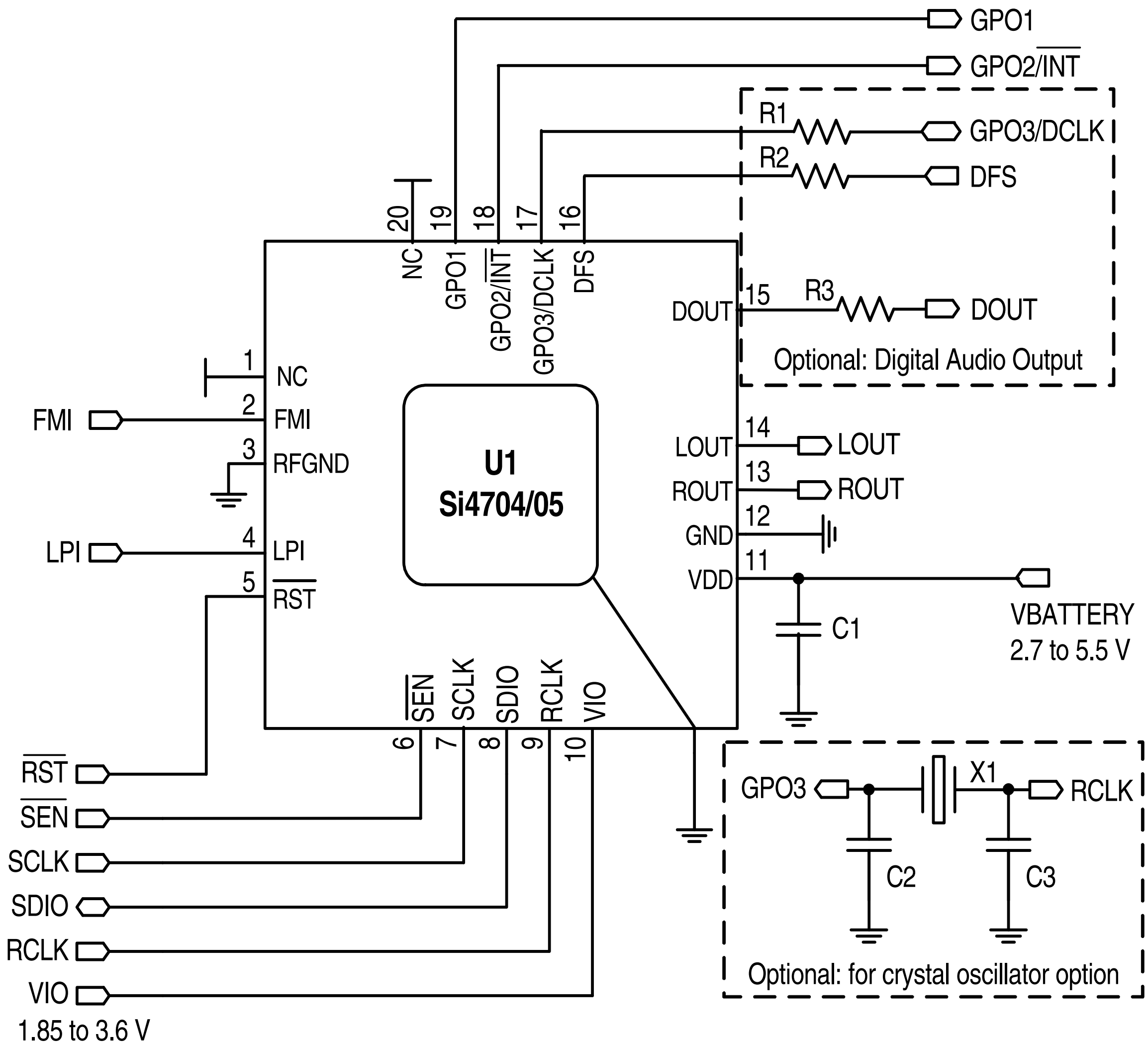
1. Additional testing information is available in "AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure." Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. At temperature (25 °C).

Table 11. Reference Clock and Crystal Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.85 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[2]			–100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance[2]			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF

Notes:
1. The Si4704/05 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See "AN332: Si47xx Programming Guide," Table 6 for more details.
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.

2. Typical Application Schematic



Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 or Pin 4 connects to the FM antenna interface. Pin 2 is for a headphone antenna. Pin 4 is for an integrated antenna.
6. Place Si4704/05 as close as possible to antenna and keep the FMI and LPI traces as short as possible.

3. Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
U1	Si4704/05 FM Radio Receiver	Silicon Laboratories
Optional Components		
C2, C3	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
R1	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R2	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R3	Resistor, 600 Ω (Optional: for digital audio)	Venkel

4. Functional Description

4.1. Overview

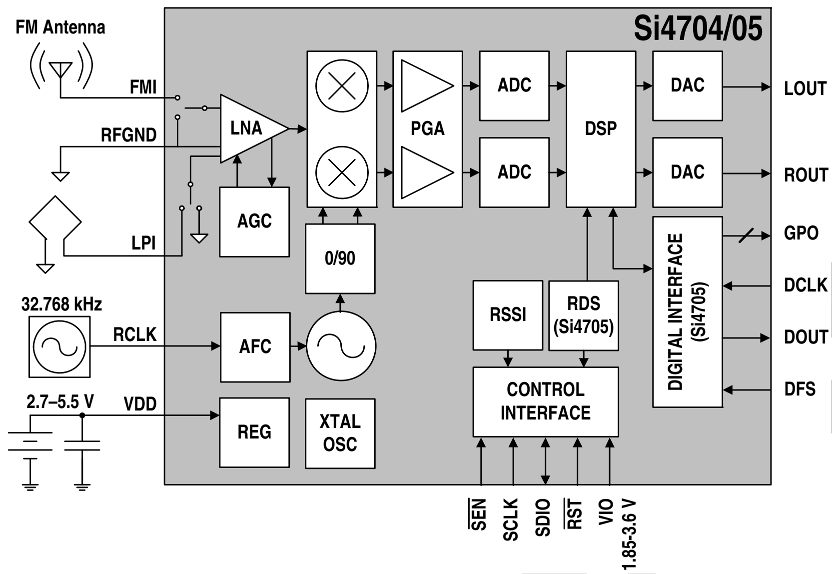


Figure 9. Functional Block Diagram

The Si4704/05 device leverages Silicon Laboratories' highly successful and proven Si4700/01/02/03 FM receiver, and offers unmatched integration and performance. The Si4704/05 offers additional features, such as EN55020 compliance, embedded antenna support, and a digital audio interface. The Si4704/05 is layout compatible with Silicon Laboratories' Si4710/11 FM Transmitter, Si4720/21 FM Transceiver, and Si4730/31 AM/FM Receiver. The Si4704/05 is the first FM radio receiver integrated circuit to support a short PCB trace or wire antenna, which can be integrated into the enclosure or PCB.

The Si4704/05's digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external inductor and bypass capacitor, and occupying board space of approximately 15 mm^2. Other advantages of the Si4704/05 include highly reliable device manufacturing, excellent quality, and ease of use to design-in and program.

The Si4704/05 includes line outputs from the on-chip digital-to-analog converters (DAC), digital audio mixers, a programmable reference clock input, and a configurable digital audio interface with the Si4705. The chip supports an I^2C-compliant 2-wire interface, an Si4700/01/02/03 backwards compatible 3-wire control interface, and an SPI control interface.

The Si4704/05 performs much of the FM demodulation digitally to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The on-board DSP provides unmatched pilot rejection, selectivity, and optimum sound quality. The Si4704/05 offers both the manufacturer and the end-user unmatched programmability and flexibility in the listening experience.

The Si4705 incorporates on-board processing capability for the European Radio Data System (RDS) and the US Radio Broadcast Data System (RBDS) including all the symbol encoding/decoding, block synchronization, error detection, and error correction functions. RDS allows digital information sent from the broadcaster to be displayed, such as station ID, song name, and music category. In Europe, alternate frequency (AF) information is also provided to automatically change stations in areas where broadcasters use multiple frequencies.

The Si4704/05 has two separate RF inputs. FMI is the input for use with a traditional FM antenna. The LPI input is for use with a short PCB trace or wire antenna that may be integrated into the system enclosure. There is a clocking mode to choose to clock the Si4704/05 from a reference clock or crystal. On the Si4705, there is an audio output mode to choose between an analog and/or digital audio output.

In the analog audio output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital audio mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog/digital audio output mode requires pins 13, 14, 15, 16, and 17.

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4704/05 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

The Si4704/05 is reset by applying a logic low on $\overline{RST}$ signal. This causes all register values to be reset to their default values. The digital output interface supply (V_{IO}) provides voltage to the $\overline{RST}$, $\overline{SEN}$, SDIO, RCLK, DOUT, DFS, and DCLK pins and can be connected to the audio baseband processor's supply voltage to save power and remove the need for voltage level translators. RCLK is not required for register operation.

The Si4704/05 reference clock is programmable, supporting many RCLK inputs as shown in Table 11.

4.2. Application Schematics and Operating Modes

The application schematic for the Si4704/05 is shown in Section "2. Typical Application Schematic" on page 16. The Si4704/05 supports selectable analog, digital, or concurrent analog and digital audio output modes. In the analog output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital output mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog and digital audio output mode requires pins 13, 14, 15, 16, and 17. In addition to output mode, there is a clocking mode to clock the Si4704/05 from a reference clock or crystal oscillator. The user sets the operating modes with commands as described in Section "5. Commands and Properties" on page 25.

4.3. FM Receiver

The Si4704/05 FM receiver is based on the proven Si4700/01 FM tuner. The receiver uses a digital low-IF architecture allowing the elimination of external components and factory adjustments. The Si4704/05 integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (64 to 108 MHz). An AGC circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the Si4704/05 to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

4.4. Digital Audio Interface (Si4705 Only)

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

4.4.1. Audio Data Formats

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.4.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

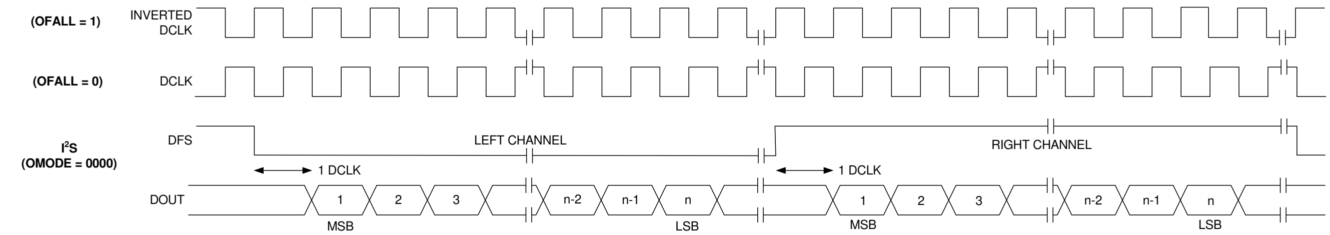


Figure 10. I²S Digital Audio Format

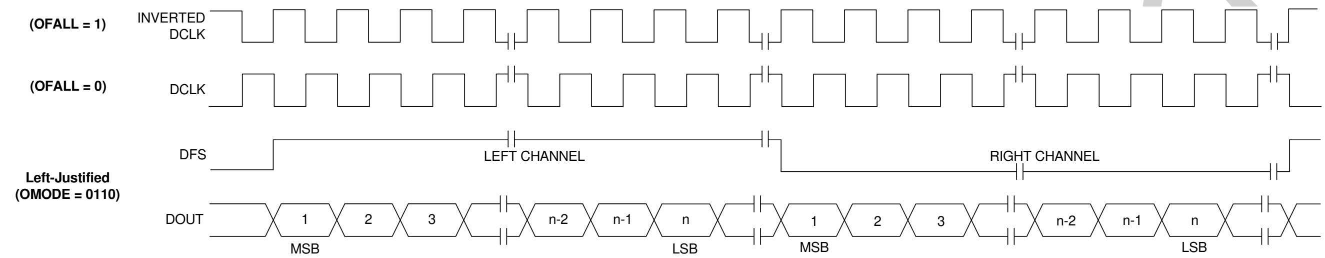


Figure 11. Left-Justified Digital Audio Format

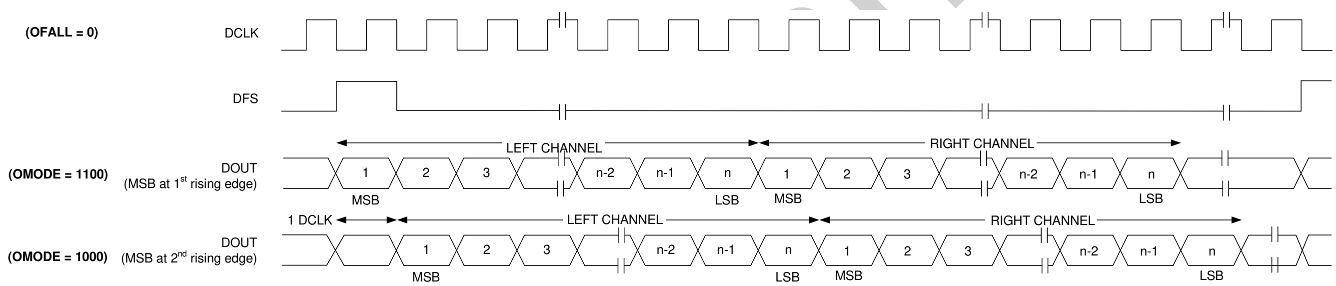


Figure 12. DSP Digital Audio Format

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4.5. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 13 below.

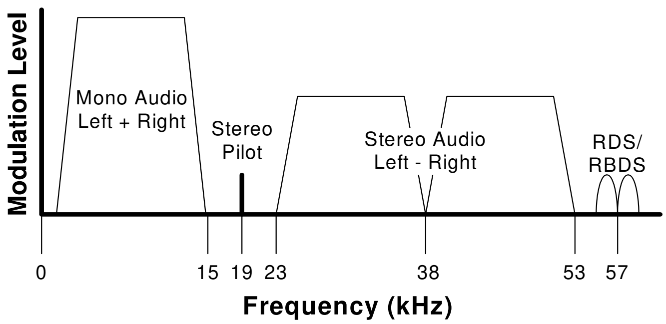

Figure 13. MPX Signal Spectrum

4.5.1. Stereo Decoder

The Si4704/05's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively. The Si4705 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

4.5.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the FM_RSQ_STATUS command. Mono operation can be forced with the FM_BLEND_MONO_THRESHOLD property.

4.6. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4704/05 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

4.7. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

4.8. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The softmute attenuation level is adjustable using the FM_SOFT_MUTE_MAX_ATTENUATION property.

4.9. RDS/RBDS Processor (Si4705 Only)

The Si4705 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4705 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4705 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors or that the block checkword contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

4.10. Tuning

The tuning frequency can be directly programmed using the FM_TUNE_FREQ command. The Si4704/05 supports channel spacing steps of 10 kHz in FM mode.

4.11. Seek

Seek tuning will search up or down for a valid channel. Valid channels are found when the receive signal strength indicator (RSSI) and the signal-to-noise ratio (SNR) values exceed the set threshold. Using the SNR qualifier rather than solely relying on the more traditional RSSI qualifier can reduce false stops and increase the number of valid stations detected. Seek is initiated using the FM_SEEK_START command. The RSSI and SNR threshold settings are adjustable using properties (see Table 14).

4.12. Reference Clock

The Si4704/05 reference clock is programmable, supporting RCLK frequencies in Table 11. Refer to Table 3, “DC Characteristics,” on page 5 for switching voltage levels and Table 9, “FM Receiver Characteristics,” on page 12 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic" on page 16. This mode is enabled using the POWER_UP command. Refer to Table 13, “Selected Si4704/05 Commands,” on page 25.

The Si4704/05 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4704/05 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4704/05 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

4.13. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4704/05 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si4704/05 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of $\overline{RST}$. The GPO1 pin includes an internal pull-up resistor, which is connected while $\overline{RST}$ is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while $\overline{RST}$ is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 12.

Table 12. Bus Mode Select on Rising Edge of $\overline{RST}$

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of $\overline{RST}$, the pins GPO1 and GPO2 are used as general purpose output (O) pins as described in Section “4.14. GPO Outputs”. In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.13.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of $\overline{RST}$.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4704/05 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4704/05 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the 7-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4704/05 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4704/05 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4704/05.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high. For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

4.13.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 3-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4704/05 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

4.13.3. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives SEN = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO).
- 0x80 = read a response (device drives one additional byte on SDIO).
- 0xC0 = read a response (device drives 16 additional bytes on SDIO).
- 0xA0 = read a response (device drives one additional byte on GPO1).
- 0xE0 = read a response (device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly eight data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly 1 byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep $\overline{\text{SEN}}$ low until all bytes have transferred. A transaction may be aborted at any time by setting $\overline{\text{SEN}}$ high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

4.14. GPO Outputs

The Si4704/05 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-impedance. The GPO pins can be reconfigured as specialized functions. GPO2/INT can be configured to provide interrupts and GPO3 can be configured to provide external crystal support or as DCLK in digital audio output mode.

4.15. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

4.16. Programming with Commands

To ease development time and offer maximum customization, the Si4704/05 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control an action such as powerup the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command. A partial list of commands is available in Table 13, “Selected Si4704/05 Commands,” on page 25.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold. A partial list of properties is available in Table 14, “Selected Si4704/05 Properties,” on page 26.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a one-byte status update indicating interrupt and clear-to-send status information. For a detailed description of the commands and properties for the Si4704/05, see “AN332: Universal Programming Guide.”

5. Commands and Properties

Table 13. Selected Si4704/05 Commands

Cmd	Name	Description
0x01	POWER_UP	Powerup device and mode selection. Modes include analog or digital output and reference clock or crystal support.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Powerdown device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x20	FM_TUNE_FREQ	Selects the FM tuning frequency.
0x21	FM_SEEK_START	Begins searching for a valid frequency.
0x22	FM_TUNE_STATUS	Queries the status of previous FM_TUNE_FREQ or FM_SEEK_START command.
0x23	FM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel (Si4705 only).
0x24	FM_RDS_STATUS	Returns RDS information for current channel and reads an entry from the RDS FIFO (Si4705 only).