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Si4706-C30

HIGH-PERFORMANCE FM RDS/RBDS RECEIVER

Note: The Si4706-C30 requires a patch for production operation. See section "11. Additional Reference Resources"

Features

- Worldwide FM band support (76–108 MHz)
- Advanced patented RDS/RBDS decoding engine
- Outstanding RDS sensitivity
- Leading RDS synchronization metrics
- Highly reliable RDS decoder
- RDS reception with FM mono broadcast
- Received signal quality indicators
- On-chip tuned resonance for embedded antenna support
- FM multi-path detection and mitigation
- FM Hi-cut control
- Advanced FM stereo-mono blend
- Automatic gain control (AGC)
- Integrated FM LNA
- Image-rejection mixer
- Frequency synthesizer with integrated VCO
- Low-IF direct conversion with no external ceramic filters
- 2.7 to 5.5 V supply voltage
- Programmable reference clock
- Stereo audio out
- I^2S Digital audio out
- 20-pin 3 x 3 mm QFN package
  - Pb-free/RoHS compliant

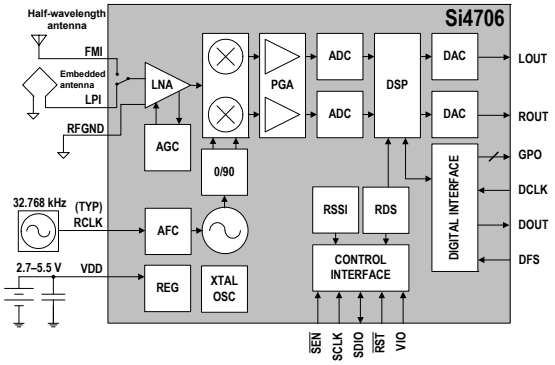
Applications

- Cellular handsets
- Portable media devices
- In-car navigation systems
- Dedicated data receiver
- Personal navigation devices (PND)
- GPS-enabled handsets and portable devices

Description

The high-performance Si4706-C30 FM RDS receiver provides the most advanced and flexible audio and RDS data processing available for portable devices today. The 100% CMOS IC integrates the complete FM and data receiver function from antenna to analog or digital audio and data out in a single 3 x 3 mm 20-pin QFN.

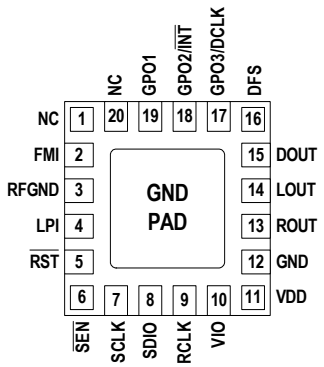
Functional Block Diagram



Ordering Information:
See page 29.

Pin Assignments

Si4706-GM
(Top View)



This product, its features, and/or its architecture is covered by one or more of the following patents, as well as other patents, pending and issued, both foreign and domestic: 7,127,217; 7,272,373; 7,272,375; 7,321,324; 7,355,476; 7,426,376; 7,471,940; 7,339,503; 7,339,504.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage[2]	V_{IO}		1.62	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
2. Operation with V_{IO} < 2.0 V requires a patch. See section “11. Additional Reference Resources”.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4706 device is a high-performance RF integrated circuit with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins DFS, SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2, and GPO3.
4. At RF input pins FMI and LPI.

Table 3. DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Receiver to Line Output						
V_{DD} Supply Current	I_{FM}	Analog Output Mode	—	21.4	24	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	400	600	µA
V_{DD} Powerdown Current	I_{DDPD}		—	10	20	µA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive	—	1	10	µA
High Level Input Voltage[1]	V_{IH}		0.7 x V_{IO}	—	V_{IO} + 0.3	V
Low Level Input Voltage[1]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[1]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[1]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[2]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[2]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
2. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}$↑[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}$↑	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is high impedance, then minimum t_{SRST} is 100 µs to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

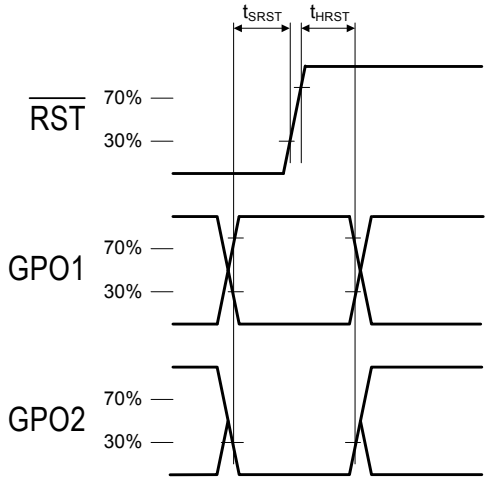


Figure 1. Reset Timing Parameters for Busmode Select Method

Table 5. 2-Wire Control Interface Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold [4, 5]	$t_{HD:DAT}$		0	—	900	ns
SCLK Input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4706 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

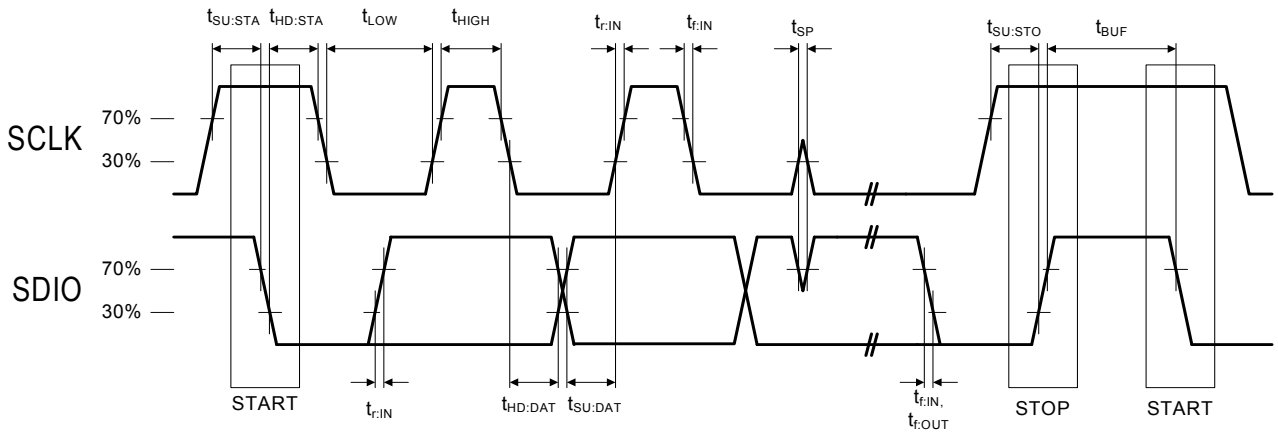


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

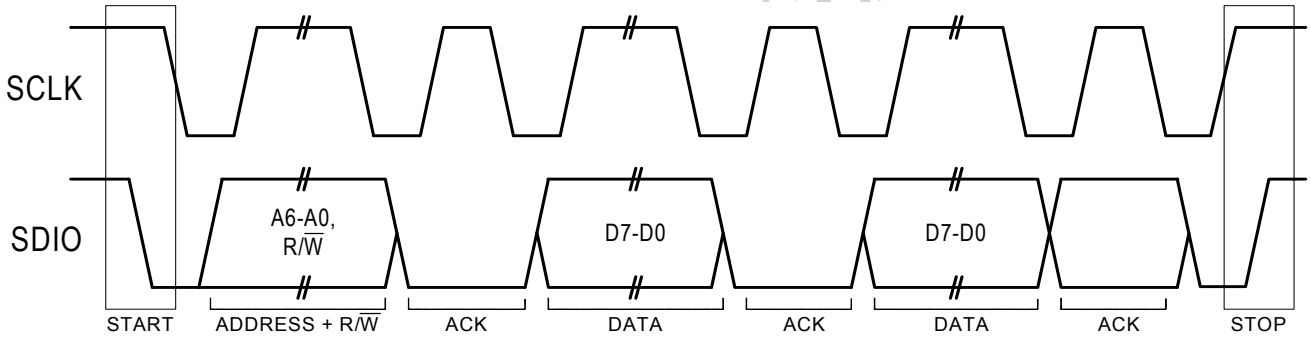


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

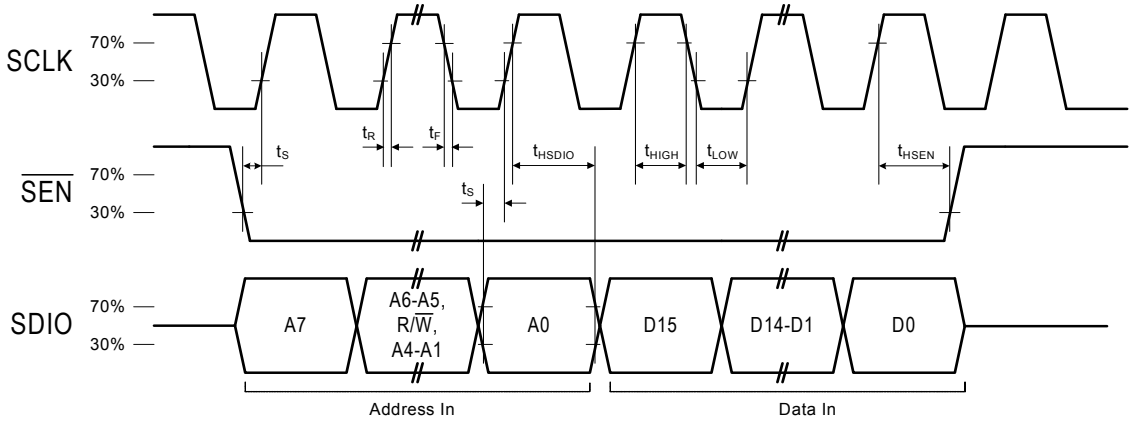


Figure 4. 3-Wire Control Interface Write Timing Parameters

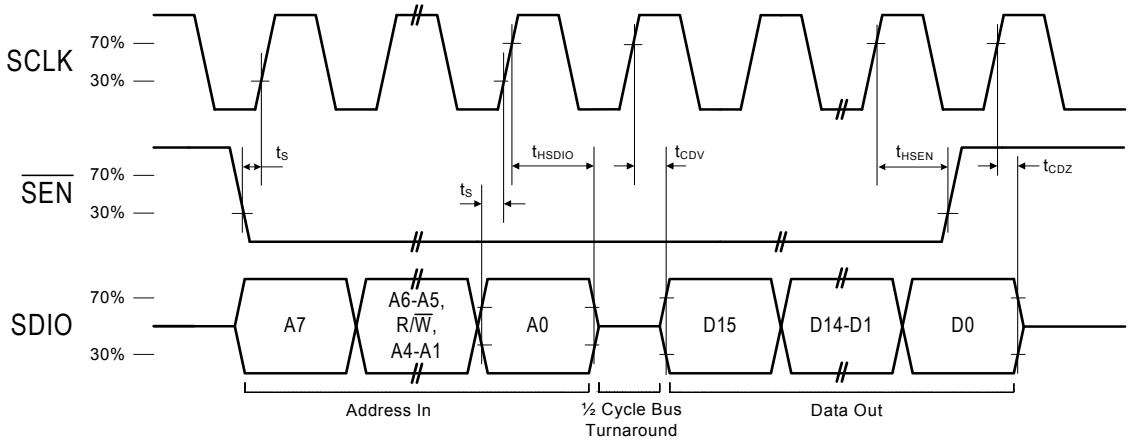


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

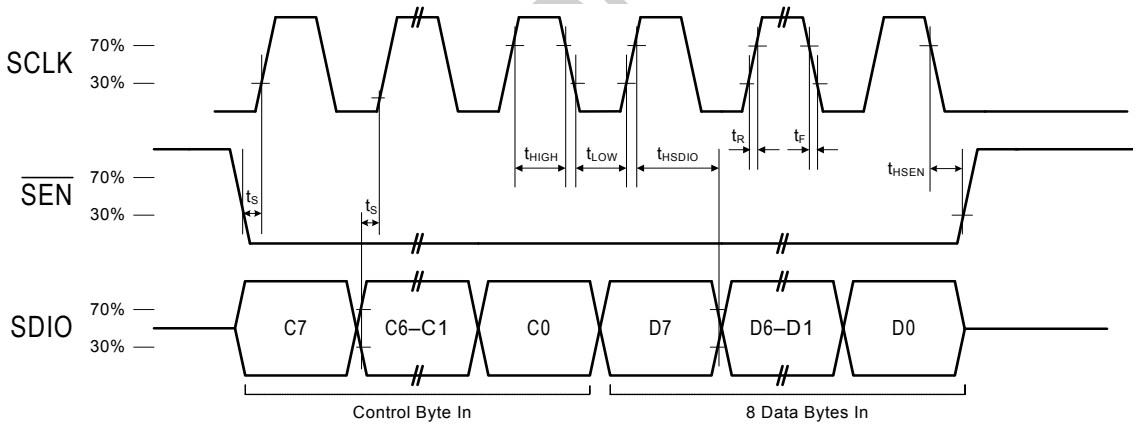


Figure 6. SPI Control Interface Write Timing Parameters

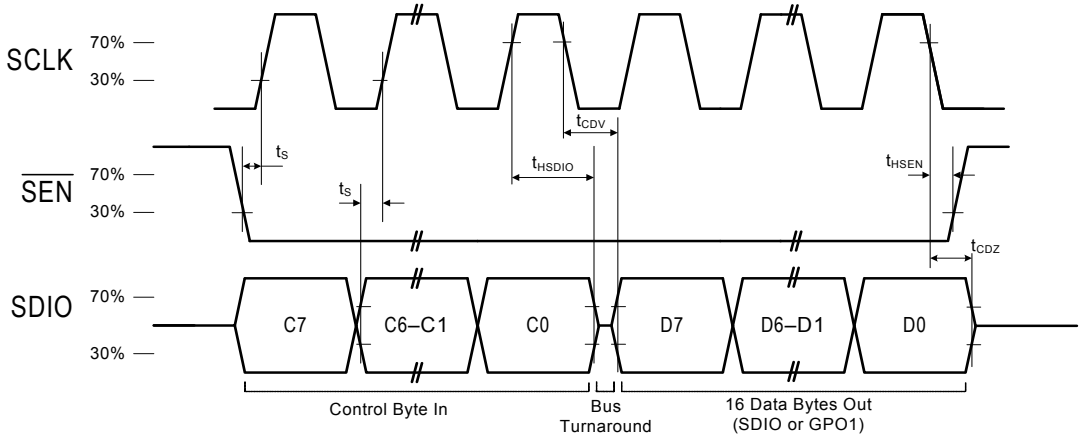


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

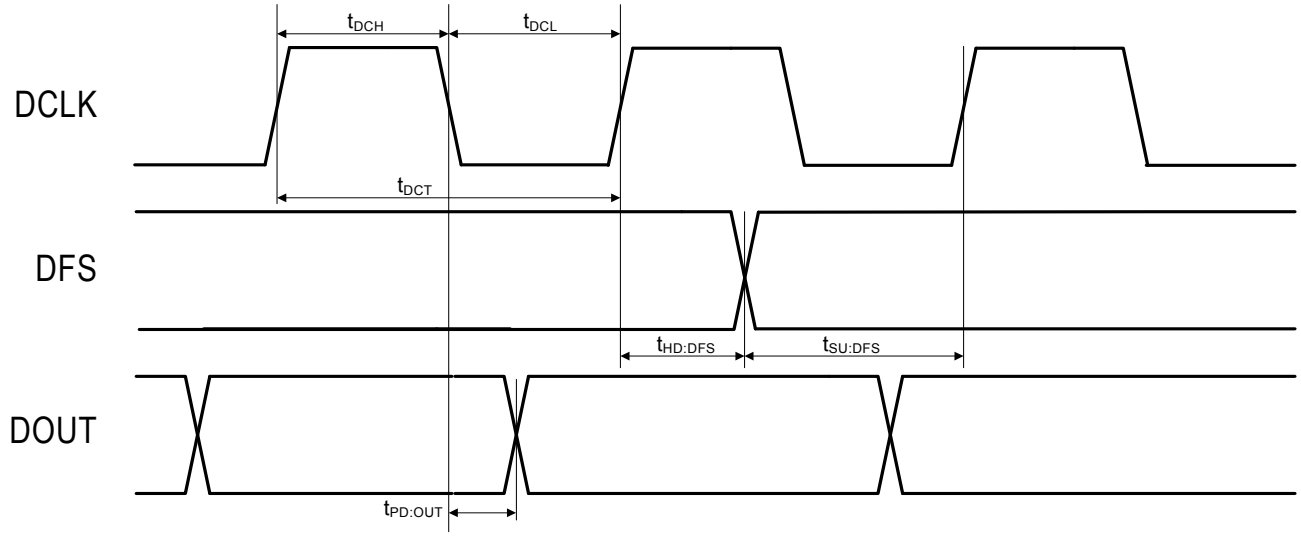


Figure 8. Digital Audio Interface Timing Parameters, I^2S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
RDS Sensitivity[3,4]		Δf = 2 kHz, RDS BLER < 5%	—	8	—	µV EMF
RDS Synchronization Persistence[3,4]		Δf = 2 kHz RDSSYNC = 1 ≥ 10 sec	—	3.8/60	—	µV EMF/RDS BLER%
RDS Synchronization Stability[3,4]		Δf = 2 kHz RDSSYNC = 1 ≥ 10 sec	—	5.9/10	—	µV EMF/ RDS BLER%
RDS Synchronization Time[3,4,5]		Δf = 2 kHz	—	40	—	ms
RDS PI Lock Time[3,4,5,5]		Δf = 2 kHz	—	60	—	ms
LNA Input Resistance[3]			3	4	5	kΩ
LNA Input Capacitance[3]			4	5	6	pF
Input IP3[3]		400 and 800 kHz blockers, AGC disabled	100	105	—	dBµV EMF
Image Rejection[3]			—	50	—	dB
AM Suppression[3]		m = 0.3	40	50	—	dB
Audio Sensitivity[4,6,7]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
Audio Sensitivity with 50 Ω Network[3,6,7]		(S+N)/N = 26 dB	—	1.1	—	µV EMF
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Blocking Sensitivity[3,8,9,10]		Δf = ±400 kHz	—	32	—	dBµV
		Δf = ±4 MHz	—	38	—	dBµV
Spurious Response Rejection[3]		In-band	35	—	—	dB
Audio Output Voltage[6]			72	80	90	mV_{RMS}

Notes:

1. Additional testing information is available in application note, “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN332: Si47xx Programming Guide”, “AN344: Si4706/07/4x Programming Guide”, and “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines”. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. Guaranteed by characterization.
4. Half-wavelength FM antenna matching network.
5. V_{EMF} = 1 mV.
6. Δf = 22.5 kHz.
7. B_{AF} = 300 Hz to 15 kHz, A-weighted.
8. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
9. Blocker Amplitude = 100 dBµV
10. Sensitivity measured at (S+N)/N = 26 dB.
11. Δf = 75 kHz.
12. At temperature 25 °C.

Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Output L/R Imbalance		Mono	–1	—	1	dB
Audio Frequency Response Low[3]		–3 dB	—	—	30	Hz
Audio Frequency Response High[3]		–3 dB	15	—	—	kHz
Audio Stereo Separation[5,6]			35	40	—	dB
Audio Mono S/N[5,6,7]			55	63	—	dB
Audio Stereo S/N[5,6,7]			—	58	—	dB
Audio THD[5,11]			—	0.1	0.5	%
De-emphasis Time Constant[3]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[3]	R_L	Single-ended, at LOUT/ROUT pins	10	—	—	kΩ
Audio Output Load Capacitance[3]	C_L	Single-ended, at LOUT/ROUT pins	—	—	50	pF
Seek/Tune Time[3]		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time[3]		From powerdown	—	—	110	ms
RSSI Offset[12]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:

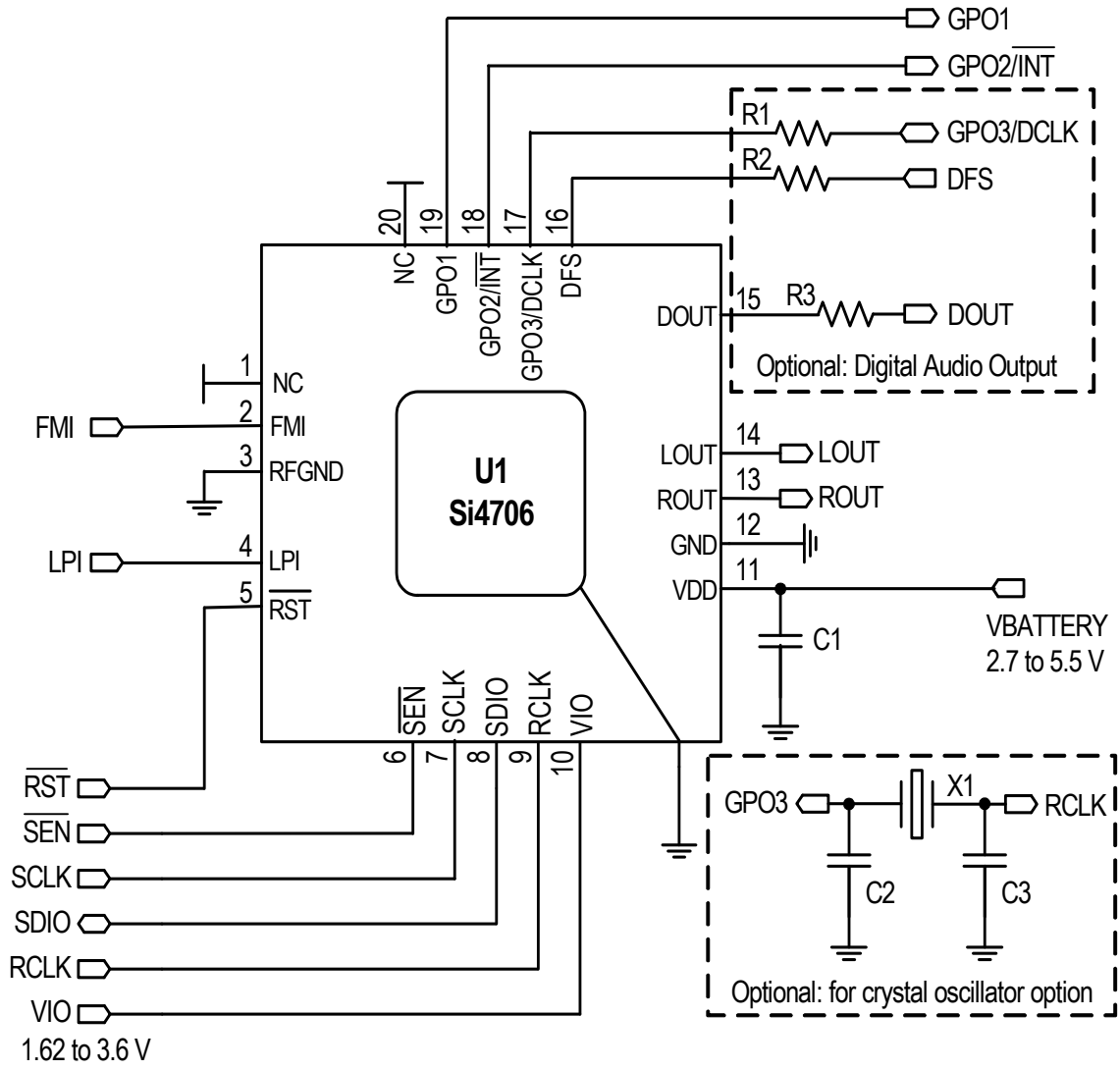
1. Additional testing information is available in application note, “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN332: Si47xx Programming Guide”, “AN344: Si4706/07/4x Programming Guide”, and “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines”. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. Guaranteed by characterization.
4. Half-wavelength FM antenna matching network.
5. V_{EMF} = 1 mV.
6. Δf = 22.5 kHz.
7. B_{AF} = 300 Hz to 15 kHz, A-weighted.
8. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
9. Blocker Amplitude = 100 dBµV
10. Sensitivity measured at (S+N)/N = 26 dB.
11. Δf = 75 kHz.
12. At temperature 25 °C.

Table 10. Reference Clock and Crystal Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1,2]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[1,3]			–100	—	100	ppm
REFCLK_PRESCALE[1,2]			1	—	4095	
REFCLK[1]			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency[1]			—	32.768	—	kHz
Crystal Frequency Tolerance[1,3]			–100	—	100	ppm
Board Capacitance[1]			—	—	3.5	pF

Notes:
1. Guaranteed by characterization.
2. The Si4706 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See “AN332: Universal Programming Guide,” Table 6 for more details.
3. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.

2. Typical Application Schematic



Notes:

1. Place C1 close to V_{DD} pin.
2. Pins 1 and 20 are no connects, leave floating.
3. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines". Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. Pin 2 or Pin 4 connects to the FM antenna interface. Pin 2 is for a half-wave antenna. Pin 4 is for an embedded antenna.
5. Place Si4706 as close as possible to antenna jack and keep the FMI and LPI traces as short as possible.

3. Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
U1	Si4706 FM Radio Receiver	Silicon Laboratories
Optional Components		
C2, C3	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
R1	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R2	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R3	Resistor, 600 Ω (Optional: for digital audio)	Venkel

4. Functional Description

4.1. Overview

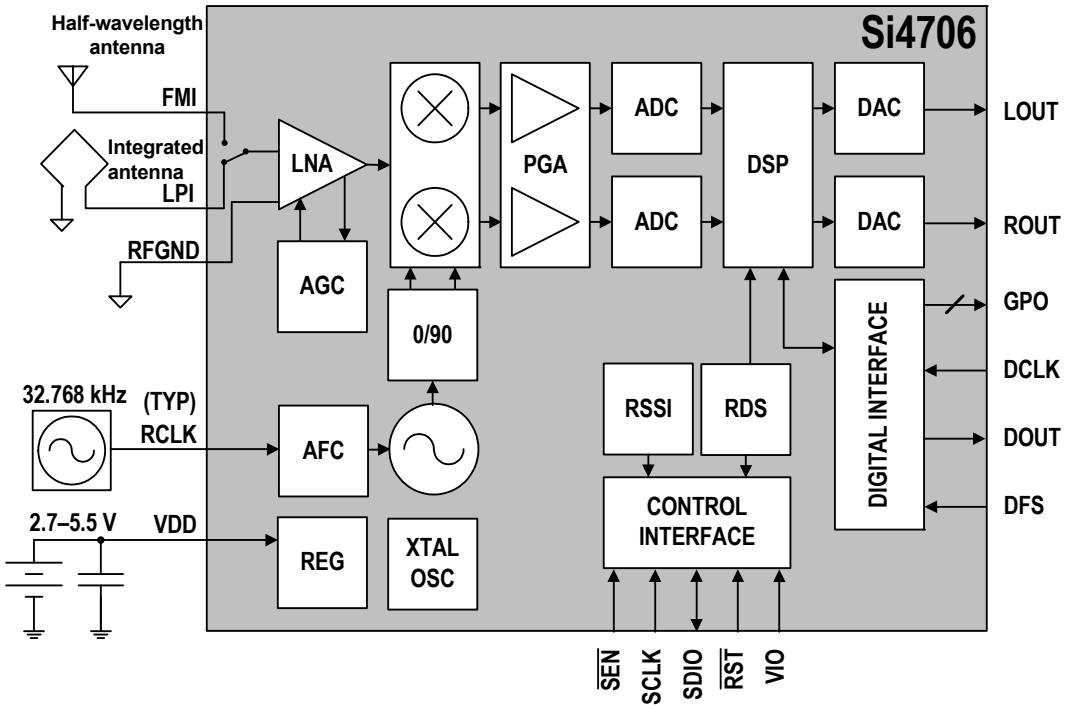


Figure 9. Functional Block Diagram

The Si4706-C30 offers advanced audio processing plus advanced RDS processing in a very small, 100% CMOS receiver integrated circuit. The device provides both analog and digital audio out, and a highly flexible RDS pre-processor and 100 block RDS buffer. It is an ideal product for handsets and portable devices seeking to optimize both sound and data receiver performance. For sound, the advanced audio processing is unprecedented in portable devices. For RDS data applications such as song-tagging, meta-data, traffic message channel, or other open data applications, the advanced and patented R(B)DS decoding engine offers outstanding data synchronization and integrity. The RDS engine includes demodulation, symbol decoding, advanced error correction, detailed visibility to block-error rates (BLER), advanced decoder reliability, and synchronization status. The Si4706 provides complete, decoded and error-corrected RDS groups (100 blocks), up to 25 groups at a time. The Si4706 offers several modes of operation for various applications which require more or less visibility to the RDS status and group data.

***Note:** The term "RDS" will be used to mean "RDS/RBDS" throughout the document.

The Si4706 receiver draws on Silicon Laboratories' broadcast audio know-how and patent portfolio, using a digital low intermediate frequency (low-IF) receiver architecture proven by hundreds of millions of Silicon Laboratories' broadcast audio receivers shipped worldwide.

Silicon Labs has shipped 1/2 billion broadcast audio receivers worldwide using this architecture. The low-IF architecture allows the Si4706 to deliver superior performance while integrating the great majority of external components required by competing solutions. The Si4706 digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external bypass capacitor and occupying board space of approximately 15 mm^2.

The Si4706 is the first FM radio receiver IC to support embedded antenna technology, allowing the FM antenna to be integrated into the enclosure or PCB of a portable device. For portable navigation devices, the Si4706 embedded antenna feature permits integration of the FM antenna into the enclosure of the device and eliminates the need for external antenna cables. Refer to "AN383: Si47XX Antenna, Schematic, Layout, And Design Guidelines" for antenna design guidelines.

The Si4706 is feature-rich, providing highly automated performance with default settings and extensive programmability and flexibility for customized system performance.

The Si4706 performs much of the FM demodulation digitally to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The on-board DSP provides unmatched pilot rejection, selectivity, and optimum sound quality. The integrated micro-controller offers both the manufacturer and the end-user unmatched programmability and flexibility in the listening experience.

4.2. FM Receiver

The Si4706 FM receiver is based on the proven Si4700/01/02/03 FM radio receiver. The part leverages Silicon Laboratories' proven and patented FM broadcast radio receiver digital architecture, delivering excellent RF performance and interference rejection. The proven digital techniques provide good sensitivity in weak signal environments while providing superb selectivity and inter-modulation immunity in strong signal environments.

The part supports the worldwide FM broadcast band (76 to 108 MHz) with channel spacings of 50–200 kHz. The Low-IF architecture utilizes a single converter stage and digitizes the signal using a high-resolution analog-to-digital converter. The audio output can be directed either to an external headphone amplifier via analog in/out or to other system ICs through digital audio interface (I^2S).

4.3. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 10 below.

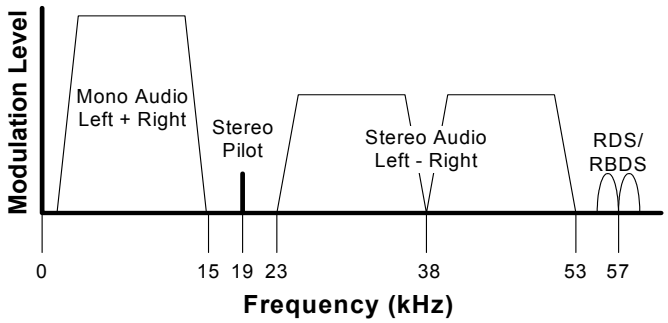


Figure 10. MPX Signal Spectrum

4.3.1. Stereo Decoder

The Si4706's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

4.3.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Three metrics, received signal strength indicator (RSSI), signal-to-noise ratio (SNR), and multi-path interference, are monitored simultaneously in forcing a blend from stereo to mono. The metric which reflects the minimum signal quality takes precedence and the signal is blended appropriately.

All three metrics have programmable stereo/mono thresholds and attack/release rates detailed in AN344 Revision 0.3: Si4706/07/4x Programming Guide (NDA) and greater. If a metric falls below its mono threshold, the signal is blended from stereo to full mono. If all metrics are above their respective stereo thresholds, then no action is taken to blend the signal. If a metric falls between its mono and stereo thresholds, then the signal is blended to the level proportional to the metric's value between its mono and stereo thresholds, with an associated attack and release rate. Stereo/mono status can be monitored with the FM_RSQ_STATUS command.

4.4. Received Signal Qualifiers

A tuned signal's quality can vary with the environmental conditions, time of day, and position of the antenna among many other factors. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si4706-C30 monitors and provides indicators of the signal quality, allowing the host processor to perform additional processing if required by the customer. The Si4706-C30 monitors and reports a set of standard industry signal quality metrics including RSSI, SNR, and multi-path interference on FM signals. As with other Si4706-C30 features, how these variables are used to improve audio performance can be left to the Silicon Labs default on-chip algorithms (recommended), or they can be customized to modify the performance of the part.

4.5. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4706 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

4.6. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

4.7. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The soft mute feature is triggered by the SNR metric. The SNR threshold for activating soft mute is programmable, as are soft mute attenuation levels and attack and decay rates.

4.8. FM Hi-Cut Control

Hi-cut control is employed on audio outputs with degradation of the signal due to low SNR and/or multi-path interference. Two metrics, SNR and multi-path interference, are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for both metrics. The transition frequency for hi-cut is also programmable with up to seven hi-cut filter settings. A single set of attack and release rates for hi-cut are programmable for both metrics from a range of 2 ms to 64 s. The level of hi-cut applied can be monitored with the FM_RSQ_STATUS command. Hi-cut can be disabled by setting the hi-cut filter setting to the default audio bandwidth of 15 kHz.

4.9. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology, including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency can be directly programmed using the FM_TUNE_FREQ. The Si4706 supports channel spacing of 50, 100, or 200 kHz in FM mode.

4.10. Seek

The Si4706 seek functionality is performed completely on-chip and will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds. The seek function can be made to stop at the band edge and provide an interrupt, or wrap the band and continue seeking until arriving at the original departure frequency. The device sets interrupts with found valid stations or, if the seek results in zero found valid stations, the device indicates failure and again sets an interrupt.(Refer to "AN332: Si47xx Programming Guide" and "AN344: Si4706/07/4x Programming Guide").

The Si4706-C30 uses RSSI, SNR, and AFC to qualify stations. Most of these variables have programmable thresholds to tailor the seek function to the subjective tastes of customers.

RSSI is employed first to screen all possible candidate stations. SNR and AFC are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations; however, the more challenging levels the thresholds are set to, the longer the overall seek time as more stations and more qualifiers will be assessed. The Si4706-C30 defaults set RSSI to a mid-level threshold and add an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations whilst keeping the seek time to acceptable levels. Generally, the time to auto-scan and store valid channels for an entire FM band with all thresholds engaged is very short depending on the band content.

Seek is initiated using the FM_SEEK_START or AM_SEEK_START commands. The RSSI and SNR threshold settings are adjustable using properties.

4.11. Digital Audio Interface

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4706 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

4.11.1. Audio Data Formats

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties. The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.11.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

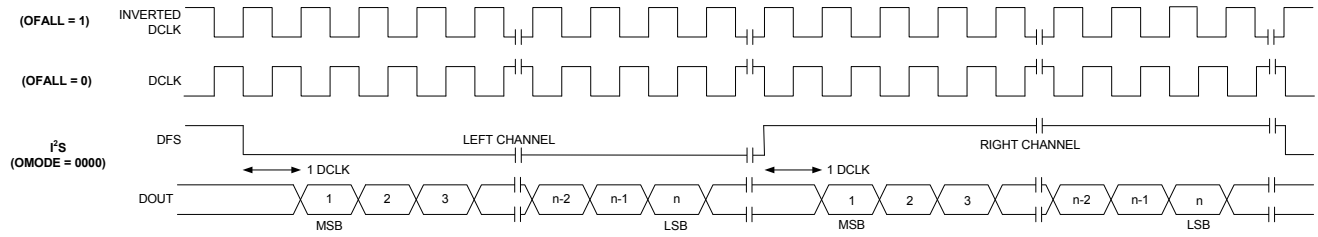


Figure 11. I²S Digital Audio Format

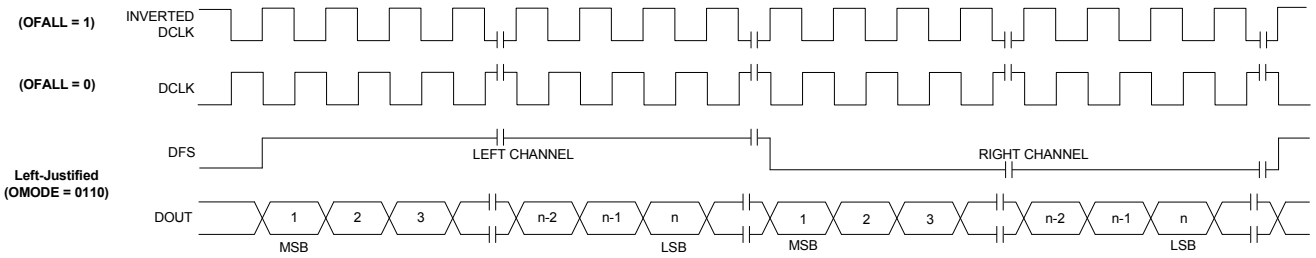


Figure 12. Left-Justified Digital Audio Format

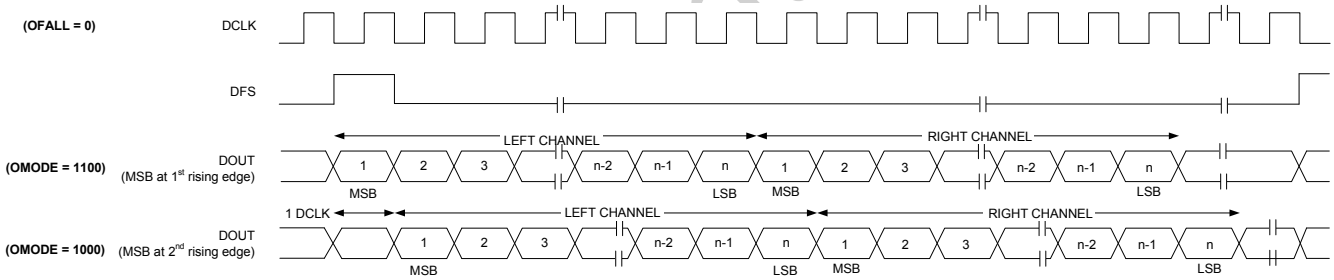


Figure 13. DSP Digital Audio Format

4.12. Embedded Antenna Support

The Si4706 is the first FM receiver to support the fast growing trend to integrate the FM receiver antenna into the device enclosure. The chip is designed with this function in mind from the outset, with multiple international patents pending, thus it is superior to many other options in price, board space, and performance.

Testing indicates that using Silicon Laboratories' patented techniques, FM performance using an embedded antenna can be very similar in many key metrics to performance using standard half-wavelength FM antennas. Refer to “AN383: Si47XX Antenna, Schematic, Layout, And Design Guidelines” for additional details on the implementation of support for an embedded antenna.

Figure 14 shows a conceptual block diagram of the Si4706 architecture used to support the embedded antenna. The half-wavelength FM receive antenna is therefore optional. Host software can detect the presence of an external antenna and switch between the embedded antenna if desired.

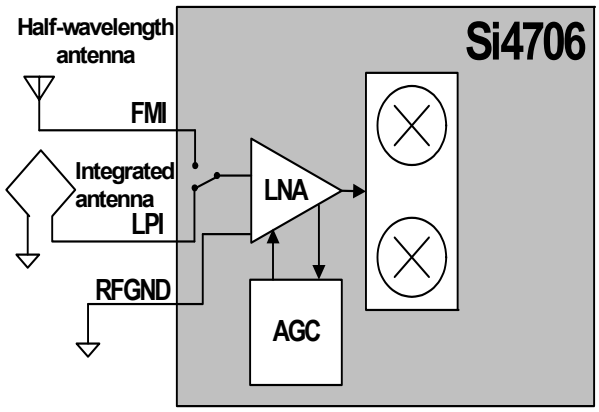


Figure 14. Conceptual Block Diagram of the Si4706 Embedded Antenna Support

4.13. RDS Decoder

The Si4706 implements an advanced, patented, high-performance RDS processor for demodulation, symbol decoding, block synchronization, error detection, and error correction. The RDS decoder provides several significant benefits over traditional implementations, including very fast and robust RDS synchronization in noisy signal levels with very high block error rates (BLER), industry-leading sensitivity, and improved data reliability in all signal environments.

Figure 15 illustrates the benefit of robust synchronization. The Si4706's strong synchronization performance at noisy signal levels minimizes or even eliminates re-synchronization time required as the signal carrier-to-noise ratio (CNR) fluctuates. The Si4706 decoder is continuously synchronized to the RDS block/group despite loss of data due to data block errors. This translates to lower loss of data compared to competing solutions.

Figure 16 illustrates the Si4706 RDS decoder performance. With the aid of robust synchronization, the decoder additionally provides for operation at lower sensitivity levels for a given BLER compared to competing solutions, and delivers reception in environments where signal power is very low or compromised. The decoder failure probability drops significantly compared to competing solutions.

The Si4706 also provides unmatched flexibility in programming the interaction between the host processor and the device. The Si4706 can be configured to provide varying levels of visibility from very high visibility to each RDS block with corresponding BLER, to a lower level of granularity providing complete RDS groups with BLER by block. Additionally, the Si4706 can provide interrupts on changes to RDS block A and/or B. The Si4706 device provides a configurable interrupt when RDS is synchronized and RDS group data has been received. The device provides configurable interrupts for up to 100 blocks with detailed BLER (25 groups), providing flexibility in interrupt configuration to the host controller. The Si4706 reports RDS decoder synchronization status and detailed bit errors for each RDS block with the FM_RDS_STATUS command. The range of reportable bit errors that are detected and corrected are 0, 1-2, 3-5, and "not correctable." More than five bit errors indicates that the corresponding block information word is not correctable.

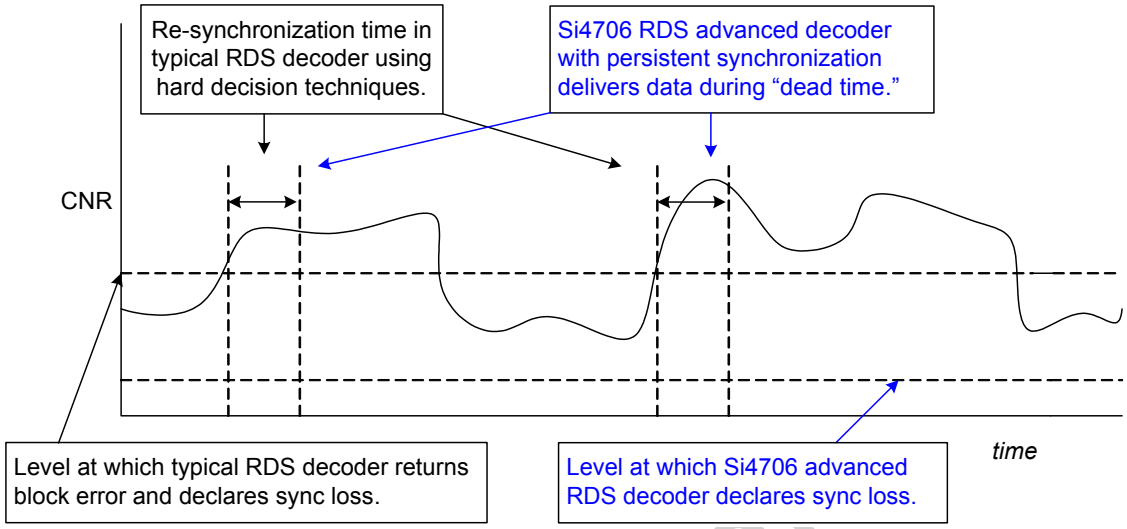


Figure 15. Illustrative Si4706 Advanced RDS Synchronization

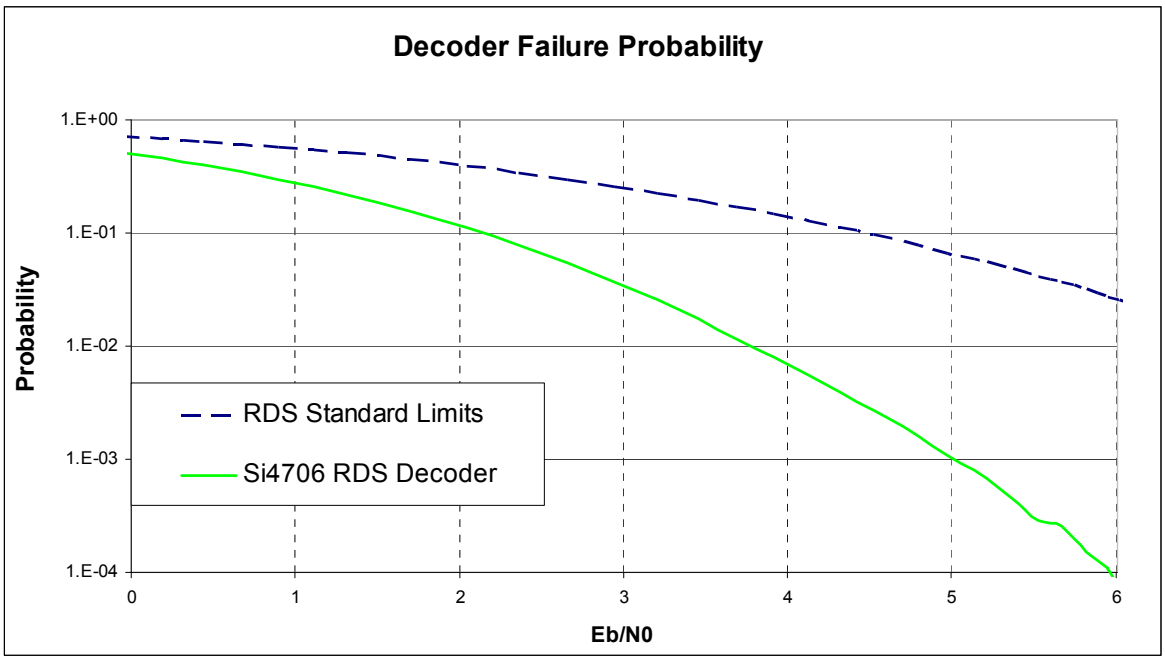


Figure 16. Si4706 Preliminary Decoder Performance

4.14. Reference Clock

The Si4706 reference clock is programmable, supporting RCLK frequencies in Table 10. Refer to Table 3, “DC Characteristics” on page 5 for switching voltage levels and Table 10, “Reference Clock and Crystal Characteristics” on page 14 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic" on page 15. This mode is enabled using the POWER_UP command. Refer to Refer to “AN332: Si47xx Programming Guide” and “AN344: Si4706/07/4x Programming Guide.”

The Si4706 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4706 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4706 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

4.15. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4706 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si4706 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of $\overline{\text{RST}}$. The GPO1 pin includes an internal pull-up resistor, which is connected while $\overline{\text{RST}}$ is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while $\overline{\text{RST}}$ is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 11.

Table 11. Bus Mode Select on Rising Edge of $\overline{\text{RST}}$

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of $\overline{\text{RST}}$, the pins GPO1 and GPO2 are used as general purpose output (O) pins as described in Section “4.16. GPO Outputs”. In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.15.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4706 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4706 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the 7-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4706 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4706 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4706.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high. For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

4.15.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 3-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4706 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.