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Si4720/21-B20

BROADCAST FM RADIO TRANSCEIVER FOR PORTABLE APPLICATIONS

Features

- Full FM RX and TX in 3 x 3 QFN
- Worldwide FM RX band support
- Compliant with worldwide FM TX regulations
- Excellent real-world performance
- Supports integrated TX/RX antenna
- Programmable transmit output voltage
- Frequency synthesizer with integrated VCO
- Integrated LDO regulator
- Minimal BOM (15 mm^2)
- Digital audio output (Si4721 only)
- Digital audio input
- Adjustable seek parameters
- Adjustable mono/stereo blend
- Adjustable soft mute
- Advanced modulation control
- Audio dynamic range control
- Audio silence detector
- Programmable reference clock input
- 2-wire and 3-wire control interface
- 2.7 to 5.5 V supply voltage
- 3 x 3 x 0.55 mm 20-pin Pb-free QFN package
- RDS/RDBS encoder/decoder (Si4721 only)

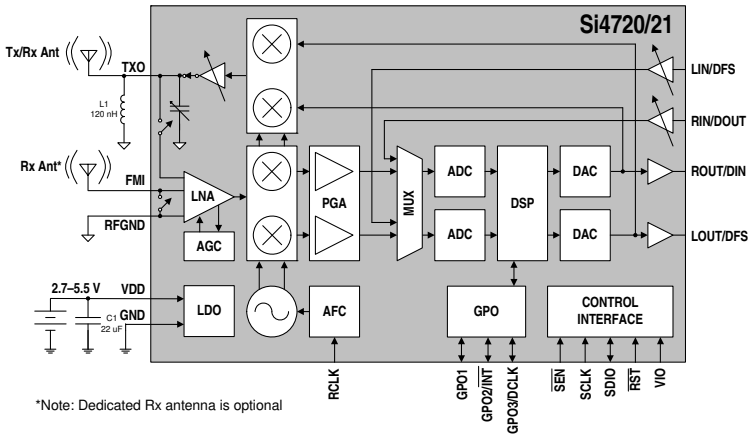
Applications

- Cellular handsets/hands-free
- MP3 players
- Portable media players
- Wireless speakers/microphone
- Satellite digital audio radios
- Personal computers/notebooks

Description

The Si4720/21 integrates the complete tuner and transmit functions for FM broadcast reception and standards-compliant, unlicensed FM broadcast stereo transmission. Users must comply with local radio frequency (RF) transmission regulations.

Functional Block Diagram



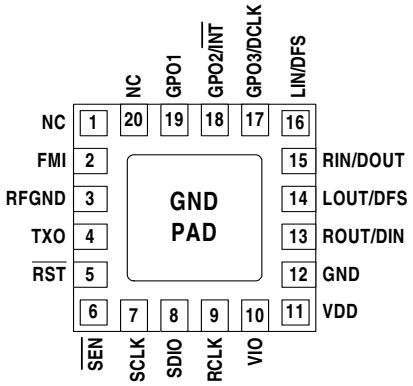
*Note: Dedicated Rx antenna is optional

Ordering Information:

See page 42.

Pin Assignments

Si4720/21
(Top View)



Patents pending

Notes:

1. To ensure proper operation and FM transceiver performance, follow the guidelines in "AN383: 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place the Si4720/21 as close as possible to the antenna jack, and keep the FMI trace as short as possible.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Power Supply Power-Up Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Power-Up Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4720/21 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.
4. At RF input pin FMI.

Table 3. DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Receiver						
RX Supply Current	I_{RX}		—	19.2	22	mA
RX Supply Current[1]	I_{RX}	Low SNR level	—	19.8	23	mA
RX Interface Supply Current	I_{IORX}		—	320	600	µA
RX RDS Supply Current[2]	I_{FM}	Analog Output Mode	—	19.9	23	mA
RX Supply Current[2]	I_{FMD}	Digital Output Mode	—	18.0	20.5	mA
FM Transmitter						
TX Supply Current	I_{TX}		—	18.8	22.8	mA
TX Interface Supply Current	I_{IOTX}		—	320	600	µA
FM Transmitter from Digital Audio Input						
TX Supply Current	I_{DTX}	DCLK = 3.072 MHz	—	18.3	—	mA
TX Interface Supply Current	I_{DIO}	DCLK = 3.072 MHz	—	320	—	µA
FM Transmitter in Receive Power Scan Mode						
RX Supply Current	I_{RX}		—	16.8	—	mA
RX Interface Supply Current	I_{IORPS}		—	400	—	µA
Supplies and Interface						
V_{DD} Powerdown Current	I_{DDPD}	Powerdown mode	—	10	20	µA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive Powerdown mode	—	3	10	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	VIO + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x VIO	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
2. Guaranteed by characterization.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.
4. For output pins SDIO, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}$↑[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}$↑	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the 1st start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

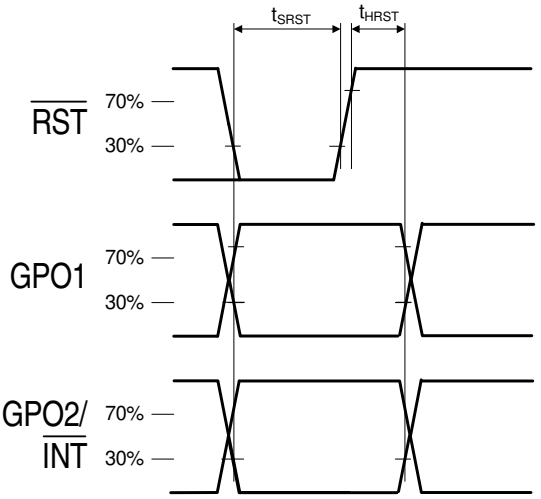


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1\ pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1\ pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low-impedance. 2-wire control interface is I^2C compatible.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4720/21 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

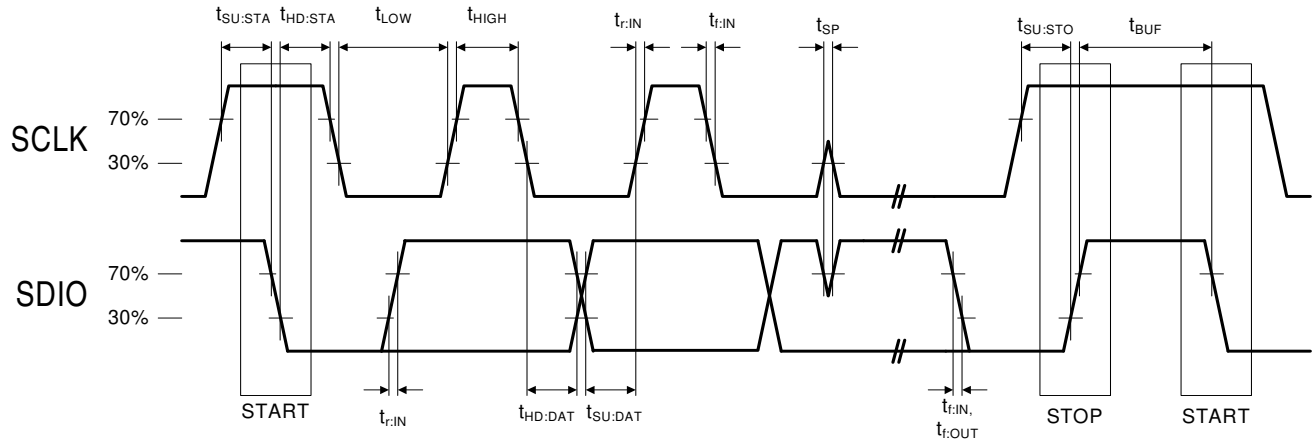


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

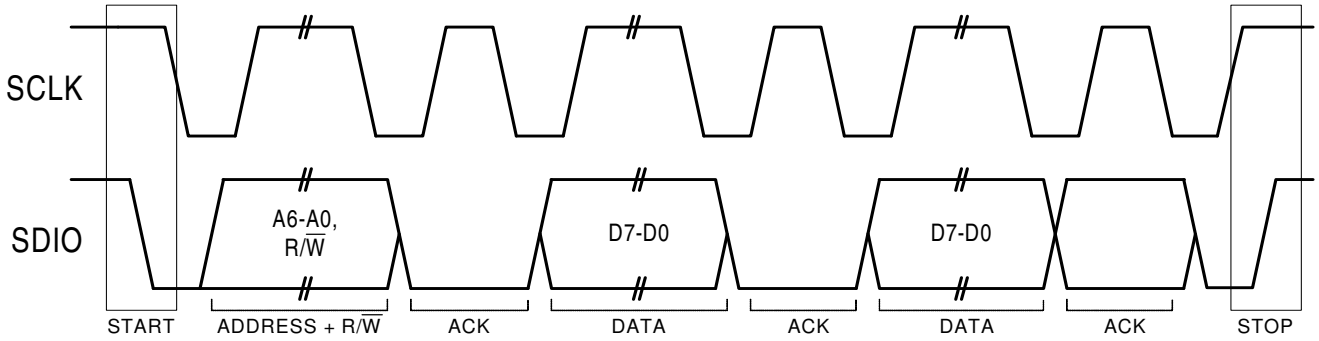


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

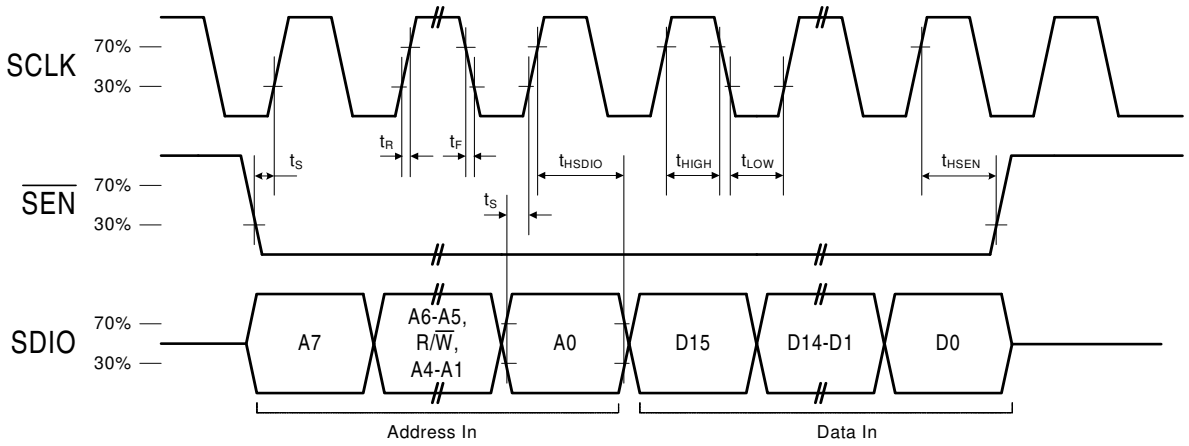


Figure 4. 3-Wire Control Interface Write Timing Parameters

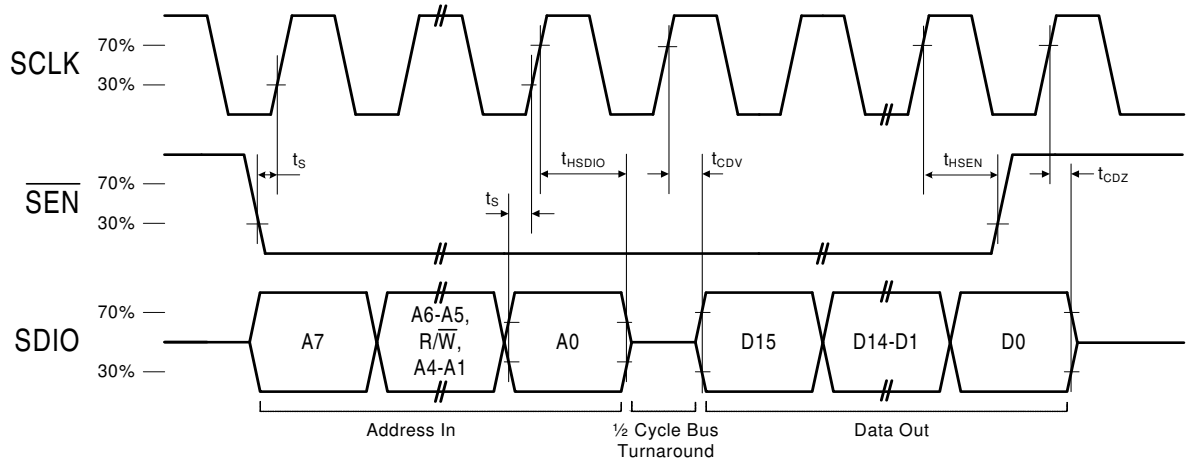


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

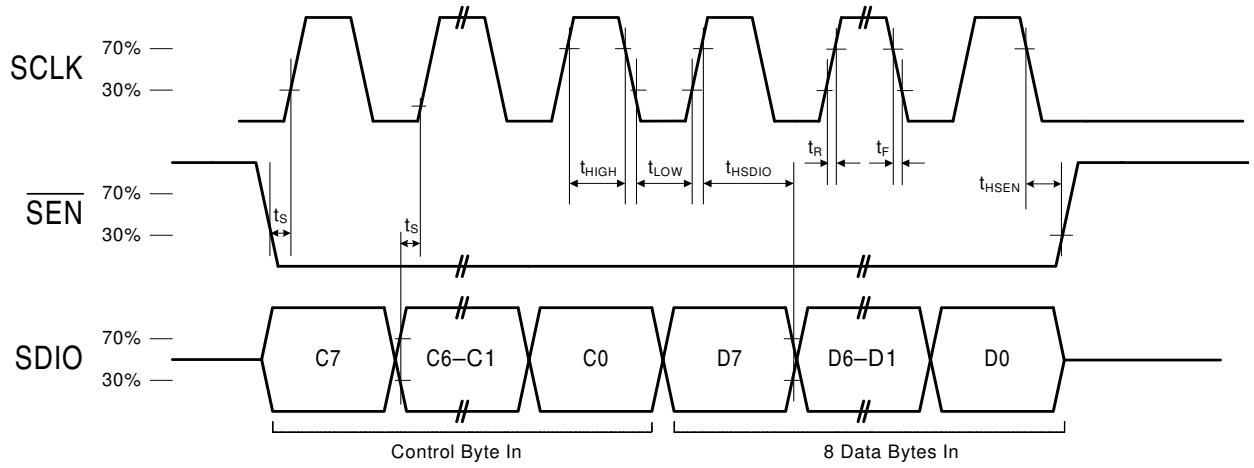


Figure 6. SPI Control Interface Write Timing Parameters

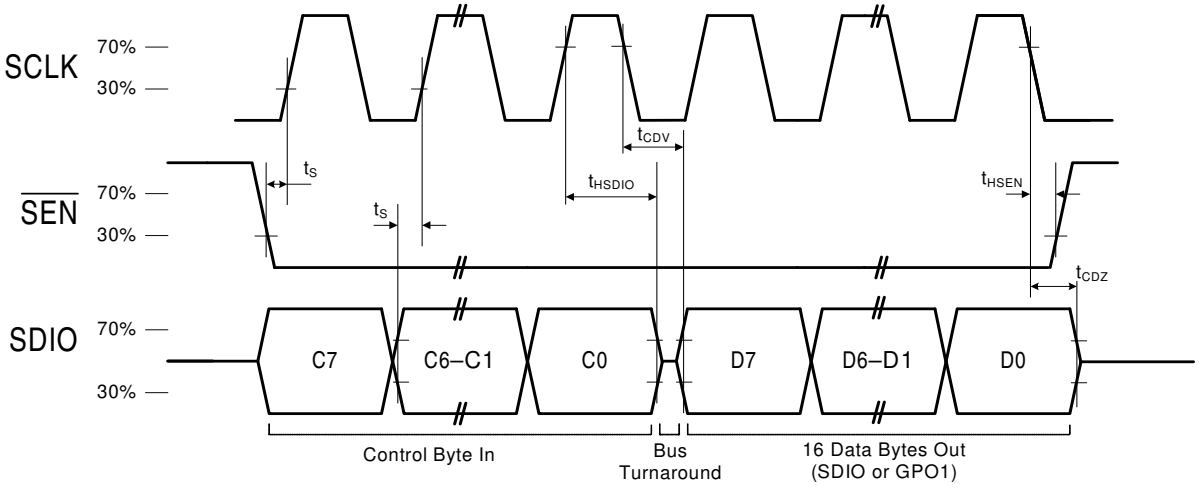


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics (Receive)
(V_{DD} = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK pulse width high	t_{DCH}		10	—	—	ns
DCLK pulse width low	t_{DCL}		10	—	—	ns
DFS set-up time to DCLK rising edge	$t_{SU:DFS}$		5	—	—	ns
DFS hold time from DCLK rising edge	$t_{HD:DFS}$		5	—	—	ns
DOUT propagation delay from DCLK falling edge	$t_{PD:DOUT}$		0	—	12	ns

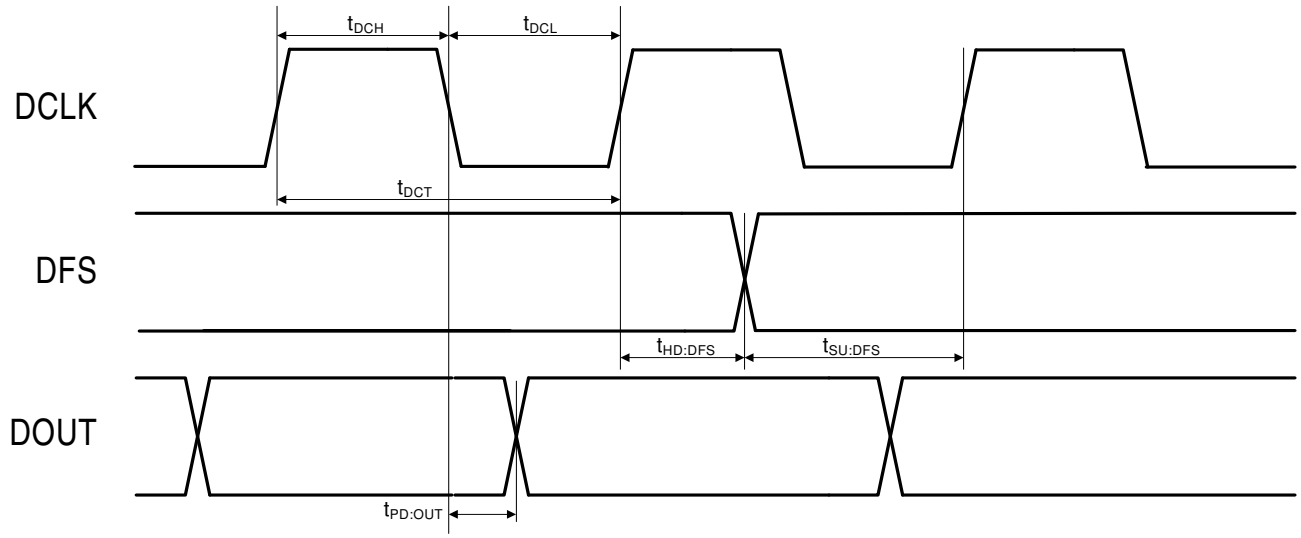


Figure 8. Digital Audio Interface Timing Parameters, I^2S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity with Headphone Network[3,4,5]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
Sensitivity with 50 Ω Network[3,4,5,6]		(S+N)/N = 26 dB	—	1.1	—	µV EMF
RDS Sensitivity[6]		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
TXO Receiver Mode Sensitivity[6]			—	3.5	—	µV EMF
LNA Input Resistance[6,7]			3	4	5	kΩ
LNA Input Capacitance[6,7]			4	5	6	pF
Input IP3[6,8]			100	105	—	dBµV EMF
AM Suppression[3,4,6,7]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[6]		In-band	35	—	—	dB
Audio Output Voltage[3,4,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,7,9]			—	—	1	dB
Audio Frequency Response Low[6]		–3 dB	—	—	30	Hz
Audio Frequency Response High[6]		–3 dB	15	—	—	kHz
Audio Stereo Separation[7,9]			25	—	—	dB
Audio Mono S/N[3,4,5,7,10]			55	63	—	dB
Audio Stereo S/N[4,5,7,10,11]			—	58	—	dB
Audio THD[3,7,9]			—	0.1	0.5	%
De-emphasis Time Constant[6]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[6,10]	R_L	Single-ended	10	—	—	kΩ

Notes:

1. Additional testing information is available in Application Note AN388. Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4720/21-GM" on page 41.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature 25 °C.

Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Output Load Capacitance[6,10]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[6]		RCLK tolerance = 100 ppm	—	—	80	ms/channel
Powerup Time[6]		From powerdown	—	—	110	ms
RSSI Offset[12]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:

1. Additional testing information is available in Application Note AN388. Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4720/21-GM" on page 41.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. At temperature 25 °C.

Table 10. FM Transmitter Characteristics[1]

Test conditions: V_{RF} = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, 75 µs pre-emphasis, unless otherwise specified.
Production test conditions: V_{DD} = 3.3 V, V_{IO} = 3.3 V, T_A = 25 °C, F_{RF} = 98 MHz.
Characterization test conditions: V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz.
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
Parameters are tested in production unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Frequency Range[2]	f_{RF}		76	—	108	MHz
Transmit Frequency Accuracy and Stability[2,3]			–3.5	—	3.5	kHz
Transmit Voltage Accuracy[2]		V_{RF} = 103–117 dBµV	–2.5	—	2.5	dB
Transmit Voltage Accuracy		V_{RF} = 102, 118 dBµV	–2.5	—	2.5	dB
Transmit Voltage Temperature Coefficient[2]			–0.075	—	–0.025	dB/°C
Transmit Channel Edge Power		> ±100 kHz, pre-emphasis off	—	—	–20	dBc
Transmit Adjacent Channel Power		> ±200 kHz, pre-emphasis off	—	–30	–26	dBc
Transmit Alternate Channel Power		> ±400 kHz, pre-emphasis off	—	–30	–26	dBc
Transmit Emissions		In-band (76–108 MHz)	—	—	–30	dBc
Output Capacitance Max[2]	C_{TUNE}		—	53	—	pF
Output Capacitance Min[2]	C_{TUNE}		—	5	—	pF
Pre-emphasis Time Constant[2]		TX_PREMPHASIS = 75 µs	70	75	80	µs
		TX_PREMPHASIS = 50 µs	45	50	54	µs
Audio SNR Mono[2]		Δf = 22.5 kHz, Mono, limiter off	58	63	—	dB
Audio SNR Stereo		Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo, limiter off	53	58	—	dB
Audio THD Mono		Δf = 75 kHz, Mono, limiter off	—	0.1	0.5	%

Notes:
1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 10 on page 19.
2. Guaranteed by characterization.
3. No measurable ΔfRF/ΔV_{DD} at ΔV_{DD} of 500 mVpk-pk at 100 Hz to 10 kHz.

Table 10. FM Transmitter Characteristics[1] (Continued)

Test conditions: V_{RF} = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, 75 µs pre-emphasis, unless otherwise specified.
Production test conditions: V_{DD} = 3.3 V, V_{IO} = 3.3 V, T_A = 25 °C, F_{RF} = 98 MHz.
Characterization test conditions: V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz.
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
Parameters are tested in production unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio THD Stereo[2]		Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo, limiter off	—	0.1	0.5	%
Audio Stereo Separation[2]		left channel only	30	35	—	dB
Sub Carrier Rejection Ratio	SCR		40	50	—	dB
Powerup Settling Time[2]			—	—	110	ms
Input Signal Level[2]	V_{AI}		—	—	0.636	V_{PK}
Frequency Flatness[2]		Mono, ±1.5 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off	30	—	15 k	Hz
High Pass Corner Frequency[2]		Mono, –3 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off	5	—	30	Hz
Low Pass Corner Frequency[2]		Mono, –3 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off	15 k	—	16 k	Hz
Audio Imbalance		Mono	–1	—	1	dB
Pilot Modulation Rate Accuracy[2]		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	–10	—	10	%
Audio Modulation Rate Accuracy[2]		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	–10	—	10	%
Input Resistance[2]		LIATTEN[1:0] = 11	50	60	—	kΩ
Input Capacitance[2]			—	10	—	pF
Received Noise Level Accuracy (Si4720/21 Only)[2]		60 dBµV input, T_A = 25 ºC	—	54	—	dBuV

Notes:
1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 10 on page 19.
2. Guaranteed by characterization.
3. No measurable $\Delta fRF/\Delta V_{DD}$ at ΔV_{DD} of 500 mVpk-pk at 100 Hz to 10 kHz.

Table 11. Digital Audio Interface Characteristics (Transmit)
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK pulse width high	t_{DCH}		10	—	—	ns
DCLK pulse width low	t_{DCL}		10	—	—	ns
DFS set-up time to DCLK rising edge	$t_{SU:DFS}$		5	—	—	ns
DFS hold time from DCLK rising edge	$t_{HD:DFS}$		5	—	—	ns
DIN set-up time from DCLK rising edge	$t_{SU:DIN}$		5	—	—	ns
DIN hold time from DCLK rising edge	$t_{HD:DIN}$		5	—	—	ns
DCLK, DFS, DIN, Rise/Fall time	t_R t_F		—	—	10	ns
DCLK Tx Frequency[1,2]			1.0	—	40.0	MHz

Notes:
1. Guaranteed by characterization.
2. The DCLK frequency may be set below the minimum specification if DIGITAL_INPUT_SAMPLE_RATE is first set to 0 (disable).

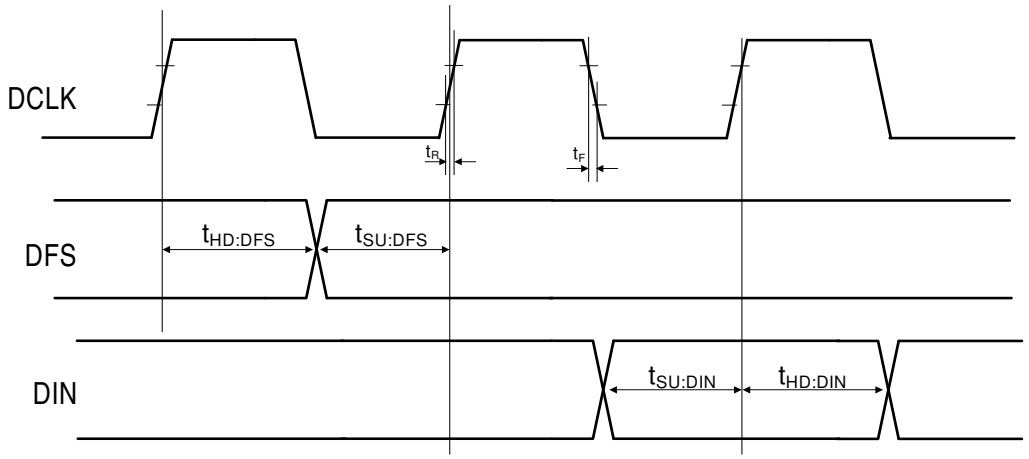


Figure 9. Digital Audio Interface Timing Parameters, I²S Mode

Table 12. FM Receive Power Scan Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tune and Signal Strength Measurement Time per Channel[2]			—	—	80	ms

Notes:
1. Settling time for ac coupling capacitors on the audio input pins after Receive to Transmit transition can take a few hundred milliseconds. The actual settling time depends on the values of the ac-coupling capacitors. Using digital audio input mode avoids this settling time.
2. Guaranteed by characterization.

Table 13. Reference Clock and Crystal Characteristics

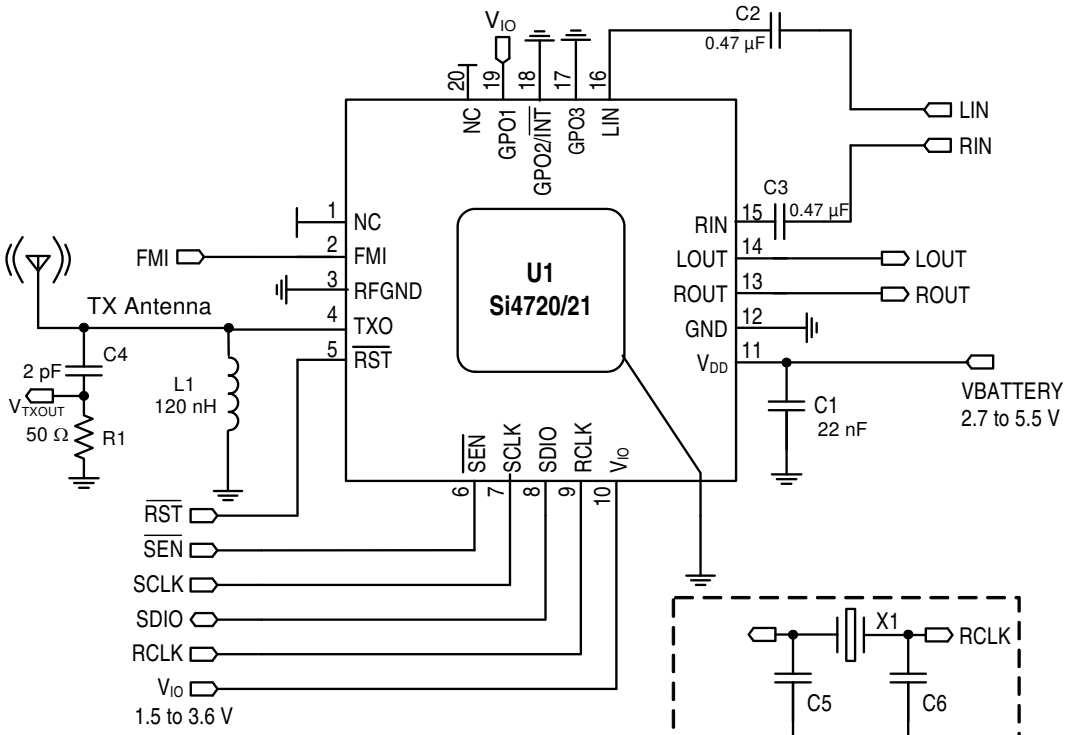
(V_{DD} = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[2]			–50	—	50	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance[2]			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF

Notes:
1. The Si4720/21 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See “AN332: Si4704/05/06/1x/2x/3x/4x FM Transmitter/AM/FM/SW/LW/WB Receiver Programming Guide” for more details.
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.

2. Test Circuit

2.1. Test Circuit Schematic



Notes:
1. Si4720/21 is shown configured in I²C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: 3 mm x 3 mm QFN Universal Layout Guide."
   Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.

Figure 10. Test Circuit Schematic

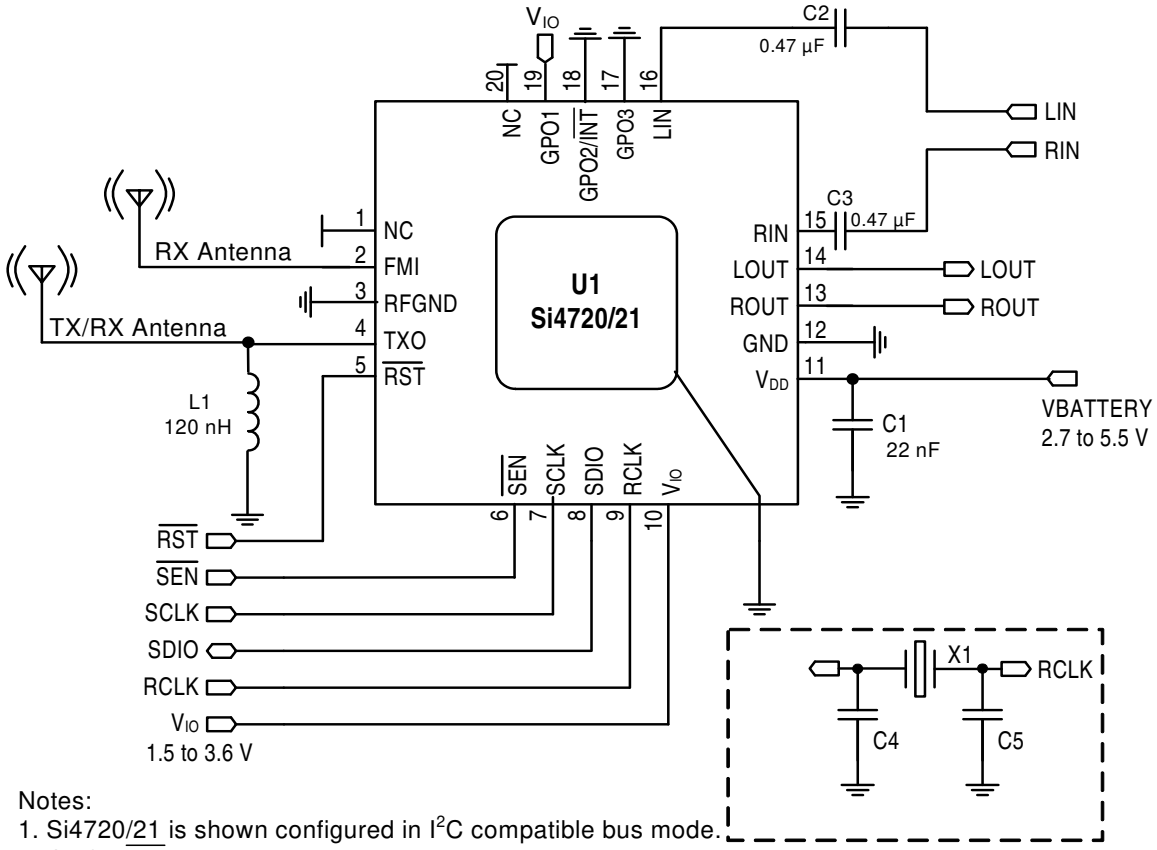
2.2. Test Circuit Bill of Materials

Table 14. Si4720/21 Test Circuit Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
C4	2 pF, ±.05 pF, 06035JZR0AB	AVX
C5, C6	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
L1	120 nH inductor, Qmin = 30	Murata
R1	49.9 Ω, 5%	Murata
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

3. Typical Application Schematic

3.1. Analog Audio Inputs/Outputs



Notes:
1. Si4720/21 is shown configured in I²C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in
   "AN383: 3 mm x 3 mm QFN Universal Layout Guide."
   Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.
5. Dedicated RX antenna at FMI input optional.

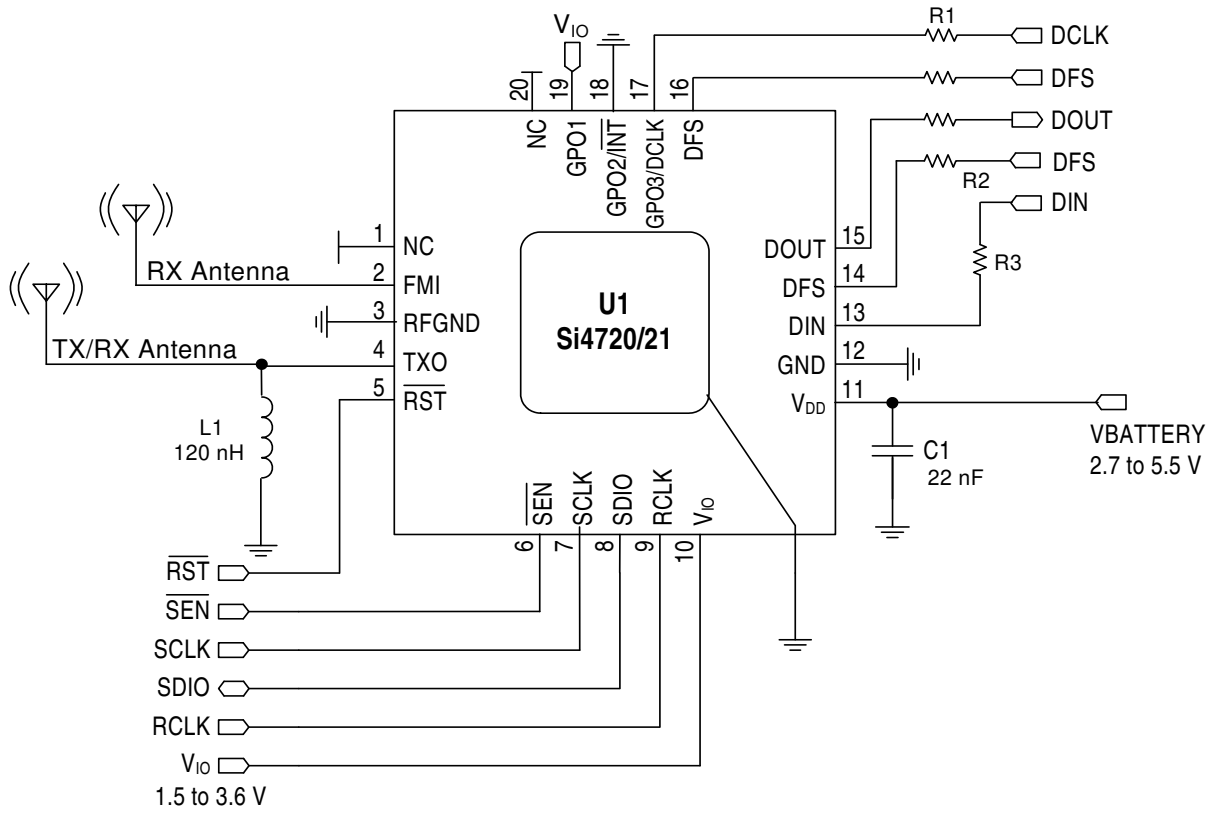
Figure 11. Analog Audio Inputs/Outputs (L_{IN}, R_{IN}, L_{OUT}, R_{OUT})

3.2. Typical Application Bill of Materials

Table 15. Si4720/21 Typical Application Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
C4, C5	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
L1	120 nH inductor, Qmin = 30	Murata
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

3.3. Digital Audio Inputs/Outputs



Notes:
1. Si4720/21 is shown configured in I^2C compatible bus mode.
2. GPO2/$\overline{INT}$ can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: Si47xx 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. Dedicated RX antenna at FMI input optional.

Figure 12. Digital Audio Inputs (DIN, DFS, DCLK)

3.4. Typical Application Schematic Bill of Materials

Table 16. Si4720/21 Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
L1	120 nH inductor, Qmin = 30	Murata
R1, R2	2 kΩ Resistor	Any
R3	600 Ω Resistor	Any
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

4. Universal AM/FM RX/FM TX Application Schematic

Figure 13 shows an application schematic that supports the Si47xx family of 3 mm x 3 mm QFN products, including the Si4702/3/4/5 FM receivers, Si471x FM transmitters, Si472x FM transceivers, and Si473x AM/FM receivers.

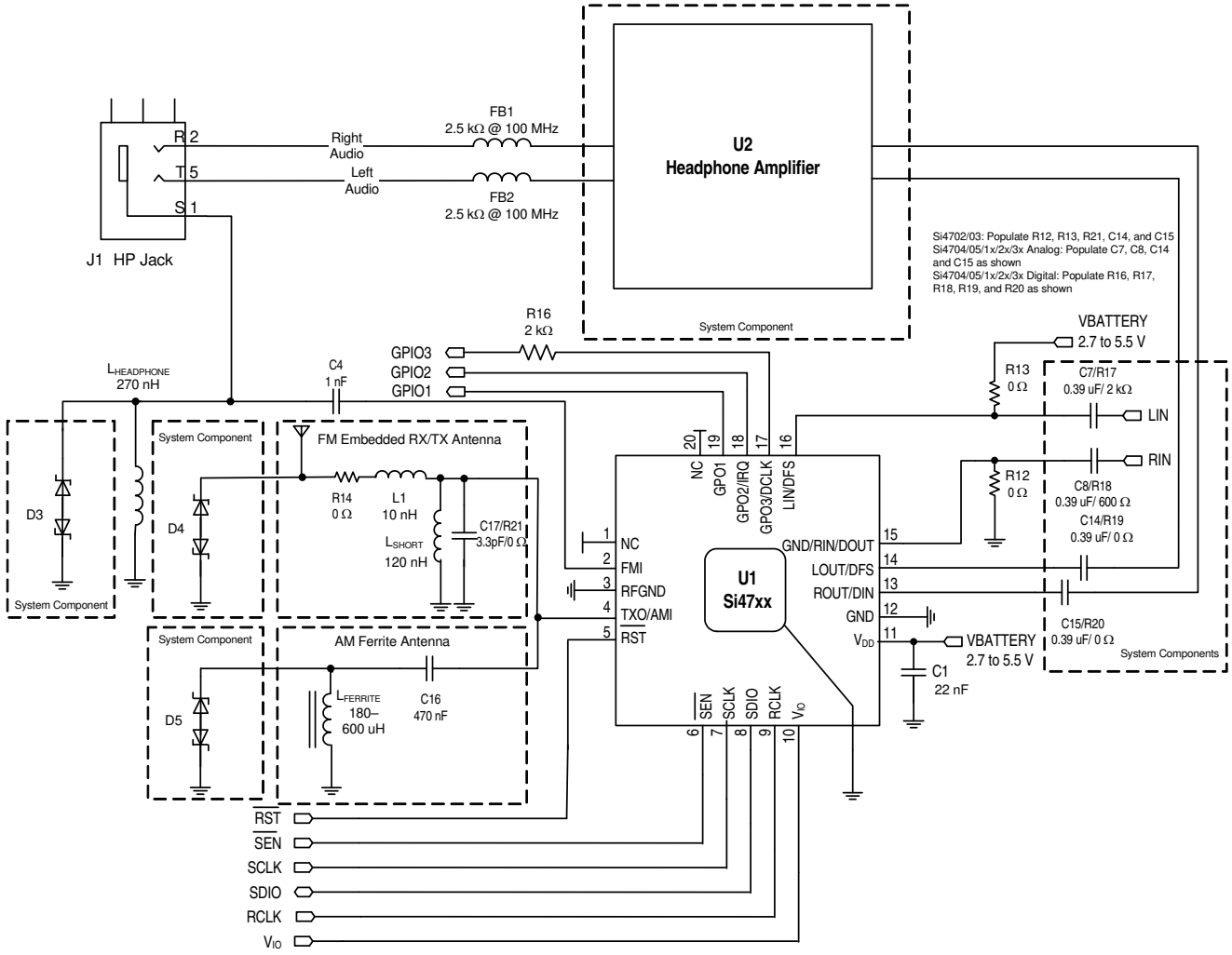


Figure 13. Universal AM/FM RX/FM TX Application Schematic

Following the schematic and layout recommendations detailed in “AN383: Universal Antenna Selection and Layout Guidelines” will result in optimal performance with the minimal application schematic shown in Figure 13. “Universal AM/FM RX/FM TX Application Schematic”. System components are those that are likely to be present for any tuner or transmitter design.

4.1. Universal AM/FM RX/FM TX Bill of Materials

The bill of materials for the expanded application schematic shown in Figure 13 is provided in Table 17. Refer to the individual device layout guides and antenna interface guides for a discussion of the purpose of each component.

Table 17. Universal AM/FM/RX/FM TX Bill of Materials

Designator	Description	Note
C1	Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402	
U1	Silicon Laboratories Si47xx, 3 mm x 3 mm, 20 pin, QFN	
R12, R13, R19, R20, R21	0 Ω jumper, 0402	R12, R13, and R21 for Si4702/03 Only
C16	AM antenna ac coupling capacitor, 470 nF, 20%, Z5U/X7R	AM Ferrite Antenna
LFERRITE	AM Ferrite loop stick, 180–600 µH	AM Ferrite Antenna
FB1,FB2	Ferrite bead, 2.5 kΩ @ 100 MHZ, 0603, Murata BLM18BD252SN1D	Headphone Antenna
LHEADPHONE	Headphone antenna matching inductor, 270 nH, 0603, Q>15, Murata LQW18ANR27J00D	Headphone Antenna
LSHORT	Embedded antenna matching inductor, 120 nH, 0603, Q>30, Murata LQW18ANR12J00D	Embedded Antenna
R14	Embedded antenna jumper, 2.2 Ω, 0402	Optional
C2	Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402	Optional
C3	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402	Optional
C5, C6	Headphone amp output shunt capacitor, 100 pF, 10%, Z5U/X7R, 0402	Optional
R7-R11	Current limiting resistor, 20 Ω–2 kΩ, 0402	Optional
C12, C13	Crystal load capacitor, 22 pF, 5%, COG	Optional
X1	Crystal, Epson FC-135	Optional
C7, C8	Si47xx input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402	System Component
D1-D5	ESD Diode, SOT23-3, California Micro Devices CM1214-01ST	System Component
C11	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402	Headphone Amplifier
C4	Headphone antenna ac coupling capacitor, 1 nF, 10%, Z5U/X7R, 0402	Headphone Antenna
C9, C10	Headphone amp output ac coupling capacitor, 125 uF, X7R, 0805	Headphone Amplifier
C14, C15	Headphone amp input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402	Headphone Amplifier
R1,R2,R3,R4	Headphone amp feedback/gain resistor, 20 kΩ, 0402	Headphone Amplifier
R5, R6	Headphone amp bleed resistor, 100 kΩ, 0402	Headphone Amplifier
U2	Headphone amplifier, National Semiconductor, LM4910MA	Headphone Amplifier
R16, R17	Current limiting resistor, 2 kΩ, 0402	System Component
R18	Current limiting resistor, 600 Ω, 0402	System Component
L1	VCO filter inductor, 10 nH, 0603, Q>30, Murata, LQW18ANR01J00D	Optional
C17	VCO filter capacitor, 3.3 pF, 0402, COG, Venkel, C0402COG2503R3JN	Optional

5. Functional Description

5.1. Overview

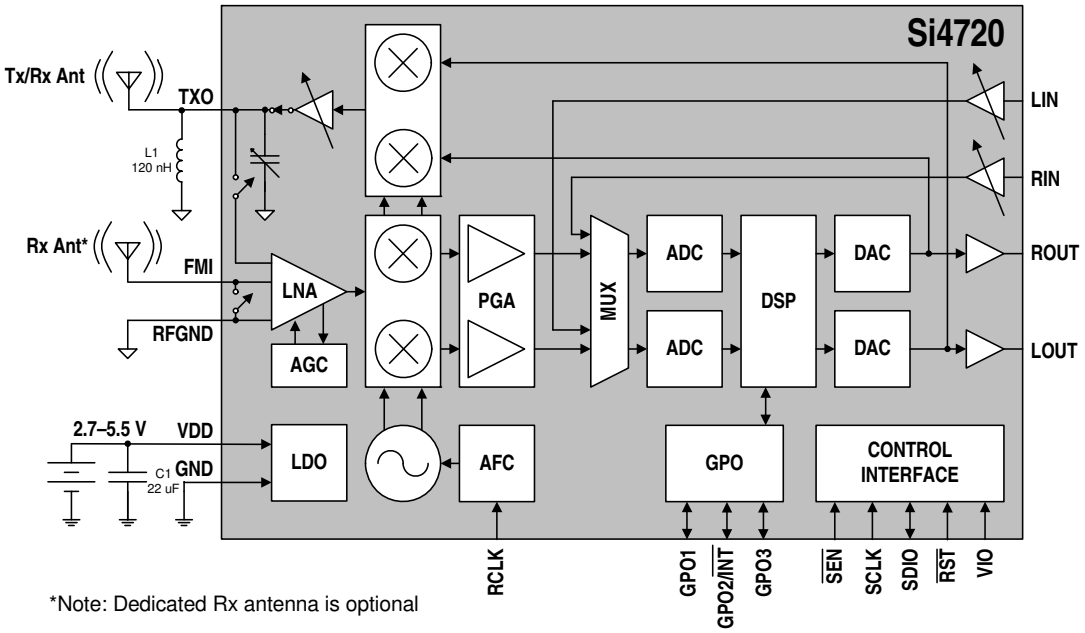


Figure 14. Functional Block Diagram

The Si4720/21 is the first single-chip FM radio transceiver. The proven and patented digital architecture of the Si4720/21 combines the functionality of the Si470x FM radio receiver with the Si471x FM transmitter, offering full FM receive and transmit capabilities in a single, ultra-small 3x3x0.55 mm QFN package. The device leverages Silicon Laboratories' highly successful and proven FM technology and offers unmatched integration and performance. FM receiver and transmit functionality may be added to any portable device by using this single chip. As with the Si470x and Si471x products, the Si4720/21 offers industry leading size, performance, low power consumption, and ease of use.

The Si4720/21 is the first FM radio transceiver integrated circuit to support a small loop antenna, which can be integrated into the enclosure or PCB of a portable device. This feature enables applications that also include Bluetooth functionality to perform FM radio reception without cables. For portable navigation devices, the Si4720's antenna architecture permits integration of the traffic messaging antenna into the enclosure of the portable device, and eliminates the need for external antenna cables.

The Si4720's digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external inductor and bypass capacitor, and a PCB space of approximately 15 mm^2. The Si4720/21 is layout compatible with Silicon Laboratories' Si470x FM radio receivers, Si473x AM/FM radio receivers, and the Si471x FM radio transmitter solutions, allowing a single PCB layout to accommodate a variety of music features. High yield manufacturability, unmatched performance, easy design-in, and software programmability are key advantages of the Si4720.

The Si4720/21's integrated receive power scan function shares the same antenna as the transmitter allowing for a compact printed circuit board design. The device operates in half duplex mode, meaning the transmitter and receiver do not operate at the same time.

The Si4720/21 performs FM modulation in the digital domain to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The onboard DSP provides modulation adjustment and audio dynamic range control for optimum sound quality.

The Si4721 supports the European Radio Data System (RDS) and the US Radio Broadcast Data System (RBDS) including all the symbol encoding, block synchronization, and error correction functions. Using this feature, the Si4721 enables data such as artist name and song title to be transmitted to an RDS/RBDS receiver.

The transmit output (TXO) connects directly to the transmit antenna with only one external inductor to provide harmonic filtering. The output is programmable over a 10 dB voltage range in 1 dB steps. The TXO output pin can also be configured for loop antenna support. Users are responsible for complying with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4720/21 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

The Si4720/21 includes a low-noise stereo line input (LIN/RIN) with programmable attenuation. To ensure optimal audio performance, the Si4720/21 has a transmit line input property that allows the user to specify the peak amplitude of the analog input required to reach maximum deviation level. The deviation levels of the audio, pilot, and RDS/RBDS signals can be independently programmed to customize FM transmitter designs. The Si4720/21 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. In addition, the device provides an overmodulation indicator to allow the user to dynamically set the maximum deviation level. The Si4720/21 has a programmable audio dynamic range control that can be used to reduce the dynamic range of the audio input signal and increase the volume at the receiver. These features can dramatically improve the end user's listening experience.

The Si4720/21 is reset by applying a logic low on the RST pin. This causes all register values to be reset to their default values. The digital input/output interface supply (V_{IO}) provides voltage to the RST, SEN, SDIO, RCLK, DIN, DFS, and DCLK pins and can be connected to the audio baseband processor's supply voltage to save power and remove the need for voltage level translators. RCLK is not required for register operation.

The Si4720/21 reference clock is programmable, supporting many RCLK inputs as shown in Table 10.

The S4720/21 are part of a family of broadcast audio solutions offered in standard, 3 x 3 mm 20-pin QFN packages. All solutions are layout compatible, allowing a single PCB to accommodate various feature offerings.

The Si4720/21 includes line inputs to the on-chip analog-to-digital converters (ADC), a programmable reference clock input, and a configurable digital audio interface. The chip supports I^2C-compliant 2-wire, 8-bit SPI, and a 3-wire control interface.

5.2. Application Schematics and Operating Modes

The application schematic for the Si4720/21 is shown in Section "3. Typical Application Schematic" on page 20. The Si4720/21 supports selectable analog, digital, or concurrent analog and digital audio output modes. In the analog output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital output mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog and digital audio output mode requires pins 13, 14, 15, 16, and 17. In addition to output mode, there is a clocking mode to clock the Si4720/21 from a reference clock or crystal oscillator. The user sets the operating modes with commands as described in Section "6. Commands and Properties" on page 36.

5.3. FM Receiver

The Si4720/21 FM receiver is based on the proven Si4700/01/02/03 FM radio receiver. The part leverages Silicon Laboratories' proven and patented Si4700/01 FM broadcast radio receiver digital architecture, delivering superior RF performance and interference rejection. The proven digital techniques provide excellent sensitivity in weak signal environments while providing superb selectivity and inter-modulation immunity in strong signal environments.

The FM receiver supports the worldwide FM broadcast band (76 to 108 MHz) with channel spacings of 50–200 kHz. The Low-IF architecture utilizes a single converter stage and digitizes the signal using a high-resolution analog-to-digital converter. The resulting digital signals are further processed through an on-chip DSP for digital channel selection, FM demodulation, and ultimately stereo audio output. The audio output can be directed either to an external headphone amplifier via analog in/out or to other system ICs through digital audio interface (I^2S).