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Si4730/31/34/35-D60

BROADCAST AM/FM/SW/LW RADIO RECEIVER

Features

- Worldwide FM band support (64–108 MHz)
- Worldwide AM band support (520–1710 kHz)
- SW band support (Si4734/35) (2.3–26.1 MHz)
- LW band support (Si4734/35) (153–279 kHz)
- Excellent real-world performance
- Integrated VCO
- Advanced AM/FM seek tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Digital FM stereo decoder
- Programmable de-emphasis
- Advanced Audio Processing
- Seven selectable AM channel filters
- AM/FM/SW/LW digital tuning
- EN55020 compliant
- No manual alignment necessary
- Programmable reference clock
- Adjustable soft mute control
- RDS/RBDS processor (Si4731/35)
- Digital audio out
- 2-wire and 3-wire control interface
- Integrated LDO regulator
- Wide range of ferrite loop sticks and air loop antennas supported
- QFN and SSOP packages
  - RoHS compliant

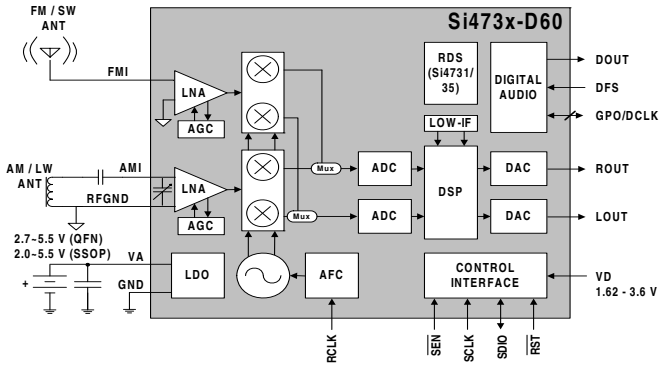
Applications

- Table and portable radios
- Mini/micro systems
- CD/DVD and Blu-ray players
- Stereo boom boxes
- Modules for consumer electronics
- Clock radios
- Mini HiFi and docking stations
- Entertainment systems

Description

The Si473x-D60 digital CMOS AM/FM radio receiver IC integrates the complete broadcast tuner and receiver function from antenna input to digital audio output. The device leverages the Silicon Labs broadcast proven digital low-IF architecture, enabling a cost-effective, digital audio platform for consumer electronic applications with high TDMA noise immunity, superior radio performance, and high fidelity audio power amplification.

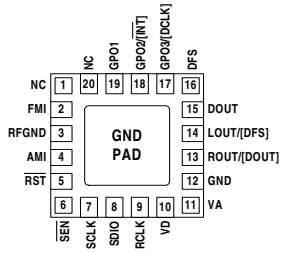
Functional Block Diagram



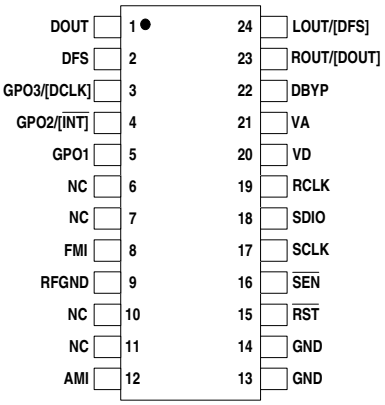
Ordering Information:
See page 31.

Pin Assignments

Si473x-D60 (QFN)



Si473x-D60(SSOP)



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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Voltage	V_A		2.7[2]	—	5.5	V
Digital and I/O Supply Voltage	V_D		1.62	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Notes:
1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at V_A = 3.3 V and 25 °C unless otherwise stated.
2. SSOP devices operate down to 2 V at 25 °C. See section “4.23. 2 V Operation (SSOP Only)” for details.

Table 2. DC Characteristics

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
V_{AQFN} Supply Current	I_{FMVA}	Digital Output Mode[1]	—	8.2	9.5	mA
V_{DQFN} Supply Current	I_{FMVD}		—	10.5	13.5	
V_{ASSOP} Supply Current	I_{FMVA}		—	18.5	21.5	
V_{DSSOP} Supply Current	I_{FMVD}		—	0.15	0.6	
V_{AQFN} Supply Current	I_{FMVA}	Analog Output Mode[2]	—	9.1	10.3	
V_{DQFN} Supply Current	I_{FMVD}		—	9.9	12.8	
V_{ASSOP} Supply Current	I_{FMVA}		—	19.1	21.3	
V_{DSSOP} Supply Current	I_{FMVD}			0.1	0.6	
AM Mode						
V_{AQFN} Supply Current	I_{AMVA}	Digital Output Mode	—	6.5	7.5	mA
V_{DQFN} Supply Current	I_{AMVD}		—	8.5	11.0	
V_{ASSOP} Supply Current	I_{AMVA}		—	14.5	16.5	
V_{DSSOP} Supply Current	I_{AMVD}		—	0.15	0.50	
V_{AQFN} Supply Current	I_{AMVA}	Analog Output Mode	—	7.5	8.5	
V_{DQFN} Supply Current	I_{AMVD}		—	8	10.2	
V_{ASSOP} Supply Current	I_{AMVA}		—	15.3	17.2	
V_{DSSOP} Supply Current	I_{AMVD}		—	0.1	0.4	
Powerdown						
V_{AQFN} Powerdown Current	I_{APD}		—	4	15	µA
V_{ASSOP} Powerdown Current			—	9.5	15	
V_{DQFN} Powerdown Current	I_{DPD}	SCLK, RCLK inactive	—	3	10	µA
V_{DSSOP} Powerdown Current		SCLK, RCLK inactive	—	3	10	
High Level Input Voltage[3]	V_{IH}		0.7 x V_D	—	V_D + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_D	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_D = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_D = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_D	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_D	V

Notes:

1. Guaranteed by characterization.
2. Backwards compatible mode to rev B and rev C. Additional features on this device may increase typical supply current.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.

Table 3. Reset Timing Characteristics[1,2,3]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}$↑[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}$↑	t_{HRST}	30	—	—	ns
$\overline{RST}$ Pulse Release time before VDD/VIO turn off	t_{RRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.
5. $\overline{RST}$ must be held low for at least 100 µs after all voltage supplies have been ramped up.
6. $\overline{RST}$ needs to be asserted (pulled low) prior to any supply voltage being ramped down.

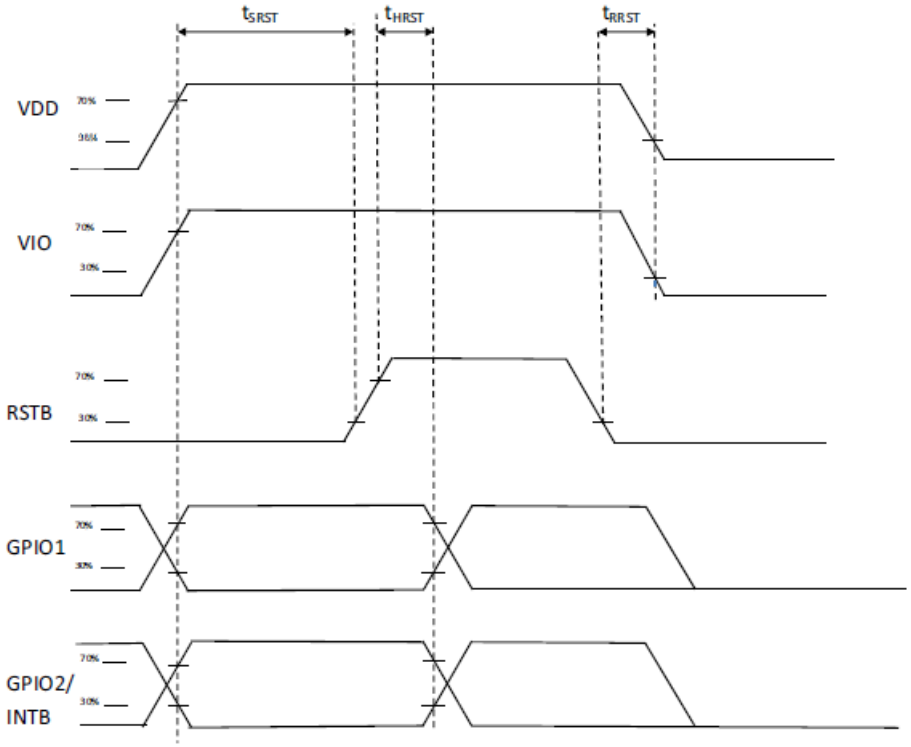


Figure 1. Reset Timing Parameters for Busmode Select

Table 4. 2-Wire Control Interface Characteristics[1,2,3]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_D = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si473x-D60 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

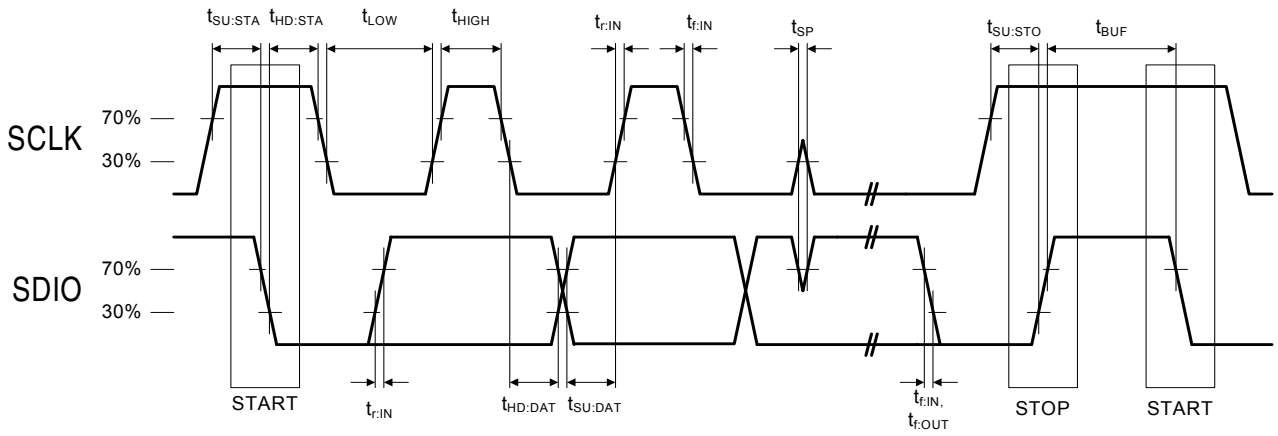


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

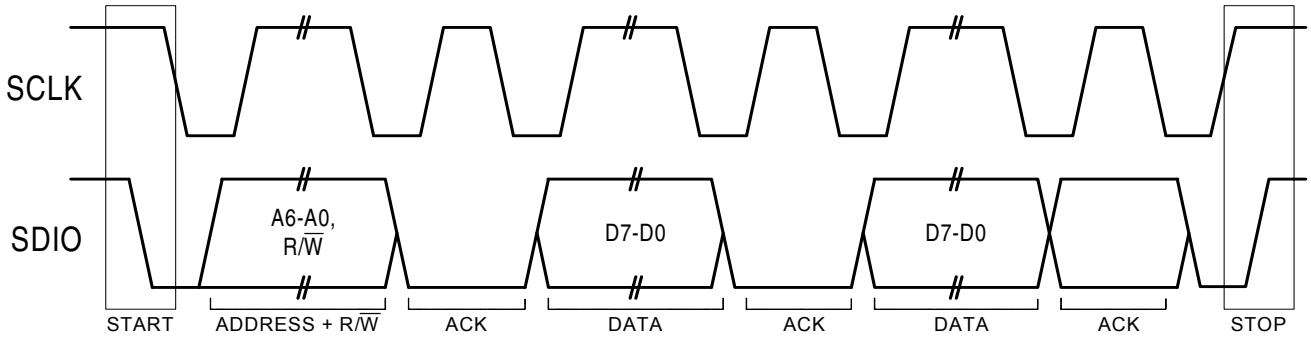


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 5. 3-Wire Control Interface Characteristics
(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

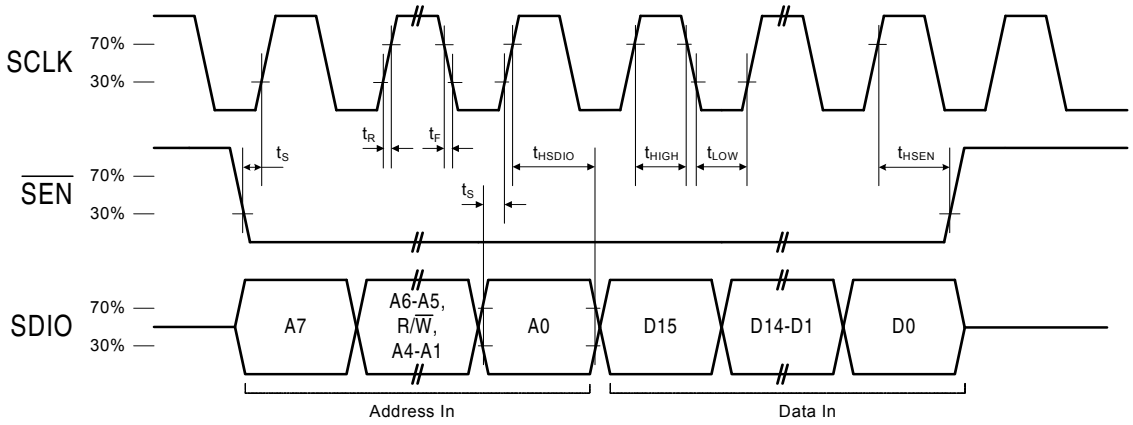


Figure 4. 3-Wire Control Interface Write Timing Parameters

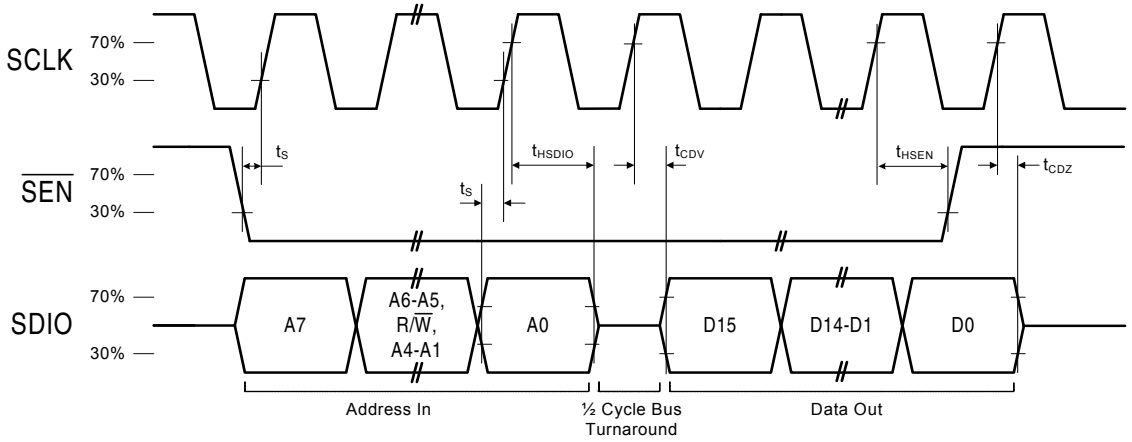


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 6. Digital Audio Interface Characteristics
(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	50	ns

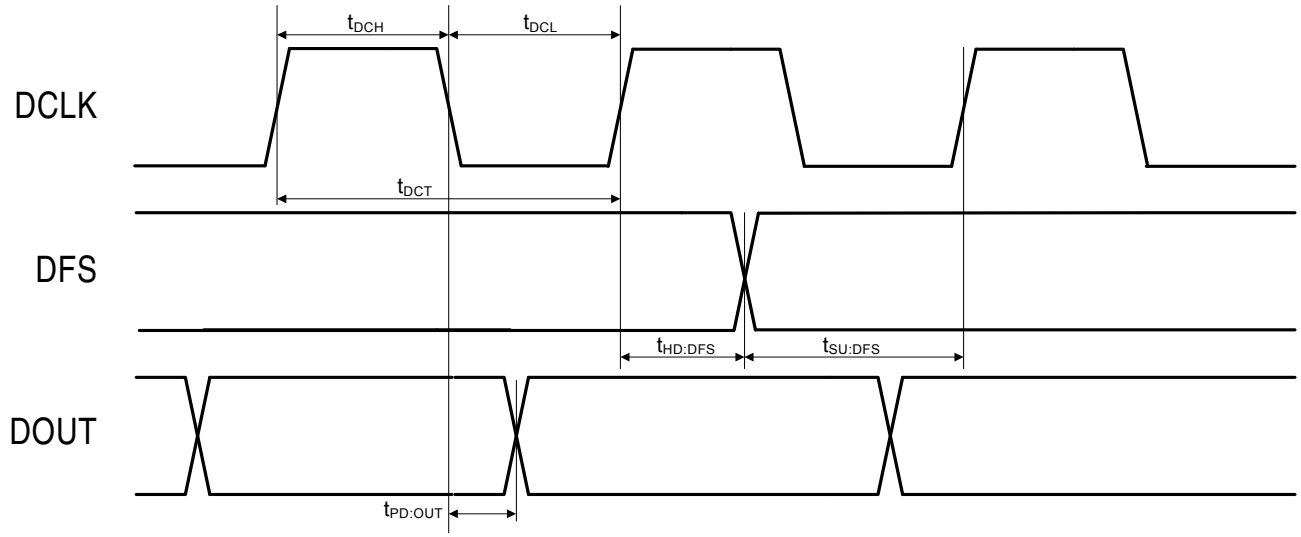


Figure 6. Digital Audio Interface Timing Parameters, I^2S Mode

Table 7. FM Receiver Characteristics[1,2]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity[3,4,5,6]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
RDS Sensitivity[6,7]		Δf = 2 kHz, RDS BLER < 5%	—	10	—	µV EMF
LNA Input Resistance[7,8]			3	4	5	kΩ
LNA Input Capacitance[7,8]			4	5	6	pF
Input IP3[7,9]			100	105	—	dBµV EMF
AM Suppression[3,4,7,8]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[7]		In-band	35	—	—	dB
Audio Output Voltage[3,4,8]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,8,10]			—	—	1	dB
Audio Frequency Response Low[7]		–3 dB	—	—	30	Hz
Audio Frequency Response High[7]		–3 dB	15	—	—	kHz
Audio Stereo Separation[8,10]			35	42	—	dB
Audio Mono S/N[3,4,5,8]			55	63	—	dB
Audio Stereo S/N[4,5,7,8]			—	58	—	dB
Audio THD[3,8,10]			—	0.1	0.5	%
De-emphasis Time Constant[7]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Blocking Sensitivity[3,4,5,6,7,11,12]		Δf = ±400 kHz	—	34	—	dBµV
		Δf = ±4 MHz	—	30	—	dBµV

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Analog audio output mode.
7. Guaranteed by characterization.
8. V_{EMF} = 1 mV.
9. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled.
10. Δf = 75 kHz.
11. Sensitivity measured at (S+N)/N = 26 dB.
12. Blocker Amplitude = 100 dBuV.
13. At temperature (25 °C).
14. At LOUT and ROUT pins.

Table 7. FM Receiver Characteristics[1,2] (Continued)

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermod Sensitivity[3,4,5,6,7,11,12]		Δf = ±400 kHz, ±800 kHz	—	40	—	dBµV
		Δf = ±4 MHz, ±8 MHz	—	35	—	dBµV
Audio Output Load Resistance[7,11,14]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[7,11,14]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[7]		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time[7]		From powerdown	—	—	110	ms
RSSI Offset[12,13]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:

1. Additional testing information is available in "AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure." Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Analog audio output mode.
7. Guaranteed by characterization.
8. V_{EMF} = 1 mV.
9. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
10. Δf = 75 kHz.
11. Sensitivity measured at (S+N)/N = 26 dB.
12. Blocker Amplitude = 100 dBuV.
13. At temperature (25 °C).
14. At LOUT and ROUT pins.

Table 8. 64–75.9 MHz Input Frequency FM Receiver Characteristics[1,2,3]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		64	—	75.9	MHz
Sensitivity[4,5,6,8]		(S+N)/N = 26 dB	—	3.5	—	µV EMF
LNA Input Resistance[3,7]			3	4	5	kΩ
LNA Input Capacitance[3,7]			4	5	6	pF
Input IP3[9]			—	105	—	dBµV EMF
AM Suppression[3,4,5,7]		m = 0.3	—	50	—	dB
Adjacent Channel Selectivity		±200 kHz	—	50	—	dB
Alternate Channel Selectivity		±400 kHz	—	70	—	dB
Audio Output Voltage[4,5,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[4,7,10]			—	—	1	dB
Audio Frequency Response Low[3]		–3 dB	—	—	30	Hz
Audio Frequency Response High[3]		–3 dB	15	—	—	kHz
Audio Mono S/N[4,3,5,7,11]			—	63	—	dB
Audio THD[4,7,10]			—	0.1	—	%
De-emphasis Time Constant		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[3,11]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[3,11]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[3]		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time[3]		From powerdown	—	—	110	ms
RSSI Offset[12]		Input levels of 8 and 60 dBµV EMF	–3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. Guaranteed by characterization.
4. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. V_{EMF} = 1 mV.
8. Analog output mode.
9. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
10. Δf = 75 kHz.
11. At LOUT and ROUT pins.
12. At temperature (25 °C).

Table 9. AM/SW/LW Receiver Characteristics[1,2]

(V_A = 2.7 to 5.5 V, V_A = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}	Long Wave (LW)	153	—	279	kHz
		Medium Wave (AM)	520	—	1710	kHz
		Short Wave (SW)	2.3	—	26.1	MHz
Sensitivity[3,4,5]		(S+N)/N = 26 dB	—	25	35	µV EMF
Large Signal Voltage Handling[5,6]		THD < 8%	—	300	—	mV_{RMS}
Power Supply Rejection Ratio[5]		ΔV_{DD} = 100 mV_{RMS}, 100 Hz	—	40	—	dB
Audio Output Voltage[3,7]			54	60	67	mV_{RMS}
Audio S/N[3,4,7]			—	60	—	dB
Audio THD[3,7]			—	0.1	0.5	%
Antenna Inductance[5,8]		Long Wave (LW)	—	2800	—	µH
		Medium Wave (AM)	180	—	450	µH
Powerup Time[5]		From powerdown	—	—	110	ms

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 520 kHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. FMOD = 1 kHz, 30% modulation, 2 kHz channel filter.
4. B_{AF} = 300 Hz to 15 kHz, A-weighted.
5. Guaranteed by characterization.
6. See “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure” for evaluation method.
7. V_{IN} = 5 mVrms.
8. Stray capacitance on antenna and board must be < 10 pF to achieve full tuning range at higher inductance levels.

Table 10. Reference Clock and Crystal Characteristics

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[2]			–100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance[2]			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF
ESR			—	—	50	kΩ
CL[3]			7	12	22	pF
CL–single ended[3]			14	24	44	pF

Notes:
1. The Si473x-D60 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. For more details, see Table 6 of “AN332: Si47xx Programming Guide”.
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing and AM seek/tune in SW frequencies.
3. Guaranteed by characterization.

Table 11. Thermal Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	—	80	—	°C/W
Ambient Temperature	T_A	–20	25	85	°C
Junction Temperature	T_J	—	—	92	°C

***Note:** Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.

Table 12. Absolute Maximum Ratings[1,2]

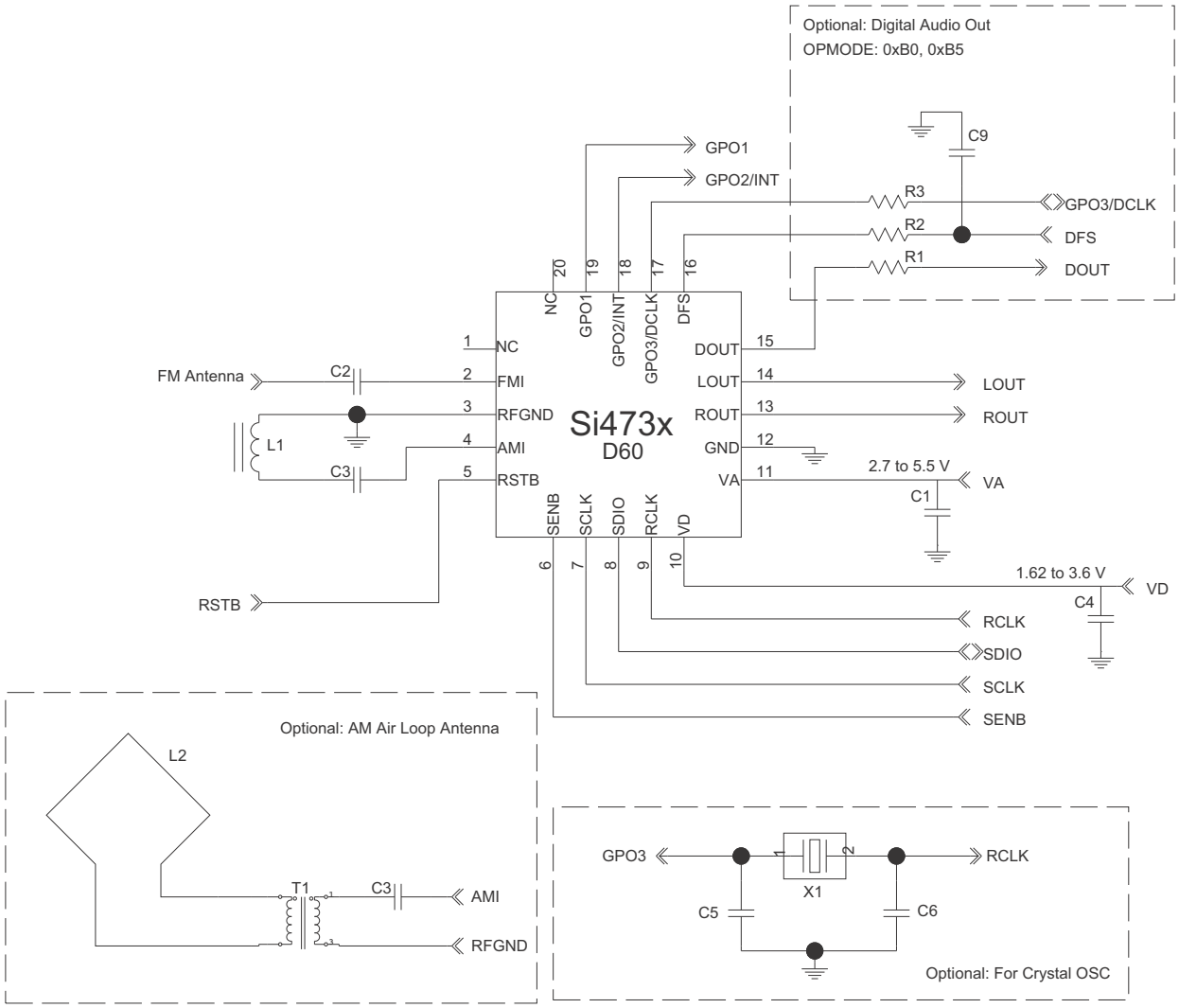
Parameter	Symbol	Value	Unit
Analog Supply Voltage	V_A	–0.5 to 5.8	V
Digital and I/O Supply Voltage	V_D	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pk}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si473x-D60 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins DFS, SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2, GPO3, and DCLK.
4. At RF input pins FMI and AMI.

2. Typical Application Schematic

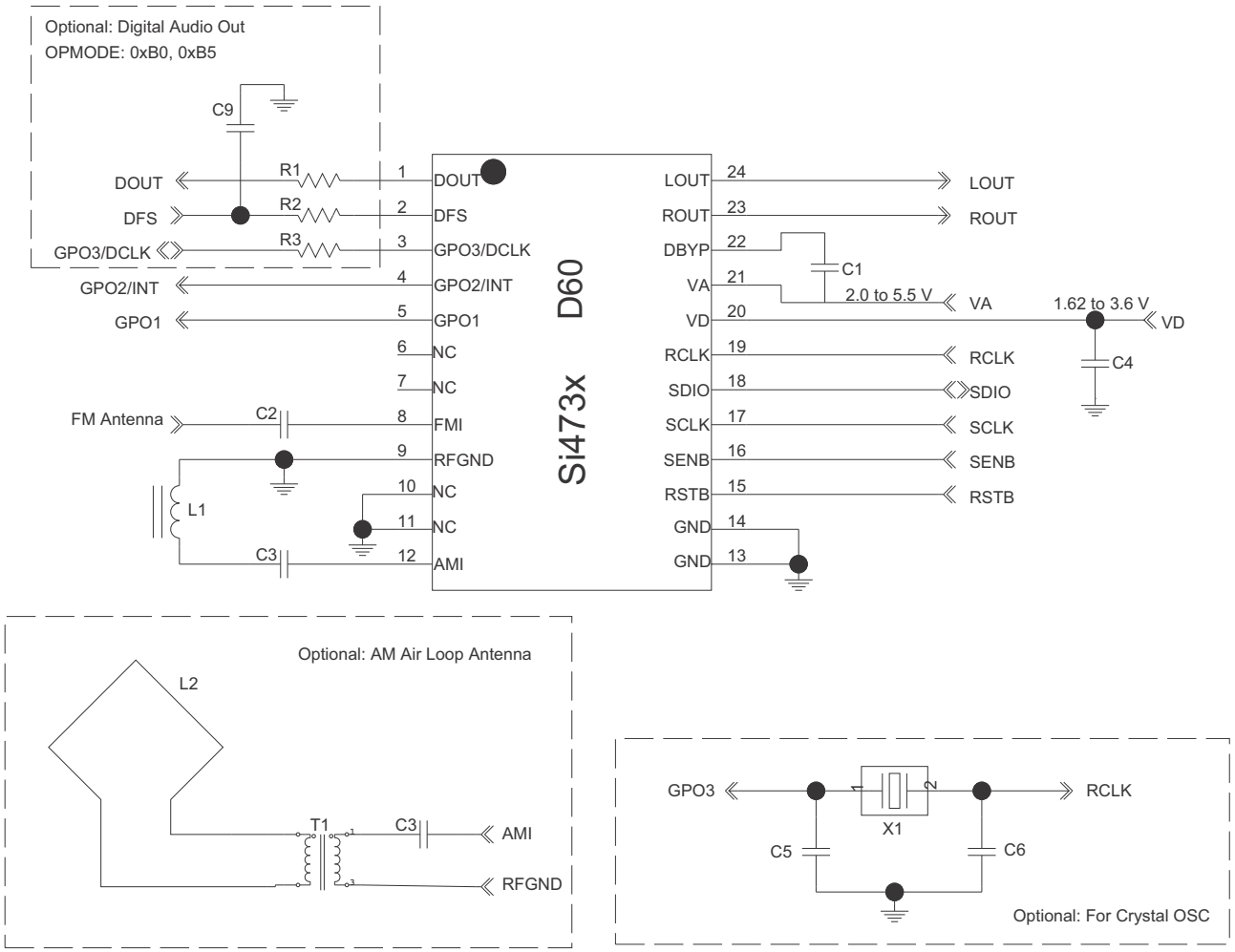
2.1. QFN Typical Application Schematic



Notes:

1. Place C1 close to VA pin and C4 close to VD pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the FM antenna interface, and pin 4 connects to the AM antenna interface.
6. Place Si473x-D60 as close as possible to antenna and keep the FMI and AMI traces as short as possible.

2.2. SSOP Typical Application Schematic



Notes:

1. Place C1 close to VA and C4 close to VD pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 6 and 7 are no connects, leave floating.
4. Pins 10 and 11 are unused. Tie these pins to GND.
5. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
6. Pin 8 connects to the FM antenna interface, and pin 12 connects to the AM antenna interface.
7. Place Si473x-D60 as close as possible to antenna and keep the FMI and AMI traces as short as possible.

3. Bill of Materials

3.1. QFN/SSOP Bill of Materials

Table 13. Si473x-D60 QFN/SSOP Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
C2	Coupling capacitor, 1 nF, ±20%, Z5U/X7R	Murata
C3	Coupling capacitor, 0.47 µF, ±20%, Z5U/X7R	Murata
C4	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R	Murata
L1	Ferrite loop stick, 180–450 µH	Jiaxin
U1	Si47xx AM/FM Radio Tuner	Silicon Laboratories
Optional Components		
C5, C6	Crystal load capacitors, 22 pF, ±5%, COG (Optional for crystal oscillator)	Venkel
C9	Noise mitigating capacitor, 2~5 pF (Optional for digital audio)	Murata
R1	Resistor, 600 Ω (Optional for digital audio)	Venkel
R2	Resistor, 2 kΩ (Optional for digital audio)	Venkel
R3	Resistor, 2 kΩ (Optional for digital audio)	Venkel
L2	Air Loop, 10-20 µH (Optional for AM Input)	Jiaxin
T1	Transformer, 1:5 turns ratio (Optional for AM Input)	Jiaxin, UMEC
X1	32.768 kHz crystal (Optional for crystal oscillator)	Epson

4. Functional Description

4.1. Overview

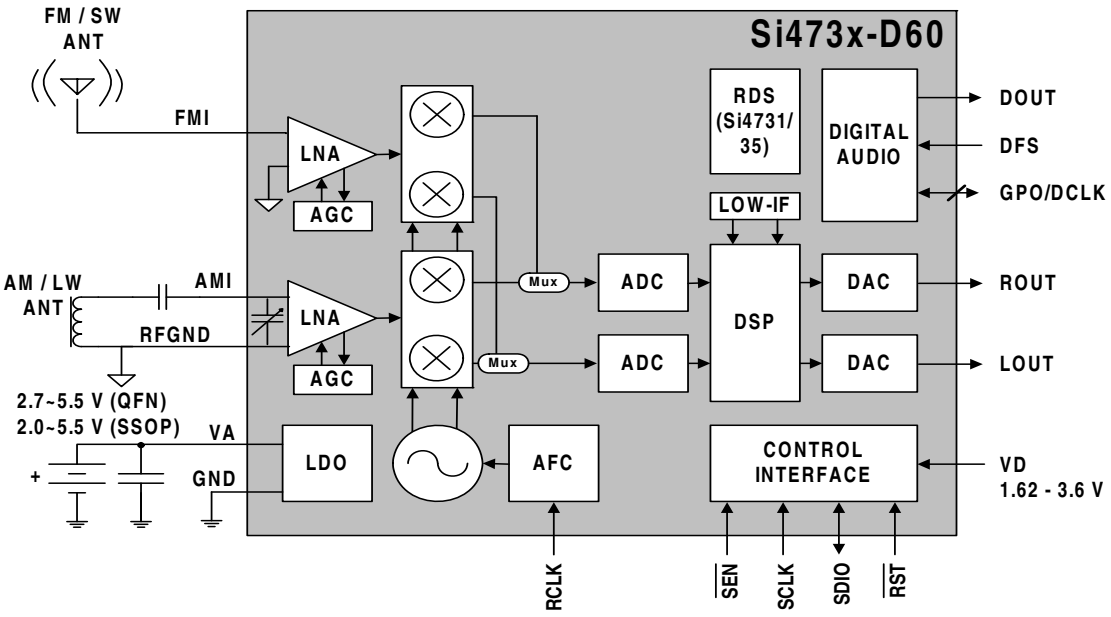


Figure 7. Functional Block Diagram

The Si473x-D60 digital CMOS AM/FM radio receiver IC integrates the complete broadcast tuner and receiver function from antenna input to digital audio output. The device leverages the Silicon Labs broadcast proven digital low-IF architecture, enabling a cost-effective digital audio platform for consumer electronic applications with high TDMA noise immunity, superior radio performance, and high fidelity audio power amplification. Offering unmatched integration and PCB space savings, the Si473x-D60 requires only a few external components and less than 15 mm^2 of board area, excluding the antenna inputs. The Si473x-D60 AM/FM radio provides the space savings and low power consumption necessary for portable devices while delivering the high performance and design simplicity desired for all AM/FM solutions.

Leveraging Silicon Laboratories' proven and patented Si4700/01 FM tuner's digital low intermediate frequency (low-IF) receiver architecture, the Si473x-D60 delivers superior RF performance and interference rejection in the AM, FM, SW, and LW bands. The high level of integration and complete system production test simplifies design-in, increases system quality, and improves reliability and manufacturability.

The Si473x-D60 is a feature-rich solution that includes advanced seek algorithms, soft mute, auto-calibrated digital tuning, FM stereo processing and advanced audio processing.

In addition, the Si473x-D60 provides analog and digital audio outputs and a programmable reference clock. The device supports I^2C-compatible 2-wire control interface, and a Si4700/01 backwards-compatible 3-wire control interface.

The Si473x-D60 utilizes digital signal processing to achieve high fidelity, optimal performance, and design flexibility. The chip provides excellent pilot rejection, selectivity, and unmatched audio performance, and offers both the manufacturer and the end-user extensive programmability and a better listening experience.

The Si4731/35 incorporates a digital signal processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions. Using this feature, the Si4731/35 enables broadcast data such as station identification and song name to be displayed to the user.

4.2. Operating Modes

The Si473x-D60 operates in either an FM receive or AM receive modes. In FM mode, radio signals are received on FMI and processed by the FM front-end circuitry. In AM mode, radio signals are received on AMI and processed by the AM front-end circuitry. In addition to the receiver mode, there is a clocking mode to choose to clock the Si473x-D60 from a reference clock or crystal. On the Si473x-D60, there is an audio output mode to choose between an analog and/or digital audio output. In the analog audio output mode, ROUT and LOUT are used for the audio output pins. In the digital audio mode, DOUT, DFS, and DCLK pins are used. Concurrent analog/digital audio output mode is also available requiring all five pins.

4.3. FM Receiver

The Si473x-D60 FM receiver is based on the proven Si4700/01 FM tuner. The receiver uses a digital low-IF architecture allowing the elimination of external components and factory adjustments. The Si473x-D60 integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (64 to 108 MHz). An AGC circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the Si473x-D60 to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

4.4. AM Receiver

The highly-integrated Si473x-D60 supports worldwide AM band reception from 520 to 1710 kHz using a digital low-IF architecture with a minimum number of external components and no manual alignment required. This digital low-IF architecture allows for high-precision filtering offering excellent selectivity and SNR with minimum variation across the AM band. The DSP also provides adjustable channel step sizes in 1 kHz increments, AM demodulation, soft mute, seven different channel bandwidth filters, and additional features, such as a programmable automatic volume control (AVC) maximum gain allowing users to adjust the level of background noise.

Similar to the FM receiver, the integrated LNA and AGC optimize sensitivity and rejection of strong interferers allowing better reception of weak stations.

The Si473x-D60 provides highly-accurate digital AM tuning without factory adjustments. To offer maximum flexibility, the receiver supports a wide range of ferrite loop sticks from 180–450 µH. An air loop antenna is supported by using a transformer to increase the effective inductance from the air loop. Using a 1:5 turn ratio inductor, the inductance is increased by 25 times and easily supports all typical AM air loop antennas which generally vary between 10 and 20 µH.

4.5. SW Receiver

The Si4734/35 is the first fully integrated IC to support AM and FM, as well as short wave (SW) band reception from 2.3 to 26.1 MHz fully covering the 120 meter to 11 meter bands. The Si4734/35 offers extensive shortwave features such as continuous digital tuning with minimal discrete components and no factory adjustments. Other SW features include adjustable channel step sizes in 1 kHz increments, adjustable channel bandwidth settings, advanced seek algorithm, and soft mute.

The Si4734/35 uses the FM antenna to capture short wave signals. These signals are then fed directly into the AMI pin in a wide band configuration. See "AN332: Si47xx Programming Guide” and “AN383: Si47xx Antenna and Schematic Guidelines" for more details.

4.6. LW Receiver

The Si4734/35 supports the long wave (LW) band from 153 to 279 kHz. The highly integrated Si4734/35 offers continuous digital tuning with minimal discrete components and no factory adjustments. The Si4734/35 also offers adjustable channel step sizes in 1 kHz increments, adjustable channel bandwidth settings, advanced seek algorithm, and soft mute.

The Si4734/35 uses a separate ferrite bar antenna to capture long wave signals.

4.7. Digital Audio Interface

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si473x-D60 supports a number of industry-standard sampling rates including 32, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

4.7.1. Audio Data Formats

The digital audio interface operates in slave mode and supports three different audio data formats:

- I2S
- Left-Justified
- DSP Mode

In I2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In left-justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties. The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.7.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

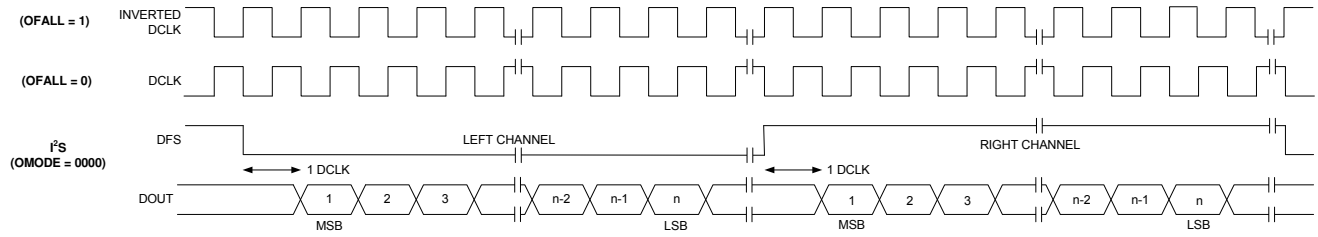


Figure 8. I2S Digital Audio Format

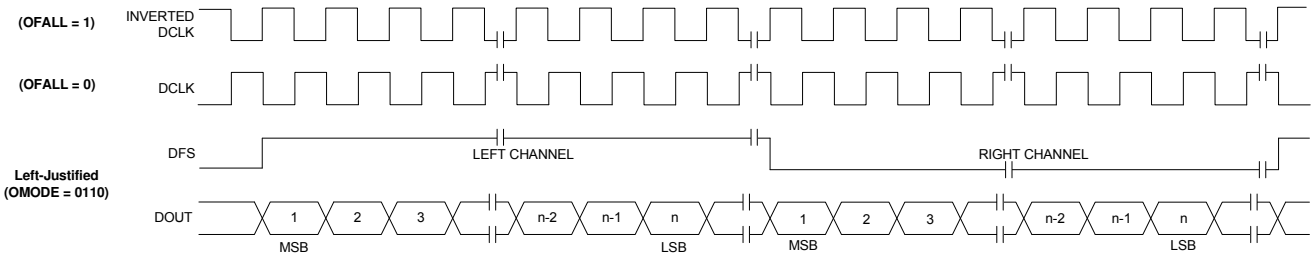


Figure 9. Left-Justified Digital Audio Format

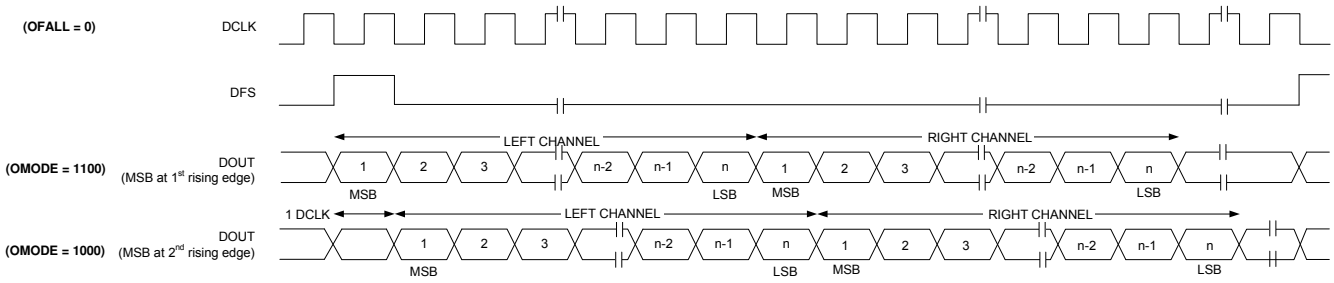


Figure 10. DSP Digital Audio Format

4.8. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 11 below.

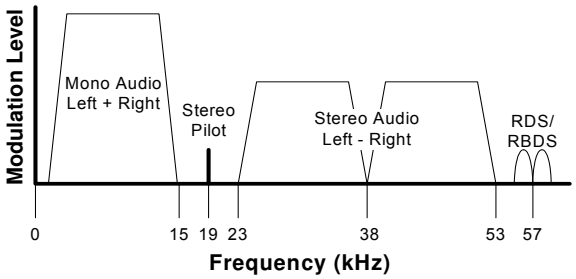


Figure 11. MPX Signal Spectrum

4.8.1. Stereo Decoder

The Si473x-D60's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

4.8.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Three metrics, received signal strength indicator (RSSI), signal-to-noise ratio (SNR), and multipath interference, are monitored simultaneously in forcing a blend from stereo to mono. The metric which reflects the minimum signal quality takes precedence and the signal is blended appropriately.

All three metrics have programmable stereo/mono thresholds and attack/release rates. If a metric falls below its mono threshold, the signal is blended from stereo to full mono. If all metrics are above their respective stereo thresholds, then no action is taken to blend the signal. If a metric falls between its mono and stereo thresholds, then the signal is blended to the level proportional to the metric's value between its mono and stereo thresholds, with an associated attack and release rate.

4.9. Received Signal Qualifiers

The quality of a tuned signal can vary depending on many factors including environmental conditions, time of day, and position of the antenna. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si473x-D60 monitors and provides indicators of the signal quality, allowing the host processor to perform additional processing if required by the customer. The Si473x-D60 monitors signal quality metrics including RSSI, SNR, and multipath interference on FM signals. These metrics are used to optimize signal processing and are also reported to the host processor. The signal processing algorithms can use either Silicon Labs' optimized settings (recommended) or be customized to modify performance.

4.10. Volume Control

The audio output may be muted. Volume is adjusted digitally by the RX_VOLUME property.

4.11. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted.

4.12. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The soft mute feature is triggered by the SNR metric. The SNR threshold for activating soft mute is programmable, as are soft mute attenuation levels and attack and release rates.

4.13. FM Hi-Cut Control

Hi-cut control is employed on audio outputs with degradation of the signal due to low SNR and/or multipath interference. Two metrics, SNR and multipath interference, are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for both metrics. The transition frequency for hi-cut is also programmable with up to seven hi-cut filter settings. A single set of attack and release rates for hi-cut are programmable for both metrics from a range of 2 ms to 64 s. The level of hi-cut applied can be monitored with the FM_RSQ_STATUS command. Hi-cut can be disabled by setting the hi-cut filter to audio bandwidth of 15 kHz.