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# Si4770/77-A20

# HIGH-PERFORMANCE CONSUMER ELECTRONICS BROADCAST RADIO RECEIVER AND HD RADIO TUNER

## Features

- Worldwide FM band support (64–108 MHz)
- Worldwide AM band support (520–1710 kHz)
- AM/FM HD Radio support (Si4777 only)
- Comprehensive signal quality metrics: RSSI, SNR, multipath interference, frequency offset, adjacent channel RSSI, frequency deviation, and image RSSI
- Advanced patented RDS soft-decision decoder
- Advanced, patented FM channel equalizer for multipath interference
- Dynamic AM/FM channel bandwidth control
- Programmable AM/FM soft mute
- FM stereo-mono blend
- FM hi-blend control
- AM/FM hi-cut control
- AM lo-cut filter
- L/R analog and digital ($I^2S$) audio outputs
- Digital Low-IF architecture
- Frequency synthesizer with fully integrated PLL-VCO
- Fully integrated AM/FM front-end including high performance LNA, AGC with integrated resistor and capacitor banks, and RF and IF peak detectors
- Integrated crystal oscillator
- Digital ($I^2S$) Zero-IF AM/FM I/Q outputs (Si4777 only)
- 1.2 to 5 V power supplies
- QFN 40-pin, 6x6x0.85 mm
  - Pb-free/RoHS compliant

## Applications

- Audio/video receivers
- Consumer electronics
- Boom boxes
- Home theater systems

## Description

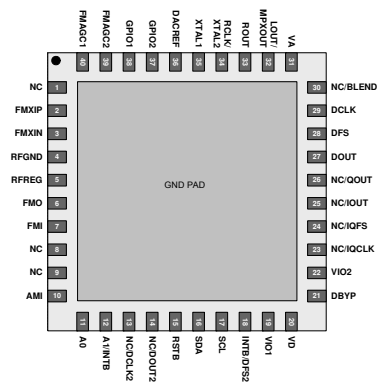
The Si4770/77-A20 broadcast receiver and HD Radio tuner (Si4777 only) employs an advanced, proven digital low-IF architecture to bring outstanding receiver performance to high-performance consumer electronics.


**Ordering Information:**

See page 49.

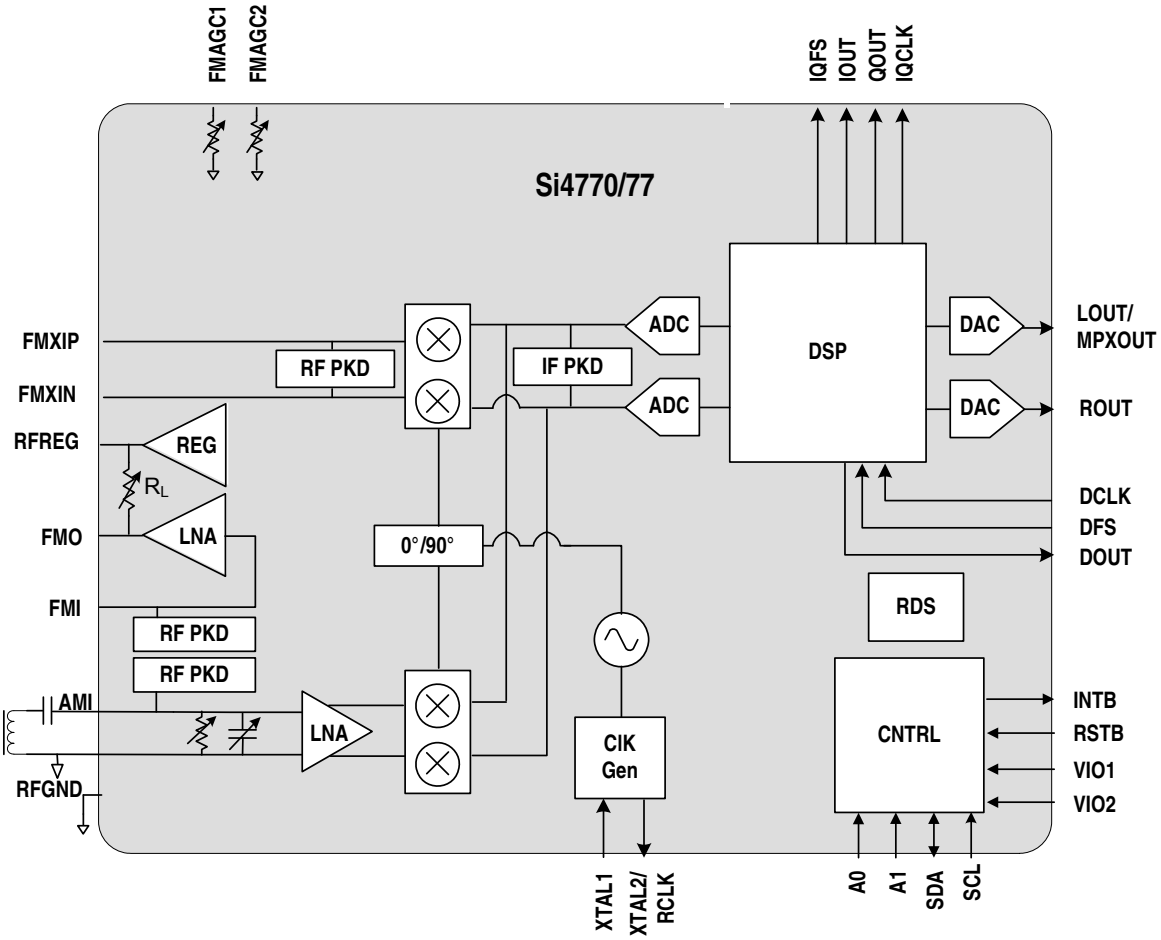
**Pin Assignments**

**Si4770/77-A20**




Patents pending

## Functional Block Diagram



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**Section** **Page**

# 1. Electrical Specifications

### Table 1. Recommended Operation Conditions*

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Analog Supply Voltage | $V_A$ | — | 4.5 | 5 | 5.5 | V |
| Digital Supply Voltage | $V_D$ | — | 2.7 | 3.3 | 3.6 | V |
| Interface Supply Voltage | $V_{IO1}$ | — | 1.7 | 3.3 | 3.6 | V |
| | $V_{IO2}$ | — | 1.2 | 3.3 | 3.6 | V |

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_D$ = 3.3 V, $V_{IO1}$ = 3.3 V, $V_{IO2}$ = 3.3 V, $V_A$ = 5 V, and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

### Table 2. DC Characteristics

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FM Mode** | | | | | | |
| Total Supply Power | | | 671 | 850 | 1049 | mW |
| $V_A$ Supply Current | $I_{VA}$ | | 121 | 130 | 139 | mA |
| $V_D$ Supply Current | $I_{VD}$ | | 47 | 60 | 79 | mA |
| $V_A$ Supply Power Down Current | $I_{VA}$ | | 20 | 90 | 170 | µA |
| $V_D$ Supply Power Down Current | $I_{VD}$ | | 5 | 20 | 50 | µA |
| **AM Mode** | | | | | | |
| Total Supply Power | | | 707 | 900 | 1100 | mW |
| $V_A$ Supply Current | $I_{VA}$ | | 129 | 140 | 147 | mA |
| $V_D$ Supply Current | $I_{VD}$ | | 47 | 60 | 81 | mA |
| $V_A$ Supply Power Down Current | $I_{VA}$ | | 20 | 90 | 170 | µA |
| $V_D$ Supply Power Down Current | $I_{VD}$ | | 5 | 20 | 50 | µA |

***Note:** See "7. I2C Control Bus" on page 44.

**Table 2. DC Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Interface Supplies** | | | | | | |
| $V_{IO1}$ Supply Current | $I_{VIO1}$ | | 0.1 | 0.5 | 0.82 | mA |
| $V_{IO2}$ Supply Current | $I_{VIO2}$ | | 0.1 | 0.2 | 0.5 | mA |
| $V_{IO1}$ Supply Power Down Current* | $I_{PD}$ | | 150 | 250 | 420 | µA |
| $V_{IO2}$ Supply Power Down Current* | $I_{PD}$ | | 5 | 20 | 150 | µA |
| **Inputs Pins SCL, SDA, RSTB, A0, A1** | | | | | | |
| High Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{IO1}$ | — | — | V |
| Low Level Input Voltage | $V_{IL}$ | | — | — | 0.3x$V_{IO1}$ | V |
| High Level Input Current | $I_{IH}$ | $V_{IN}$ = $V_{I01}$ = 3.6 V | –10 | — | 10 | µA |
| Low Level Input Current | $I_{IL}$ | $V_{IN}$ = 0 = V, $V_{I01}$ = 3.6 V | –10 | — | 10 | µA |
| **Input Pins DCLK, DFS** | | | | | | |
| High Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{IO2}$ | — | — | V |
| Low Level Input Voltage | $V_{IL}$ | | — | — | 0.3 x $V_{IO2}$ | V |
| High Level Input Current | $I_{IH}$ | $V_{IN}$ = $V_{I02}$ = 3.6 V | –10 | — | 10 | µA |
| Low Level Input Current | $I_{IL}$ | $V_{IN}$ = 0 V, $V_{I02}$ = 3.6 V | –10 | — | 10 | µA |
| **Input Pins GPIO1, GPIO2** | | | | | | |
| High Level Input Voltage | $V_{IH}$ | GPIO1 and GPIO2 are internally regulated at 3.6 V | 2.52 | — | — | V |
| Low Level Input Voltage | $V_{IL}$ | | — | — | 1.08 | V |
| High Level Input Current | $I_{IH}$ | $V_{IN}$ = 3.6 V | –10 | — | 10 | µA |
| Low Level Input Current | $I_{IL}$ | $V_{IN}$ = 0 V | –10 | — | 10 | µA |
| **Output Pins INTB** | | | | | | |
| High Level Output Voltage | $V_{OH}$ | Output is common drain output with internal 10 kΩ pull-up to $V_{IO1}$ | 0.8x$V_{IO1}$ | — | — | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OUT}$ = –500 µA | — | — | 0.2x$V_{IO1}$ | V |

***Note:** See "7. I2C Control Bus" on page 44.

**Table 2. DC Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Output Pins SDA** | | | | | | |
| High Level Output Voltage | $V_{OH}$ | Output is common drain output with external 4.7 kΩ pull-up to $V_{IO1}$ | 0.8x$V_{IO1}$ | — | — | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OUT}$ = –500 µA | — | — | 0.2x$V_{IO1}$ | V |
| **Output Pins GPIO1, GPIO2** | | | | | | |
| High Level Output Voltage | $V_{OH}$ | GPIO1 and GPIO2 are internally regulated at 3.6 V, IOUT = +500 µA | 2.88 | — | — | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OUT}$ = –500 µA | — | — | 0.72 | V |
| **Output Pins IQCLK, IQFS, IOUT, QOUT, DFS, DCLK, DOUT** | | | | | | |
| High Level Output Voltage | $V_{OH}$ | $I_{OUT}$ = 500 µA | 0.8 x $V_{IO2}$ | — | — | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OUT}$ = –500 µA | — | — | 0.2 x $V_{IO2}$ | V |
| ***Note:** See "7. I2C Control Bus" on page 44. | | | | | | |

**Table 3. Digital Audio Interface Characteristics***

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DCLK Input Cycle Time | $t_{CYC:\ DCLK}$ | | 70 | — | — | ns |
| DCLK Input Pulse Width High | $t_{HI:\ DCLK}$ | | 0.4 x $t_{CYC:DCLK}$ | — | 0.6 x $t_{CYC:DCLK}$ | ns |
| DCLK Input Pulse Width Low | $t_{LO:\ DCLK}$ | | 0.4 x $t_{CYC:DCLK}$ | — | 0.6 x $t_{CYC:DCLK}$ | ns |
| DFS Setup Time | $t_{SU:DFS}$ | | 10 | — | — | ns |
| DFS Hold Time | $t_{HD:DFS}$ | | 5 | — | — | ns |
| DOUT ouTput Delay | $t_{PD:DOUT}$ | | 0 | — | 35 | ns |
| Capacitive Loading | $C_B$ | $VIO_2 \leq 1.33$ V | — | — | 10 | pF |
| | | $VIO_2 > 1.33$ V | — | — | 15 | |

***Note:** Guaranteed by characterization.

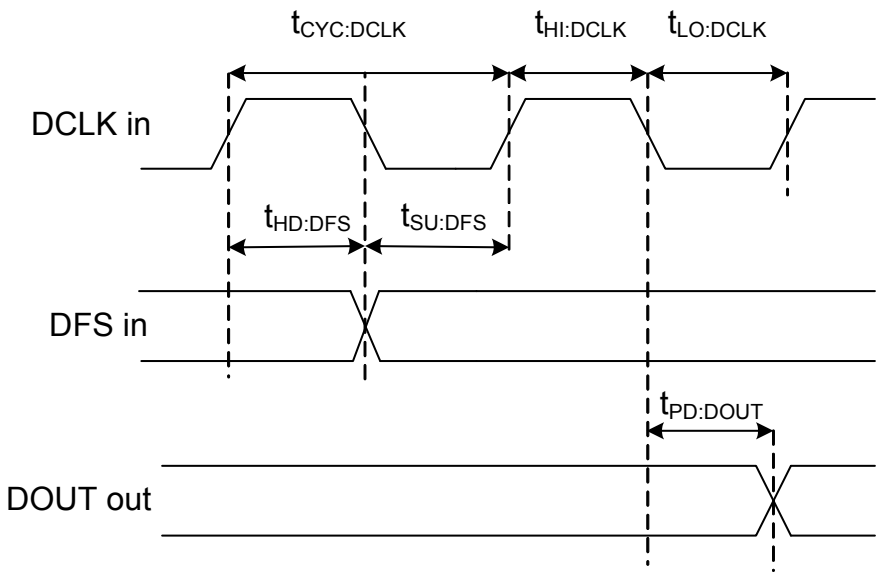


**Figure 1. Digital Audio**

**Table 4. Digital Zero-IF I/Q Interface Characteristics (Si4777 Only)[1]**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IQCLK Output Cycle Time | $t_{CYC:IQCLK}$ | | 0.8 x per | per[2] | 1.2 x per | ns |
| IQCLK Output Pulse Width High | $t_{HI:IQCLK}$ | | 0.22 x per | — | 0.59 x per | ns |
| IQCLK Output Pulse Width Low | $t_{LO:IQCLK}$ | | 0.41 x per | — | 0.78 x per | ns |
| IQFS Output Delay | $t_{PD:IQFS}$ | | 0 | — | (0.5 x per) + 18 | ns |
| IQFS Output Setup to IQCLK Rise[3] | $t_{SU:IQFS}$ | | (0.5 x per) – 18 | — | — | ns |
| IOUT Output Delay | $t_{PD:IOUT}$ | | 0 | — | (0.5 x per) + 18 | ns |
| QOUT Output Delay | $t_{PD:QOUT}$ | | 0 | — | (0.5 x per) + 18 | ns |
| IOUT Output Setup to IQCLK rise[3] | $t_{SU:IOUT}$ | | (0.5 x per) – 18 | — | — | ns |
| QOUT Output Setup to IQCLK Rise[3] | $t_{SU:QOUT}$ | | (0.5 x per) – 18 | — | — | ns |

**Notes:**
1. Guaranteed by characterization.
2. per is the IQCLK I/Q bit clock period. Refer to Table 15 on page 35 for IQCLK bit clock frequencies.
3. Minimum time the Si4770/77-A20 will produce between valid output and the next rising edge of IQCLK

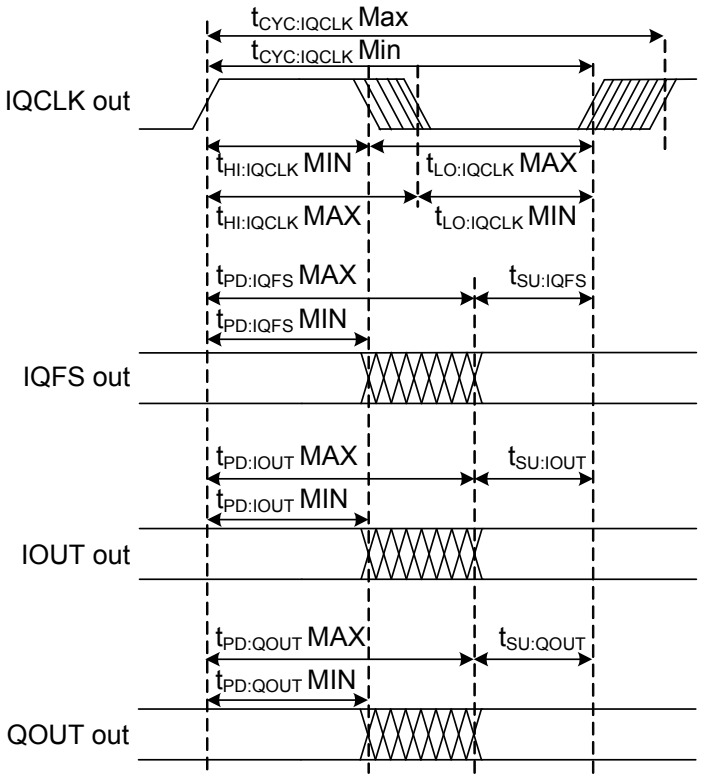


**Figure 2. Digital Zero-IF I/Q**

**Table 5. Reference Clock and Crystal Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Reference Clock, Pin RCLK** | | | | | | |
| RCLK Supported Frequencies | | | — | 36.4<br>37.8<br>37.209375 | — | MHz |
| RCLK Frequency Tolerance | | | –100 | — | 100 | ppm |
| **RCLK = 36.4 MHz, 37.8 MHz, 37.209375 MHz** | | | | | | |
| Phase Noise | | 100 Hz offset | — | — | –86 | dBc/Hz |
| | | 1 kHz offset | — | — | –101 | dBc/Hz |
| | | 10 kHz offset | — | — | –108 | dBc/Hz |
| | | ≥ 100 kHz offset | — | — | –122 | dBc/Hz |
| Input Capacitance | | | — | 7 | — | pF |
| Input Voltage | | AC coupling capacitor = 1 µF<br>Square wave input | | | 400 | $mV_{PP}$ |
| | | AC coupling capacitor = 1 µF<br>Sine wave input | 300 | — | 900 | $mV_{PP}$ |
| **Crystal Oscillator, Pins XTAL1, XTAL2** | | | | | | |
| Crystal Frequency | | | — | 36.4<br>37.8<br>37.209375 | — | MHz |
| Crystal Frequency Tolerance | | | –100 | — | 100 | ppm |
| Load Capacitance, Programmable, Each Pin to GND | | | 5 | — | 21.8 | pF |

### Table 6. I²C Control Interface Characteristics

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Pins SCL, SDA** | | | | | | |
| SCL Frequency | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCL Low Time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SCL Input to SDA ↓ Setup (START) | $t_{SU:STA}$ | | 0.6 | — | — | µs |
| SCL Input from SDA ↓ Hold (START) | $t_{HD:STA}$ | | 0.6 | — | — | µs |
| SDA Input to SCL ↑ Setup | $t_{SU:DAT}$ | | 100 | — | — | ns |
| SDA Input from SCL ↓ Hold | $t_{HD:DAT}$ | | 0 | — | 900 | ns |
| SDA Output Delay | $t_{PD:DAT}$ | | 300 | — | 900 | ns |
| SCL Input to SDA ↑ Setup (STOP) | $t_{SU:STO}$ | | 0.6 | — | — | µs |
| STOP to START Time | $t_{BUF}$ | | 1.3 | — | — | µs |
| SDA Output Fall Time | $t_{f:OUT}$ | | $20 + 0.1\frac{C_B}{1pF}$ | — | 250 | ns |
| SDA Input, SCL Rise/Fall Time | $t_{f:IN}$, $t_{r:IN}$ | | $20 + 0.1\frac{C_B}{1pF}$ | — | 300 | ns |
| Capacitive Loading | $C_B$ | | — | — | 50 | pF |
| Pulse Width Rejected by Input Filter | $t_{SP}$ | | — | — | 50 | ns |

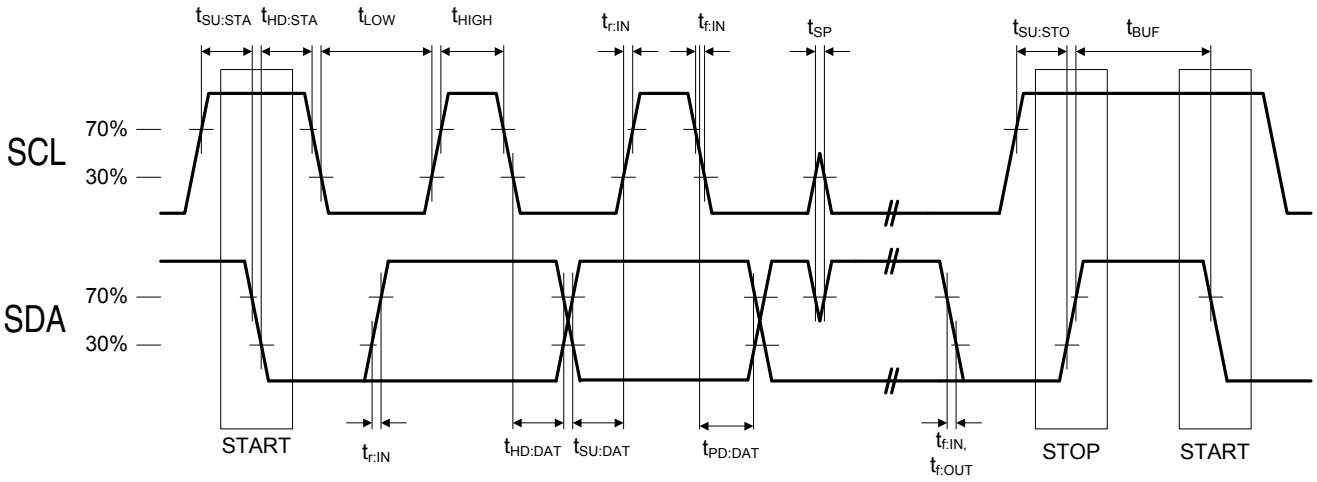


**Figure 3. I²C Control Interface Read and Write Timing Parameters**

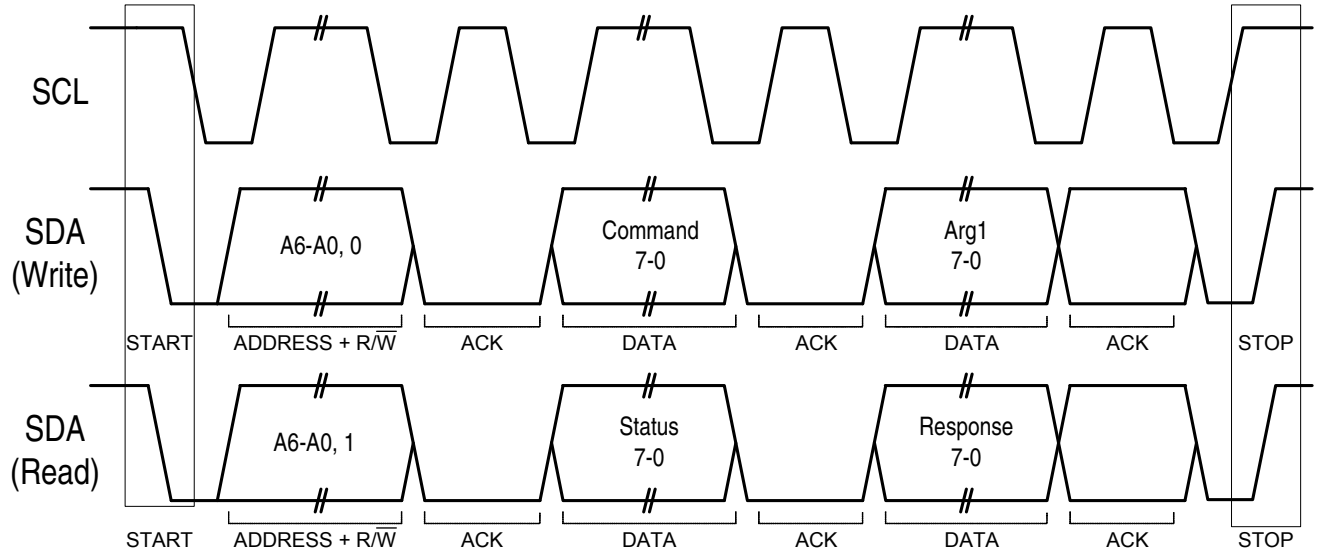


**Figure 4. I²C Control Interface Read and Write Timing Diagram**

### Table 7. FM Receiver Characteristics

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, FM modulation (L = R), $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and $F_{RF}$ = 98 MHz in application circuit unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Frequency | | 64 | — | 108 | MHz |
| Frequency Step Resolution | | 10 | — | 200 | kHz |
| Powerup Time[1,2] | RCLK or Crystal = 36.4 MHz, 37.8 MHz, 37.209375 MHz | — | — | 100 | ms |
| Tune time[1] | | — | 1.5 | — | ms |
| Seek Time/Channel[1] | At LOUT and ROUT pins | — | 20 | — | ms |
| Max Frequency Deviation[1] | Audio THD <1%, over-deviation handling enabled | — | 150 | — | kHz |
| RF AGC Range | | — | 40 | — | dB |
| AGC Gain Resolution[3] | | — | 2 | — | dB |
| RF AGC Threshold Accuracy[3] | | | 2 | — | dB |
| IF AGC Threshold Accuracy[3] | | | 1 | — | dB |
| **Following FM Receiver Specifications Refer to Si4770/77-A20 Application Circuit Input** | | | | | |
| IP3[6] | Blockers at 400/800 kHz offset AGC disabled (Max RF gain) | 115 | 117 | — | dBµV |
| Sensitivity[6] | Audio SINAD = 26 dB AGC disabled (Max RF gain) | — | –3.5 | –2 | dBµV |
| Image Rejection[1] | Deviation = 22.5 kHz | 65 | 70 | — | dB |
| Adjacent Channel Rejection[1,6] | Audio SINAD = 26 dB Desired = 40dBµV, $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz Undesired at ±100 kHz offset, $F_{MOD}$ = 400 Hz, $F_{DEV}$ = 22.5 kHz | 63 | 65 | — | dB |

**Notes:**

1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

**Table 7. FM Receiver Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, FM modulation (L = R), $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and $F_{RF}$ = 98 MHz in application circuit unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Alternate Channel Rejection[6] | Audio SINAD = 26 dB<br>Desired = 40 dBµV, $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz<br>Undesired at ±200 kHz offset, $F_{MOD}$ = 400 Hz, $F_{DEV}$ = 22.5 kHz | 65 | 72 | — | dB |
| THD | $F_{DEV}$ = 75 kHz | — | 0.05 | 0.1 | % |
| Mono (S+N)/N[6] | | 66 | 75 | — | dB |
| Stereo (S+N)/N[6] | Stereo modulation (L = 1, R = 0), deviation = 67.5 kHz, pilot deviation = 6.75 kHz | 64 | 70 | — | dB |
| AM Suppression[1] | AM: m = 0.3/Fmod = 1 kHz, RF level = 60 dBµV | 50 | 55 | — | dB |
| De-Emphasis Time Constant[3] | | 70 | 75 | 80 | µsec |
| | | 45 | 50 | 54 | µsec |
| L/R Imbalance | Deviation = 75 kHz | –1 | — | 1 | dB |
| Stereo Separation | Stereo modulation (L = 1, R = 0), Deviation = 67.5 kHz, pilot deviation = 6.75 kHz | 40 | 43 | — | dB |
| Stereo THD | Stereo modulation (L = 1, R = 0), Deviation = 67.5 kHz, pilot deviation = 6.75 kHz | — | 0.1 | 0.2 | % |
| Pilot Signal Rejection[1] | Stereo modulation (L = 1, R = 0), Deviation = 67.5 kHz, pilot deviation = 6.75 kHz | — | 55 | — | dB |
| RDS Sensitivity[1] | Δf = 2 kHz, RDS BLER < 5% | — | 13 | 14.5 | dBµV |
| RDS Synchronization Time[1] | Δf = 2 kHz<br>RF input = 60 dBµV | — | 70 | — | ms |
| RDS PI Lock Time[1] | Δf = 2 kHz<br>RF input = 60 dBµV | — | 85 | — | ms |

**Notes:**

1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

**Table 7. FM Receiver Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, FM modulation (L = R), $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and $F_{RF}$ = 98 MHz in application circuit unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **FM Mixer Inputs: Pins FMXIP, FMXIN** | | | | | |
| Maximum RF Input Voltage[3] | 1 dB compression point of mixer | — | 112 | — | dBµV |
| Mixer Input Resistance[3] | | — | 8 | — | kΩ |
| Mixer Input Capacitance[3] | | — | 6 | — | pF |
| IP3[4,5,6] | Blockers at 400/800 kHz offset, Max Gain (AGC disabled) | — | 123 | — | dBµV |
| Sensitivity[5,6] | Audio SINAD = 26 dB Max Gain (AGC disabled) | — | 3.5 | — | dBµV |
| **FM Resistor Banks: FMAGC1, FMAGC2** | | | | | |
| FMAGC1 Min | | — | 2.5 | — | Ω |
| FMAGC1 Max | | — | 800 | — | Ω |
| FMAGC1 Step Size | Maximum parallel resistance change | — | 800 | — | Ω |
| FMAGC2 Min | | — | 2.5 | — | Ω |
| FMAGC2 Max | | — | 800 | — | Ω |
| FMAGC2 Step Size | Maximum parallel resistance change | — | 800 | — | Ω |
| **FM LNA: Pins FMI, FMO** | | | | | |
| **Single Receiver Mode** | | | | | |
| FMI Input Resistance[3,7] | | — | 50 | — | Ω |
| FMI Input Capacitance[3] | | — | 2 | — | pF |
| FMI Return Loss[3] | 64 MHz < F < 108 MHz | — | 15 | — | dB |
| FMI Input Referred Noise[3] | | — | 0.73 | — | $nV/\sqrt{Hz}$ |
| FMI LNA IP3[3,8] | Blockers at 400/800 kHz offset, Max Gain | — | 128 | — | dBµV |

**Notes:**

1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

**Table 7. FM Receiver Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, FM modulation (L = R), $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and $F_{RF}$ = 98 MHz in application circuit unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FMO Output Resistance[3] | Nominal FMI to FMO gain = 8 dB, Source load = 50 Ω | — | 125 | — | Ω |
| FMO Output Capacitance[3] | | — | 2 | — | pF |
| **Dual Receiver Mode** | | | | | |
| FMI Input Resistance[7,3] | | — | 100 | — | Ω |
| FMI Input Capacitance[3] | | — | 1.5 | — | pF |
| FMI Return Loss[3] | 64 MHz < F < 108 MHz | — | 15 | — | dB |
| FMI Input Referred Noise[3] | | — | 1.20 | — | nV/$\sqrt{Hz}$ |
| FMI LNA IP3[3,8] | Blockers at 400/800 kHz offset, Max Gain | — | 126 | — | dBµV |
| FMO Output Resistance[3] | Nominal FMI to FMO gain = 8dB, Source load = 50 Ω | — | 250 | — | Ω |
| FMO Output Capacitance[3] | | — | 2 | — | pF |
| **Audio Outputs: Pins LOUT and ROUT** | | | | | |
| Audio Frequency Response Low[1,2] | ±3 dB | — | — | 30 | Hz |
| Audio Frequency Response High[1,2] | ±3 dB | 15 | — | — | kHz |
| Output Load Resistance[3] | At LOUT and ROUT pins | 10 k | — | — | Ω |
| Output Load Capacitance[3] | At LOUT and ROUT pins | — | — | 50 | pF |
| Output Voltage | Deviation = 22.5 kHz | 99 | 112 | 125 | mVRMS |
| Power Supply Rejection Ratio (PSRR)[3] | 100 Hz ripple on power supply lines. Ripple voltage = 100 $mV_{PP}$ of power supply voltage | — | 45 | — | dB |

**Notes:**

1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

**Table 7. FM Receiver Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, FM modulation (L = R), $F_{MOD}$ = 1 kHz, $F_{DEV}$ = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and $F_{RF}$ = 98 MHz in application circuit unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **FM MPX Output: Pins MPXOUT** | | | | | |
| Output Voltage[1] | $F_{RF}$ = 83 MHz, RF level = 65 dBµV, $F_{DEV}$ = 3 kHz, $F_{MOD}$ = 76 kHz unless otherwise noted | 14 | 16 | — | mVRMS |
| Output Load Resistance[3] | | — | 10 | — | kΩ |
| Output Load Capacitance[3] | | — | 50 | — | pF |
| PSRR[3] | 100 Hz ripple on power supply lines. Ripple voltage = 100 $mV_{PP}$ of power supply voltage | — | 45 | — | dB |
| Bandwidth[1] | | 110 | — | — | kHz |
| **Following FM MPX Specifications Refer to Si4770/77-A20 Application Circuit** | | | | | |
| (S+N)/N[1,11] | $F_{RF}$ = 83 MHz, RF level = 65 dBµV, $F_{DEV}$ = 3 kHz, $F_{MOD}$ = 76 kHz unless otherwise noted | 25 | 30 | — | dB |
| Sensitivity[1,11] | $F_{RF}$ = 83 MHz, $F_{DEV}$ = 3 kHz, $F_{MOD}$ = 76 kHz unless otherwise noted, SINAD = 5 dB | — | 19 | 25 | dBµV |

**Notes:**

1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

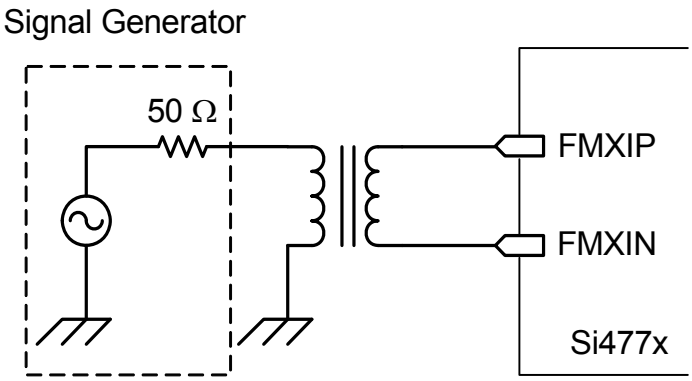


**Figure 5. FM Test Circuit for Mixer Input IP3 and Sensitivity Measurement**

### Table 8. AM Receiver Characteristics

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, AM modulation = 30%, $F_{MOD}$ = 1 kHz, RF level = 74 dBµV, and $F_{RF}$ = 1 MHz unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Frequency | | 520 | — | 1710 | kHz |
| Frequency Step Resolution | | 1 | — | 10 | kHz |
| Powerup Time[1,2] | RCLK or Crystal = 36.4 MHz, 37.8 MHz, 37.209375 MHz | — | — | 100 | ms |
| Tune Time[1] | | — | 15 | — | ms |
| Seek Time/Channel[1] | At LOUT and ROUT pins | — | 55 | — | ms |
| Maximum RF Input Voltage[1,2] | Mod = 90%, Fmod = 1 kHz, SINAD = 57 dB | — | 93 | — | dBµV |
| Image Rejection[1,3] | | 68 | 72 | — | dB |
| Adjacent Channel Rejection[1,3] | SINAD = 20 dB<br>Desired = 40 dBµV, $F_{MOD}$ = 1 kHz, MOD = 30%<br>Undesired at ±9 kHz offset, $F_{MOD}$ = 400 Hz, MOD = 30% | 57 | 62 | — | dB |
| Alternate Channel Rejection[1,3] | SINAD = 20 dB<br>Desired = 40dBµV, $F_{MOD}$ = 1 kHz, MOD = 30%<br>Undesired at ±18 kHz offset, $F_{MOD}$ = 400 Hz, MOD = 30% | 59 | 62 | — | dB |
| IP3[1,3] | Blockers at 40/80 kHz, AGC disabled (Max gain) | 110 | 120 | — | dBµV |

**Notes:**
1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
4. Guaranteed by design.

**Table 8. AM Receiver Characteristics (Continued)**

($T_{AMB}$ = –40 to 85 °C, $V_A$ = 4.5 to 5.5 V, $V_D$ = 2.7 to 3.6 V, $V_{IO1}$ = 1.7 to 3.6 V, $V_{IO2}$ = 1.2 to 3.6 V. Typical values measured at $T_{AMB}$ = 25 °C, AM modulation = 30%, $F_{MOD}$ = 1 kHz, RF level = 74 dBµV, and $F_{RF}$ = 1 MHz unless otherwise specified)

| Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IP2[1,3] | Desired = 700 kHz,<br>Undesired = 1000 kHz, 1700 kHz<br>AGC disabled (Max gain) | 142 | 146 | — | dBµV |
| RF AGC Range | | — | 50 | — | dB |
| AGC Step Resolution | | | 2 | | dB |
| RF AGC Threshold Accuracy[4] | | — | 2 | — | dB |
| IF AGC Threshold Accuracy[4] | | — | 2 | — | dB |
| Sensitivity[1,3] | SINAD = 20 dB, AGC Disabled (Max RF Gain) | — | 14 | 17 | dBµV EMF |
| THD[1,3] | Mod = 30% | — | 0.1 | — | % |
| | Mod = 90% | — | 0.2 | — | % |
| Audio SNR[1,3] | Mod = 30% | 60 | 65 | — | dB |
| Antenna Inductance[3] | | 180 | — | 540 | µH |
| **Audio Outputs: Pins LOUT and ROUT** | | | | | |
| Audio Output Resistance Load[4] | | 10k | — | — | Ω |
| Audio Output Capacitance Load[4] | Single Ended | — | — | 50 | pF |
| Audio Output Voltage | | 96 | 108 | 121 | mVRMS |
| PSRR at Audio Output Pins[4] | Ripple test should be for 100 Hz ripple on power supply lines<br>Ripple voltage = 100 $mV_{PP}$ of power supply voltage | — | 45 | — | dB |

**Notes:**
1. Guaranteed by characterization.
2. Measured at $T_{AMB}$ = 25 °C.
3. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
4. Guaranteed by design.

### Table 9. Thermal Conditions

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient Temperature | $T_{AMB}$ | — | –40 | 25 | 85 | °C |
| Junction Temperature | $T_J$ | — | — | — | 115 | °C |
| Delta from Junction to Ambient* | $\theta_{JA}$ | — | — | 27 | — | °C/W |

***Note:** The $\theta_{JA}$ is layout-dependent, and, therefore, PCB layout must provide adequate heat-sink capability. The $\theta_{JA}$ is specified assuming adequate ground plane.

### Table 10. Absolute Maximum Ratings[1]

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Analog Supply Voltage | $V_A$ | –0.5 | 5.9 | V |
| Digital Supply Voltage | $V_D$ | –0.5 | 3.9 | V |
| I/O 1 Supply Voltage | $V_{IO1}$ | –0.5 | 3.9 | V |
| I/O 2 Supply Voltage | $V_{IO2}$ | –0.5 | 3.9 | V |
| I/O 1 Input Current[2] | $I_{IN1}$ | –10 | 10 | µA |
| I/O 1 Input Voltage[2] | $V_{IN1}$ | –0.3 | $V_{I01}$ + 0.3 | V |
| I/O 2 Input Current[3] | $I_{IN2}$ | –10 | 10 | µA |
| I/O 2 Input Voltage[3] | $V_{IN2}$ | –0.3 | $V_{I02}$ + 0.3 | V |
| Operating Temperature | $T_{OP}$ | –40 | 95 | °C |
| Storage Temperature | $T_{STG}$ | –55 | 150 | °C |
| AM RF Input Level[4] | $V_{RFIN}$ | –1 | $V_A$ + 1 | V |
| AM RF Input Current[4] | $I_{RFIN}$ | –100 | 100 | mA |
| FM RF Input Level[5] | $V_{RFIN}$ | –1 | 1 | V |
| FM RF Input Current[5] | $I_{RFIN}$ | –100 | 100 | mA |
| HBM ESD | $V_{HBM}$ | –2 | 2 | kV |
| MM ESD | $V_{MM}$ | –200 | 200 | V |
| CDM ESD[6] | $V_{CDM}$ | –500 | 500 | V |
| CDM ESD[7] | $V_{CDM}$ | –750 | 750 | V |

**Notes:**
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. For input pins SCL, SDA, RSTB, A0, A1, GPIO1, GPIO2.
3. For input pins DCLK and DFS.
4. At RF input pins AM1.
5. At RF input pins FMXIN, FMXIP, FMI, FMAGC1, FMAGC2.
6. All pins.
7. Corner pins.

## 2. Typical Application Schematic

Figure 6 shows the proposed application schematic.

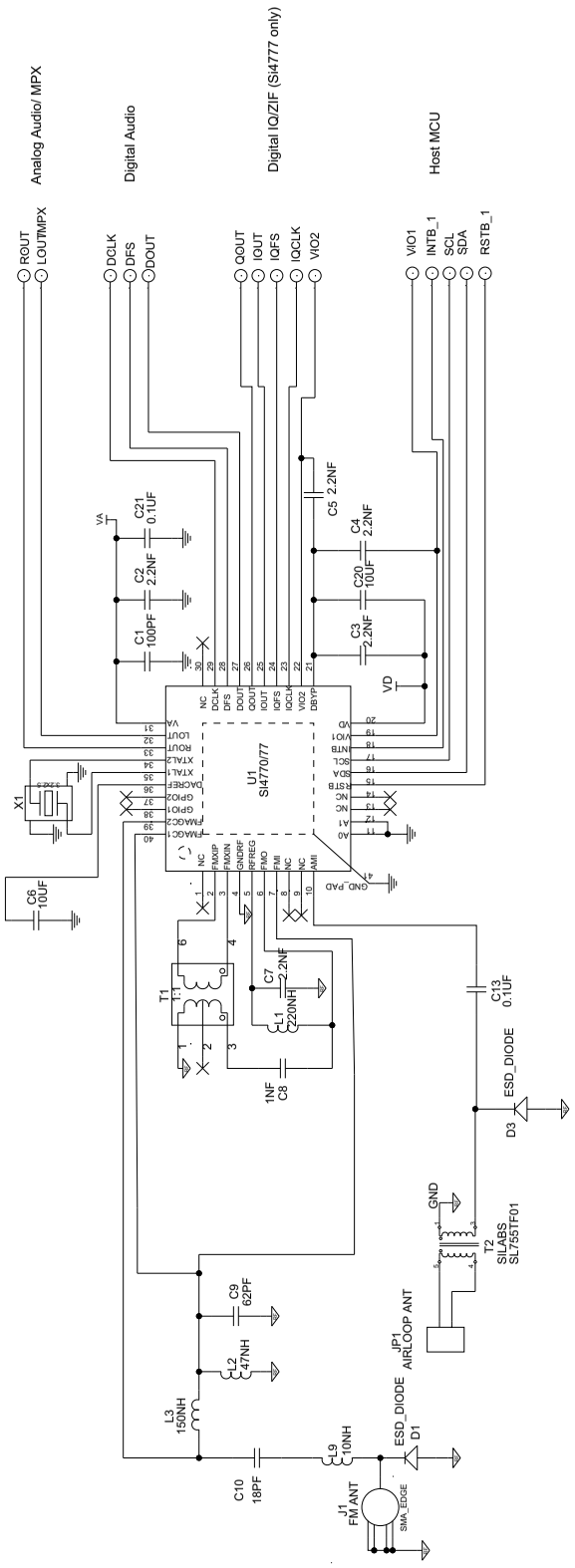


**Figure 6. Application Circuit**

## 3. Bill of Materials

**Table 11. Si4770/77-A20 Bill of Materials**

| Item | Qty | Ref | Package | Value | Mfr | Part Number |
|---|---|---|---|---|---|---|
| 1 | 1 | T2 | Transformer, Thru-hole | | Silicon Laboratories | SL755TF01 |
| 2 | 1 | T1 | BALUN, 1:1, Toko | | Toko | 458PT1566 |
| 3 | 2 | C13, C21 | CAP, SM, 0402 | 0.1 µF | Murata | GRM155R71A204KA01D |
| 5 | 1 | C1 | CAP, SM, 0402 | 100 pF | Murata | GRM1555C1H101JZ01 |
| 6 | 1 | C10 | CAP, SM, 0402 | 18 pF | Murata | GRM1555C1H180JZ01 |
| 7 | 1 | C8 | CAP, SM, 0402 | 1 nF | Murata | GRM155R61H102KA01 |
| 8 | 5 | C2, C3, C4, C5, C7 | CAP, SM, 0402 | 2.2 nF | Murata | GRM155R71H222KA01 |
| 9 | 1 | C9 | CAP, SM, 0402 | 62 pF | Murata | GRM1555C1H620JD01 |
| 10 | 2 | C6, C20 | CAP, SM, 0603 | 10 µF | Digikey | 490-3896-2-ND |
| 11 | 1 | J1 | CONN, SMA, Edgemount | | AEP Connectors | |
| 12 | 1 | JP1 | CONN, TH, HEADER, .100 PITCH,1X2 | | Samtec | HTSW-101-07-G-D |
| 13 | 2 | D1, D3 | ESD Protector, SM | | TE Connectivity | PESD0402-140 |
| 14 | 1 | U1 | IC, SM, Si4770/77-A20, QFN40 | | Silicon Laboratories | Si4770/77 |
| 15 | 1 | L9 | IND, SM, 0603 | 10 nH | Murata | |
| 16 | 1 | L3 | IND, SM, 0603 | 150 nH | Murata | LQW18ANR15G00 |
| 17 | 1 | L1 | IND, SM, 0603 | 220 nH | Murata | LQW18ANR22G00 |
| 18 | 1 | L2 | IND, SM, 0603 | 47 nH | Murata | LQW18AN47NG00 |
| 21 | 1 | X1 | XTAL, SM, 3.2 x 2.5 mm | See Table 12 | See Table 12 | See Table 12 |

**Table 12. Crystal Options**

| Frequency (MHz) | Mfr | Series | P/N |
|---|---|---|---|
| 36.400000 | NDK | NX3225SA | EXS00A-CS02420 |
| 37.800000 | NDK | NX3225SA | EXS00A-CS02421 |
| 37.209375 | NDK | NX3225SA | EXS00A-CS02422 |
| 36.400000 | TaiSaw | SMD 3.2x2.5 36.4 MHz Crystal Unit | TZ1514A |
| 37.800000 | TaiSaw | SMD 3.2x2.5 37.8 MHz Crystal Unit | TZ1517A |
| 37.209375 | TaiSaw | SMD 3.2x2.5 37.209375 MHz Crystal Unit | TZ1522A |
| 36.400000 | Jauch | JXE115 | Q36,40-JAS32P4-12-10/20-T1-LF |
| 37.800000 | Jauch | JXE115 | Q37,80-JAS32P4-12-10/20-T1-LF |
| 37.209375 | Jauch | JXE115 | Q37,209375-JAS32P4-12-10/20-T1-LF |
| 36.400000 | Epson Toyocom | TSX-3225 | OUTD-2B-0541 |
| 37.800000 | Epson Toyocom | TSX-3225 | OUTD-2B-0541 |
| 37.209375 | Epson Toyocom | TSX-3225 | OUTD-2B-0541 |

# 4. Functional Description

## 4.1. Overview

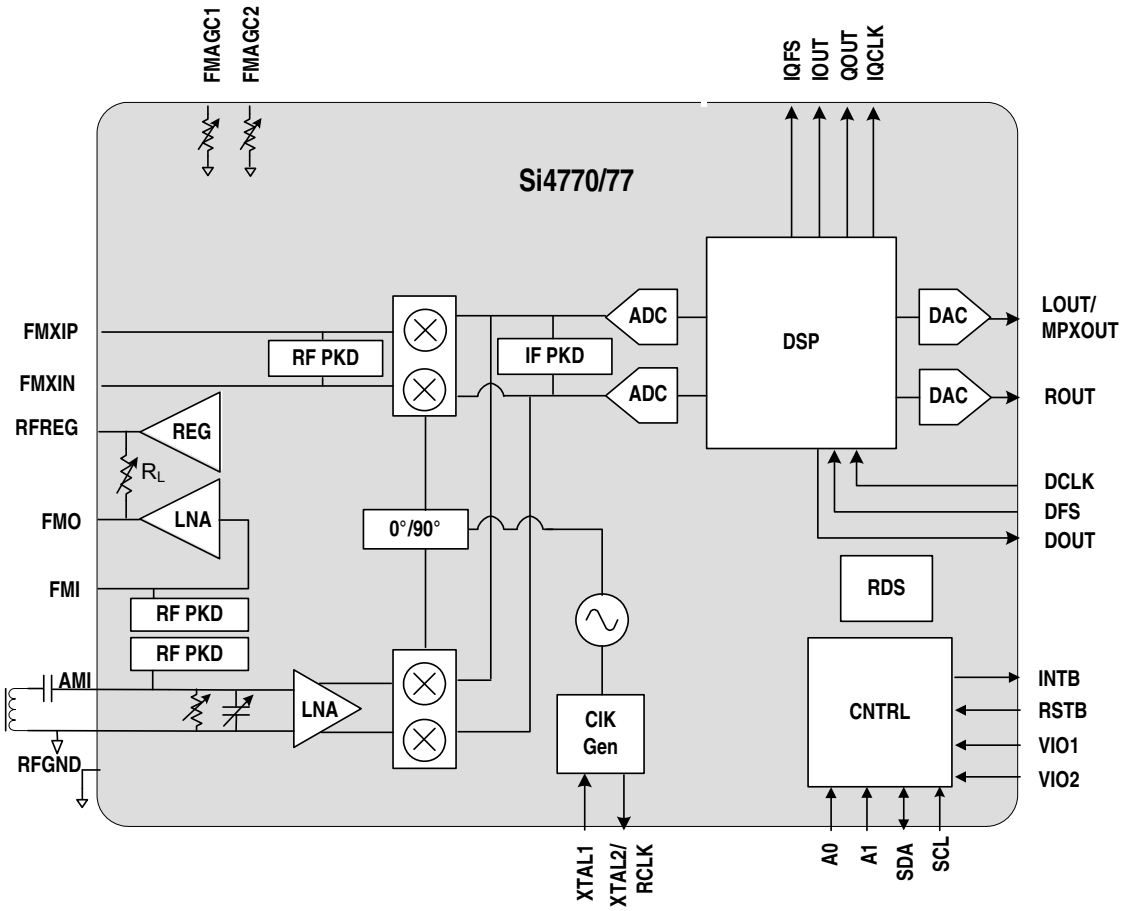


**Figure 7. Si4770/77-A20 Block Diagram**

The Si4770/77-A20 radio receiver family employs 100% RF CMOS technology to bring outstanding receiver performance to the consumer electronics industry. The Si4770/77-A20 receiver family supports worldwide radio reception. The Si4770/77-A20 incorporates a digital pre-processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions. The Si4777 supports AM/FM HD radio channel reception with digital ($I^2S$) Zero-IF (ZIF) I/Q outputs for interface to an HD radio processor.

The family leverages Silicon Laboratories' patented low-IF digital architecture, delivering superior RF performance and interference rejection. The low-IF architecture delivers superior performance while integrating the great majority of external components required by competing solutions.

The proven digital techniques provide excellent sensitivity in weak signal environments and superb selectivity and intermodulation immunity in strong signal environments. The solution offers dynamic AM/FM channel bandwidth control, auto-calibrated digital tuning, and proven AM/FM seek functionality based on multiple signal quality and band parameters. The family offers highly flexible and advanced audio processing including programmable softmute, FM stereo-mono blend, dynamic AM/FM channel bandwidth, AM/FM hi-cut, FM hi-blend, and AM lo-cut filters. In addition, the Si4770/77-A20 provides an integrated clock oscillator or accepts a reference clock and an $I^2C$-compatible, 2-wire control interface. The Si4770/77-A20 receiver system specifies a minimal bill of materials, resulting in a small board space requirement and making the solution ideal for any consumer electronics application from single tuner radios to multiple tuner radios.

**Table 13. Part Number Descriptions**

| Part Number | Description | FM (64–108 MHz) | MW (520–1710 kHz) | RDS | Analog MPX (VICS/DARC) | IBOC Blend | Digital ZIF (HD/DRM) | Channel EQ | IR Cal |
|---|---|---|---|---|---|---|---|---|---|
| Si4770 | AM/FM RDS, VICS | ✓ | ✓ | ✓ | ✓ | | | ✓ | ✓ |
| Si4777 | AM/FM RDS, VICS, HD Tuner | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

## 4.2. Clocking

The Si4770/77-A20 generates all internal clocking from an external crystal using an on-chip oscillator or an external programmable reference clock. The reference clock of Si4770/77-A20 is a sinusoidal or rectangular clock provided by an external source on pin RCLK. The supported crystal and external clock source frequencies are selected frequencies in the 36–38 MHz range.

The power up command enables the selection of an external crystal or reference clock. The reference clock and/or crystal accuracy should be ±100 ppm. In a multi-receiver system, a single crystal can be shared between all Si4770/77-A20 receivers. The Si4770/77-A20 family features programmable loading capacitors for the on-chip crystal oscillator, eliminating external loading capacitors.

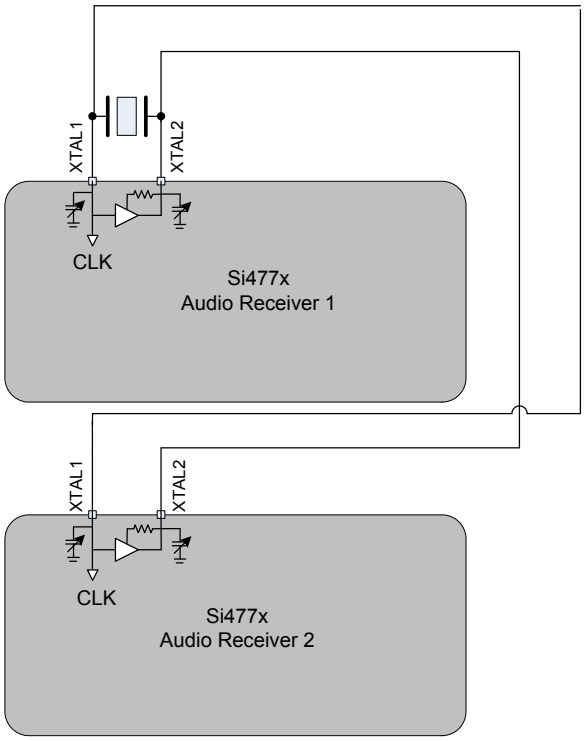


**Figure 8. Xtal Share between Two Tuners**

## 4.3. Tuning

The Si4770/77-A20 includes a complete on-chip PLL-VCO frequency synthesizer to generate the quadrature LO input to the image-reject AM and FM mixers. The Si4770/77-A20 employs a single-conversion mix (down conversion) to a fixed low IF center frequency. An innovative high-performance image reject mixer architecture allows for IF center frequencies below 300 kHz, thereby eliminating ceramic filters required in 10.7 MHz IF tuner architectures. The tune command automatically programs the LO frequency to the center of the desired channel plus (minus) the output center IF frequency when using a high-side (low-side) mix. The Si4770/77-A20 supports 50, 100, or 200 kHz channel spacing for FM, 9 or 10 kHz for AM.