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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China











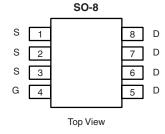
N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
30	0.0185 at V _{GS} = 10 V	9		
	0.030 at V _{GS} = 4.5 V	7		

FEATURES

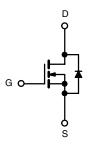
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- High-Efficient PWM Optimized
- 100 % UIS and R_g Tested





Ordering Information: Si4800BDY-T1-E3 (Lead (Pb)-free)

Si4800BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	$_{A}$ = 25 °C, unle	ss otherwise r	noted			
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	30		V	
Gate-Source Voltage		V _{GS}	± 25			
Continuous Proin Current /T 150 °C\â.b	T _A = 25 °C	- I _D	9	6.5		
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 70 °C		7.0	5.0		
Pulsed Drain Current (10 µs Pulse Width)		I _{DM}	40		Α	
Continuous Source Current (Diode Conduction) ^{a, b}		I _S	2.3			
Avalanche Current	L = 0.1 mH	I _{AS} 15		15		
Single-Pulse Avalanche Energy	L=0.1 IIII	E _{AS}	11.25		mJ	
Mariana Barana Birana a b	T _A = 25 °C	P _D	2.5 1.3		W	
Maximum Power Dissipation ^{a, b}	T _A = 70 °C] ' ⁻ D	1.6	0.8	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
			Limits		
Parameter		Symbol	Тур.	Max.	Unit
Manianum Ituration to Ambient	t ≤ 10 s	R _{thJA}	40	50	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	70	95	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	24	30	

Notes:

a. Surface Mounted on FR4 board.

b. $t \le 10 \text{ s}$.

Si4800BDY

Vishay Siliconix



Parameter	Symbol	Symbol Test Conditions		Тур.	Max.	Unit
Static	<u> </u>					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.8		1.8	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zava Cata Valtaga Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	V _{GS} = 0 V		1	μА
Zero Gate Voltage Drain Current		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	ate Drain Current ^a $I_{D(on)}$ $V_{DS} \ge 5 V_{DS}$		30			Α
	В	V _{GS} = 10 V, I _D = 9 A	0.0155 0.01		0.0185	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$		0.023	0.030	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 9 A		16		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.3 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.2	V
Dynamic ^b	1		•	•		
Total Gate Charge	Q_g			8.7	13	
Gate-Source Charge	Q_{gs}	V _{DS} = 15 V, V _{GS} = 5.0 V, I _D = 9 A		1.5		nC
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_g		0.5	1.4	2.2	Ω
Turn-On Delay Time	t _{d(on)}			7	15	
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		12	20	1
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		32	50	ns
Fall Time	t _f			14	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.3 A, dI/dt = 100 A/μs		30	60	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

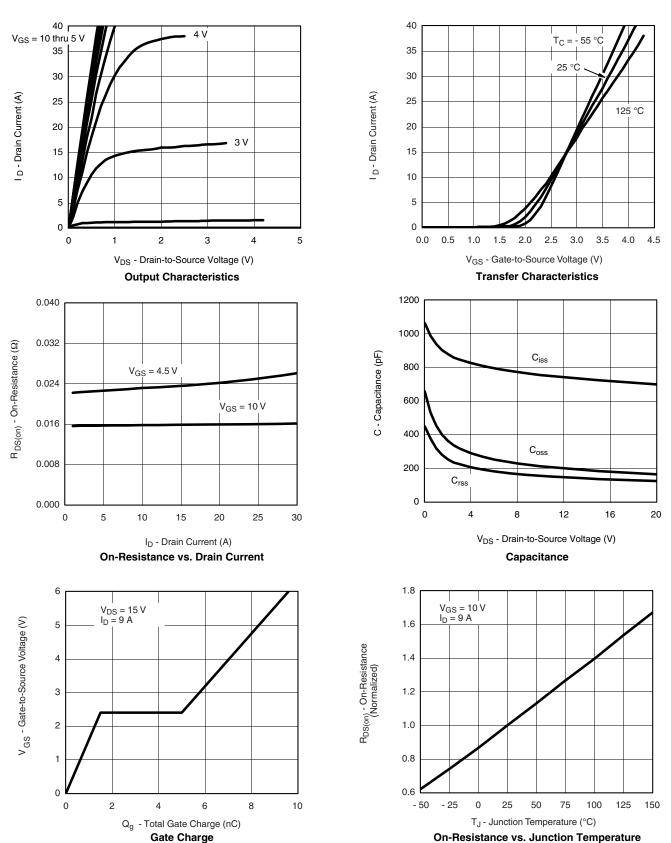
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.



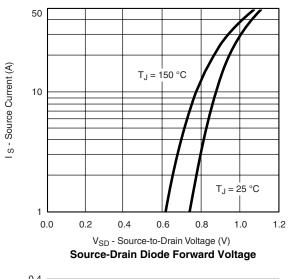


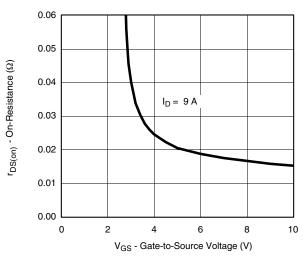
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

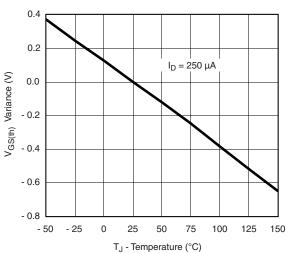


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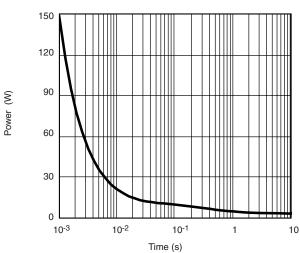
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





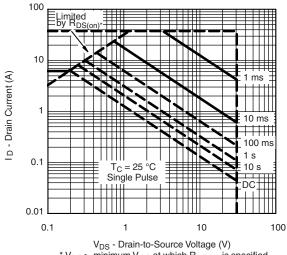


On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

Single Pulse Power, Junction-to-Ambient

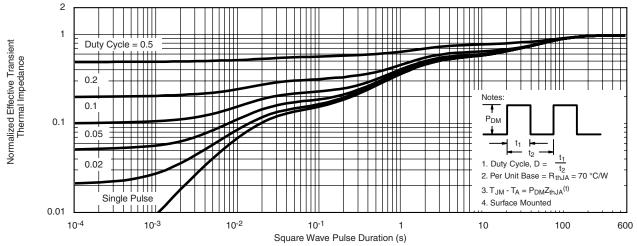


 $$V_{DS}$$ - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

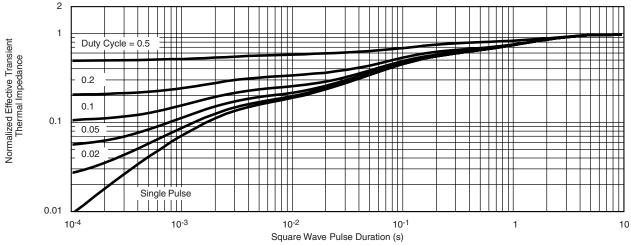
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



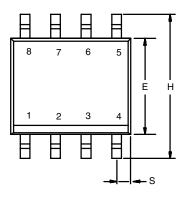
Normalized Thermal Transient Impedance, Junction-to-Foot

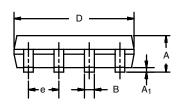
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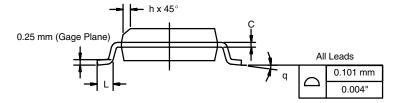
Document Number: 72124 S-83039-Rev. H, 29-Dec-08



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

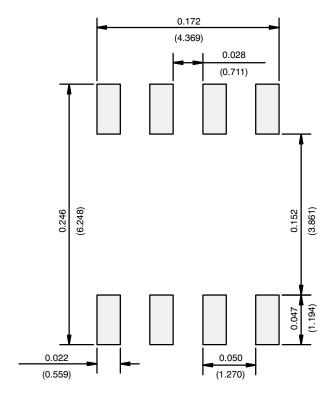
DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

APPLICATION NOTE



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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