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# **Dual N-Channel 40-V (D-S) MOSFET**

PRODUCT SUMMARY					
	V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)	
N-Channel	nel 40	0.039 at V <sub>GS</sub> = 10 V	6.6	6.6	
N-Charine		$0.050$ at $V_{GS} = 4.5 \text{ V}$	5.8	0.0	

### **FEATURES**

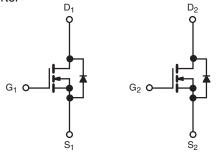
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



# COMPLIANT HALOGEN FREE Available

### **APPLICATIONS**

· CCFL Inverter



N-Channel MOSFET

N-Channel MOSFET

	SO-8	_	
S <sub>1</sub> 1	1	8	D <sub>1</sub>
G <sub>1</sub> 2	1	7	$D_1$
S <sub>2</sub> 3	1	6	$D_2$
G <sub>2</sub> 4	1	5	$D_2$
	Top View	_	

Ordering Information: Si4906DY-T1-E3 (Lead (Pb)-free)

Si4906DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	40	V	
Gate-Source Voltage		V <sub>GS</sub>	± 16	v
	T <sub>C</sub> = 25 °C		6.6	
Continuous Proin Current (T. – 150 °C)	T <sub>C</sub> = 70 °C		5.3	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	5.3 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		4.2 <sup>b, c</sup>	
Pulsed Drain Current (10 µs Pulse Width)	I <sub>DM</sub>	30	Α	
0 0 0 0	T <sub>C</sub> = 25 °C		2.5	
Source-Drain Current Diode Current	T <sub>A</sub> = 25 °C	- I <sub>S</sub>	1.7 <sup>b, c</sup>	
Pulsed Sorce-Drain Current	I <sub>SM</sub>	30		
Single Pulse Avalanche Current	l 0.4 mal l	I <sub>AS</sub>	13	
Single-Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	8.5	mJ
	T <sub>C</sub> = 25 °C		3.1	
Manipus David Distriction	T <sub>C</sub> = 70 °C		2	14/
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2 <sup>b, c</sup>	W
	T <sub>A</sub> = 70 °C		1.28 <sup>b, c</sup>	
Operating Junction and Storage Temperature Rang	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
			Lir				
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	52	62.5	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	32	40	C/VV		

### Notes:

- a. Based on  $T_{C}$  = 25  $^{\circ}C.$
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 110 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		40		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I <sub>D</sub> = 250 μA		- 4.6			
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.8		2.2	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$			100	nA	
Zawa Cata Waltana Duain Comment	1	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	$I_{DSS}$	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μΑ	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	20			Α	
	В	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		0.032	0.039		
Drain-Source On-State Resistance <sup>D</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4 A		0.041	0.050	Ω	
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A		15		S	
Dynamic <sup>a</sup>							
Input Capacitance	C <sub>iss</sub>			625		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		88			
Reverse Transfer Capacitance	C <sub>rss</sub>			50			
Total Gate Charge	Q <sub>g</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		14.4	22	nC	
				6.6	10		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 5 \text{ A}$		1.6			
Gate-Drain Charge	Q <sub>gd</sub>			2.3			
Gate Resistance	$R_{g}$	f = 1 MHz		2.3	3.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			9	15		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 4 $\Omega$		51	77		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		21	32	1	
Fall Time	t <sub>f</sub>	1		6	10		
Turn-On Delay Time	t <sub>d(on)</sub>			13	20	ns	
Rise Time	ì,	$V_{DD}$ = 20 V, $R_L$ = 4 $\Omega$		85	128		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		17	26		
Fall Time	t <sub>f</sub>	1		7	11		
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.5	Ι ,	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				30	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A		0.79	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			30	45	ns	
Rody Diodo Povorco Pocovery Chargo		1 1 7 A 41/44 100 A/45 T 05 00		30	45	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	I <sub>F</sub> = 1.7 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		17		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			13			

### Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Guaranteed by design, not subject to production testing.

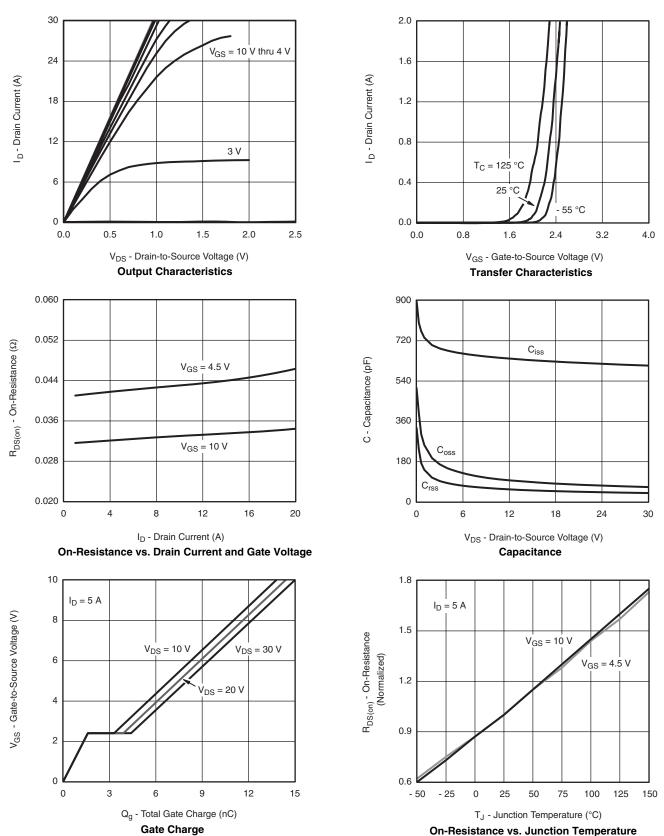
b. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.





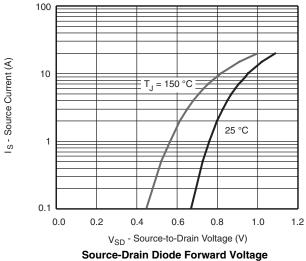


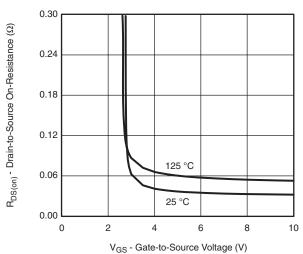
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

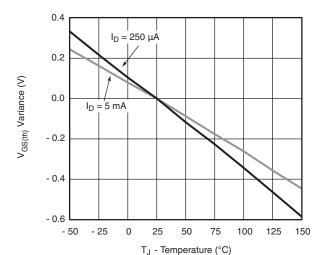


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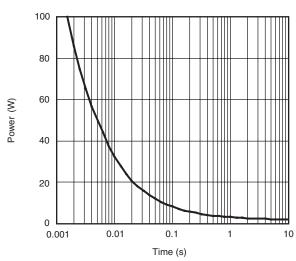
# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





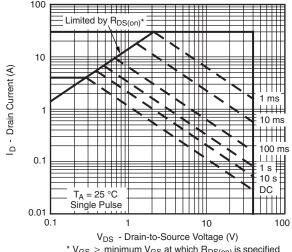


On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

Single Pulse Power, Junction-to-Ambient

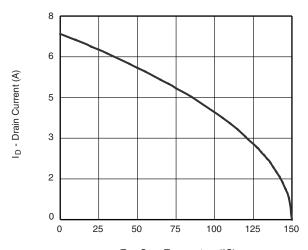


\*  $V_{GS} > minimum \, V_{GS}$  at which  $R_{DS(on)}$  is specified Safe Operating Area, Junction-to-Ambient



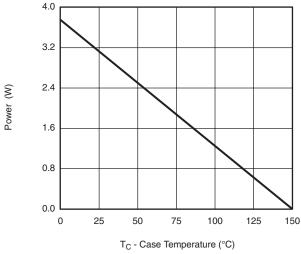


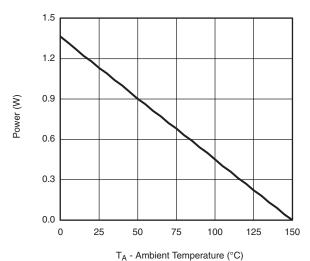
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $T_{\mbox{\scriptsize C}}$  - Case Temperature (°C)

### **Current Derating\***





Power Derating, Junction-to-Foot

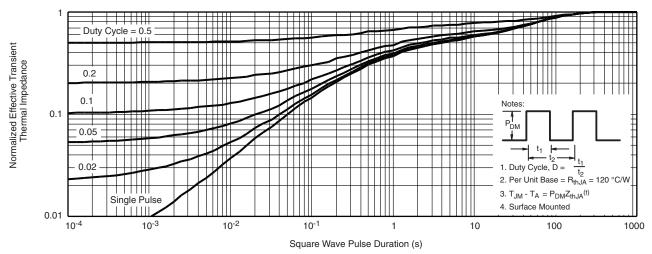
Power Derating, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

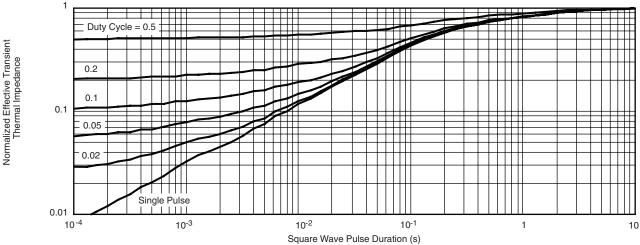
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# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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