Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Si5040

# 10 Gbps XFP Transceiver with Jitter Attenuator

## Features

Complete, high-performance, low-power, 10 Gbps XFP transceiver featuring independent CDRs, DSPLL®-based jitter-attenuating CMUs, and data retimers in both transmit and receive directions.

- DSPLL-based, jitter-attenuating CMUs in both transmit and receive directions
- Frequency-agile jitter filtering from 9.8 to 11.35 Gbps (continuous)
- Compliant to XFP specifications and jitter specifications for telecom (SONET/SDH, OTU-2) and datacom (10 GbE/10 GbE+FEC and 10 GFC/10 GFC+FEC) applications
- Supports referenceless operation
- Integrated limiting amplifier provides better than 8 mV receiver sensitivity
- User-programmable receiver loss-of-signal (LOS) detector
- Transmitter jitter generation 2.5 $mUI_{rms}$ (typical)
- Automatic slicing level adjustment with optional programmable override
- Programmable sample phase adjustment
- Line loopback, XFI loopback, pattern generation, and pattern check test capabilities
- 1.8/3.3 V or single 1.8 V supply
- 575 mW (typ) power dissipation
- 5x5 mm LGA package
- Serial microcontroller interface control


**Ordering Information:**

See page 103.

## Applications

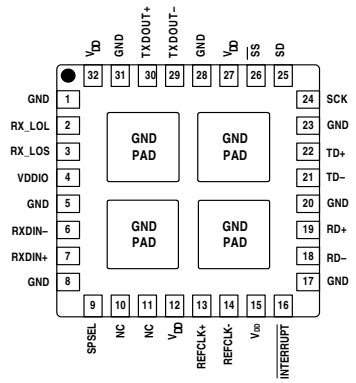
- XFP telecom modules
- XFP datacom modules
- Optical test equipment
- Jitter-attenuation and signal regeneration of 10 Gbps serial signal on line cards

## Description

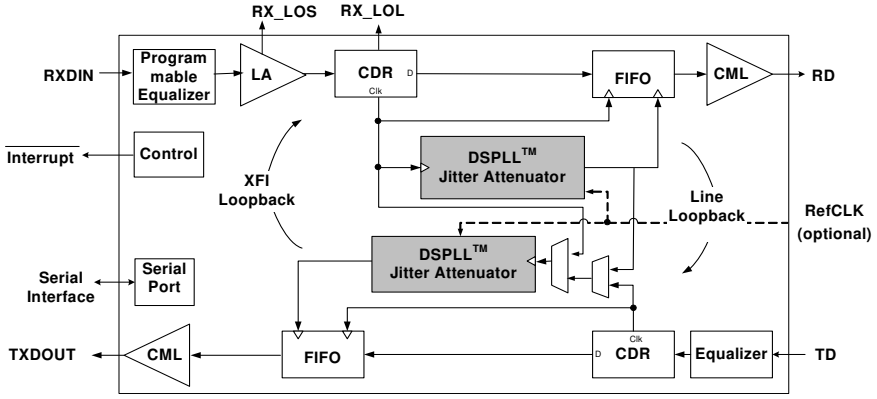
The Si5040 is a complete, low-power, high-performance XFP transceiver suitable for multiple XFP module types, from short-reach datacom to long-reach telecom applications. The Si5040 integrates a rate-agile, programmable-bandwidth, jitter-attenuating CMU in the transmit direction, which significantly attenuates jitter present at the XFI interface and on the applied reference clock, removing the need for an external jitter cleanup circuit. The device supports referenceless operation or operation with a synchronous or asynchronous reference clock. The device can be completely configured through a serial microcontroller interface. The Si5040 is compliant with all XFP requirements in both datacom and telecom applications. The Si5040 is packaged in a 5x5 mm LGA package and dissipates 575 mW (typ).

## Pin Assignments

**Si5040**
**(Transparent Top View)**

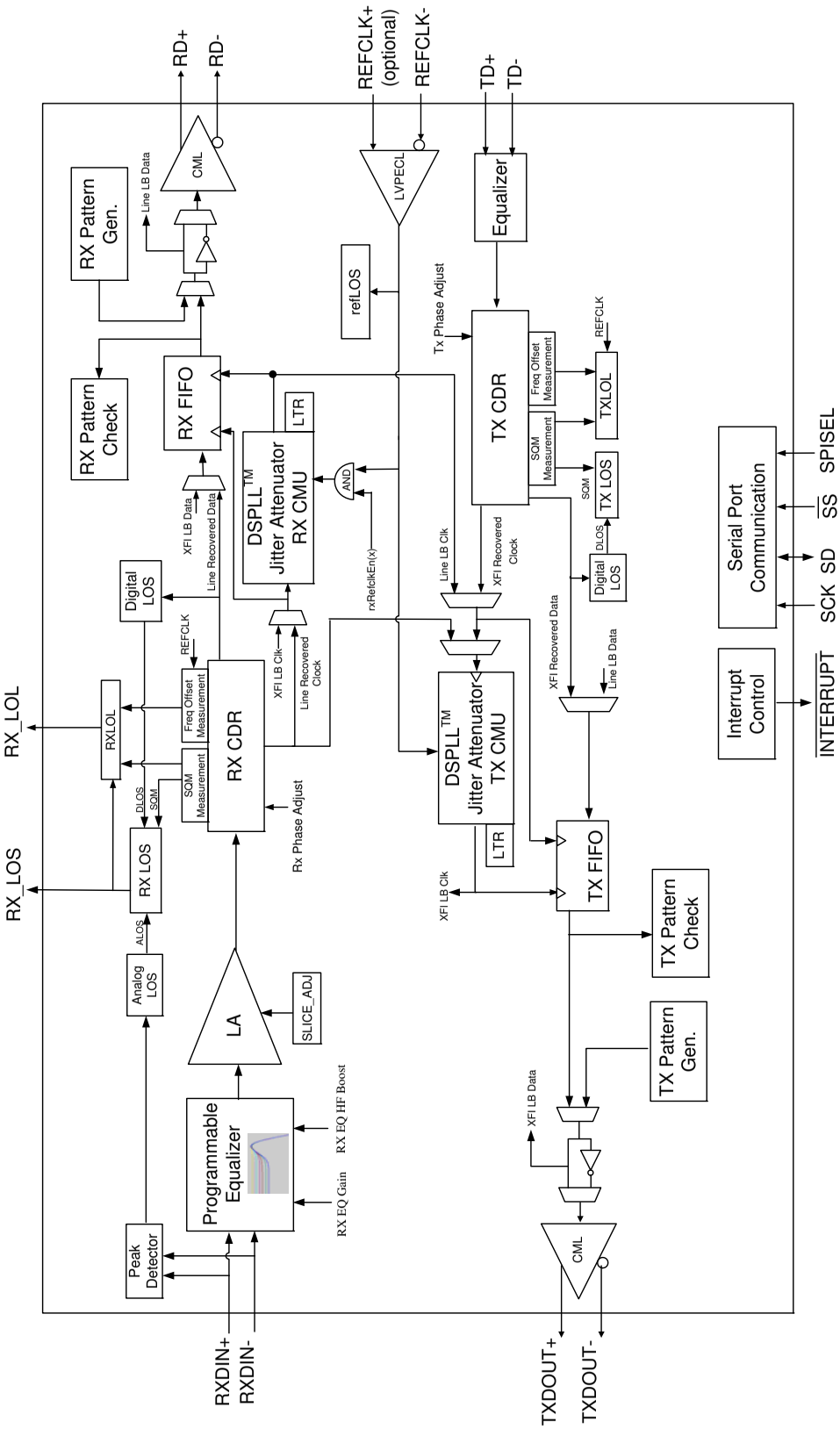



## Functional Block Diagram



# TABLE OF CONTENTS

# 1. Si5040 Detailed Block Diagram



## 2. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| Ambient Temperature | $T_A$ | | –40 | 25 | 95 | °C |
| Supply Voltage | $V_{DD}$[2] | | 1.62 | 1.80 | 1.89 | V |
| LVTTL I/O Supply Voltage | $V_{DDIO}$ | | 1.62 | — | 3.63 | V |

**Notes:**
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Maximum power ramp-up time to reach $V_{DD} \geq 1.62$ V should be less than 50 ms. Any ramp-up time slower than 50 ms will require a software reset to ensure proper calibration of all internal circuits.

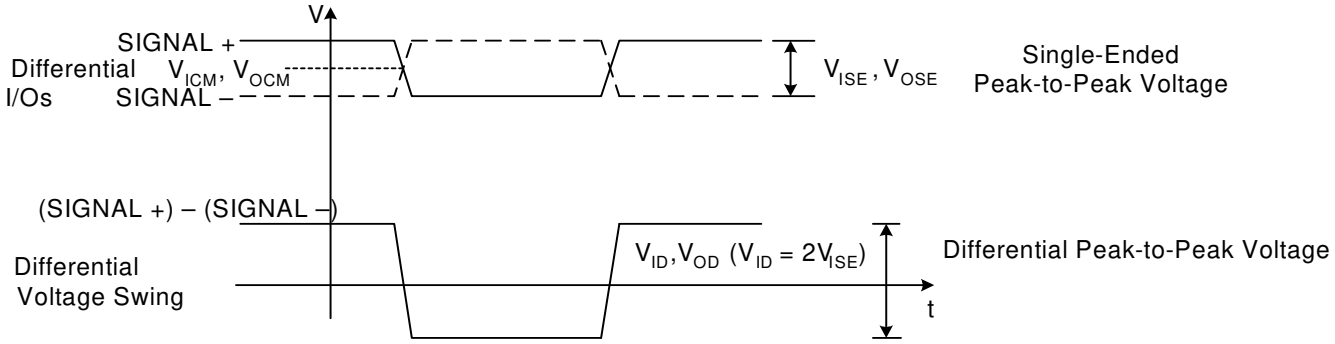



**Figure 1. Voltage Measurement**

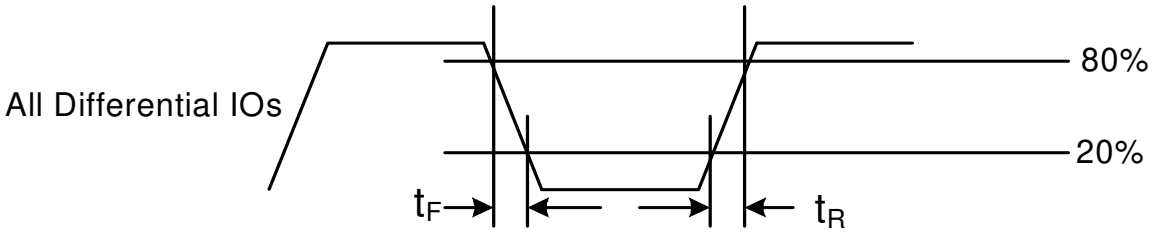



**Figure 2. Rise/Fall Time Measurement**

**Table 2. DC Characteristics**
($V_{DD}$ = 1.8 V +5%/–10%, $T_A$ = –40 to 95 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | | — | — | 370 | mA |
| Power Dissipation | $P_D$ | $V_{DD}$ = 1.89 V[1]<br>$V_{DD}$ = 1.8 V[1] | —<br>— | —<br>575 | 700<br>— | mW |
| Differential Input Voltage Swing (RXDIN) (at BER $10^{-12}$) | $V_{ID}$ | Figure 1 with Receive Equalizer bypassed | 8 | — | 1000 | $mV_{PPD}$ |
| Common Mode Output Voltage (TXDOUT) | $V_{OCM}$ | Figure 1 | — | 1.3 – $V_{OD}$/2 | — | V |
| Differential Output Voltage Swing (TXDOUT), Differential Peak-to-Peak<br>OutLevel[2:0] = 111<br>110<br>101<br>100<br>011<br>010<br>001<br>000 | $V_{OD}$ | Figure 1<br>$R_L$ = 100 Ω | <br>800<br>700<br>600<br>500<br>400<br>300<br>200<br>100 | <br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>— | <br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>— | $mV_{PPD}$ |
| LVPECL Input Voltage Swing, Differential Peak-to-Peak (REFCLK)[2] | $V_{ID}$ | Figure 1 | 250 | — | 2400 | $mV_{PPD}$ |
| Differential Input Impedance (TD, REFCLK, RXDIN) | $R_{IN}$ | | — | 100 | — | Ω |
| LVTTL Input Voltage Low | $V_{IL}$ | $V_{DDIO}$ = 3.3 V[3] | –0.3 | — | 0.8 | V |
| LVTTL Input Voltage High | $V_{IH}$ | $V_{DDIO}$ = 3.3 V[3] | 2.0 | — | $V_{DDIO}$ + 0.3 | V |
| LVTTL Input Impedance | $R_{IN}$ | | 10 | — | — | kΩ |
| LVTTL Output Voltage Low ($I_{OUT}$ = 2 mA) | $V_{OL}$ | $V_{DDIO}$ = 3.3 V[3] | — | — | 0.4 | V |
| LVTTL Output Voltage High ($I_{OUT}$ = 2 mA) | $V_{OH}$ | $V_{DDIO}$ = 3.3 V[3] | 2.4 | — | — | V |
| Differential Output Impedance (RD, TXDOUT) | $R_{OUT}$ | | — | 100 | — | Ω |
| Termination Mismatch (RD) | | | — | — | 5 | % |
| Termination Mismatch (TD) | | | — | — | 5 | % |

**Notes:**
1. TX CMU Mode 0.
2. REFCLK must be ac-coupled. For CMU Mode 1 or TX LTR operation, the minimum input swing should be 650 $mV_{PPD}$.
3. $V_{DDIO}$ = 1.8 V, not characterized.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 V +5%/–10%, $T_A$ = –40 to 95 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$I^2C$ Bus Lines (SD, SCK)** | | | | | | |
| Input Voltage Low | $V_{ILI2C}$ | | — | — | 0.3 x $V_{DDIO}$ | V |
| Input Voltage High | $V_{IHI2C}$ | | 0.7 x $V_{DDIO}$ | — | — | V |
| Input Current | $I_{II2C}$ | $V_{IN}$ = 0.1 x $V_{DDIO}$ to 0.9 x $V_{DDIO}$ | –10 | — | 10 | µA |
| Hysteresis of Schmitt trigger inputs | $V_{HYSI2C}$ | $V_{DDIO}$ = 1.8 V | 0.1 x $V_{DD}$ | — | — | V |
| | | $V_{DDIO}$ = 3.3 V | 0.05 x $V_{DD}$ | — | — | V |
| Output Voltage Low | $V_{OLI2C}$ | $V_{DDIO}$ = 1.8 V $I_O$ = 3 mA | — | — | 0.2 x $V_{DD}$ | V |
| | | $V_{DDIO}$ = 3.3 V $I_O$ = 3 mA | — | — | 0.4 | V |

**Notes:**
1. TX CMU Mode 0.
2. REFCLK must be ac-coupled. For CMU Mode 1 or TX LTR operation, the minimum input swing should be 650 $mV_{PPD}$.
3. $V_{DDIO}$ = 1.8 V, not characterized.

### Table 3. AC Characteristics–RXDIN (Receiver Input)

($V_{DD}$ = 1.8 V +5/–10%, $T_A$ = –40 to 95 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RX Path Data Rate | | | 9.80 | 9.95 | 11.35 | Gbps |
| Input Return Loss (RXDIN) | | < 2 GHz<br>5 GHz<br>10 GHz | 15<br>10<br>5 | —<br>—<br>— | —<br>—<br>— | dB<br>dB<br>dB |
| ALOS Range | | Analog Mode | 10 | — | 400 | $mV_{PPD}$ |
| ALOS Step Size | | Analog Mode | — | 1 | — | $mV_{PPD}$ |
| ALOS Relative Accuracy | | Analog Mode | 1 | — | — | mV |
| DLOS Range | | Consecutive Digits Mode | 0.5 | — | 100 | µs |
| DLOS Accuracy | | Consecutive Digits Mode | 0.5 | — | — | µs |
| ALOS Hysteresis (Programmable 0.4 dB steps) | | Analog Mode | 0 | — | 6 | dB |
| Slice Voltage Range | | mode = absolute or proportional | –240 | — | 240 | $mV_D$ |
| Slice Voltage Error | | Max error from the programmed absolute slice voltage | | | ±20 | % |
| Sample Phase Range | | | –12 | — | 12 | ps |
| Jitter Tolerance OC-192 BER = $10^{-12}$ | $J_{TOL(PP)}$ | f = 2.0 kHz | 15 | 30 | — | $UI_{PP}$ |
| | | f = 20 kHz | 1.5 | 3.0 | — | $UI_{PP}$ |
| | | f = 400 kHz | 1.5 | 3.0 | — | $UI_{PP}$ |
| | | f = 4 MHz | 0.4 | — | — | $UI_{PP}$ |
| | | f = 80 MHz | 0.4 | — | — | $UI_{PP}$ |
| Acquisition Time (Default mode)<br>REFCLK<br>Referenceless | $T_{AQ}$ | Register 86, bit 6:3 = 8 decimal<br>Register 68, bit 3:0 = 2 decimal<br>Register 67, bit 6:2 = 17 decimal | <br>—<br>— | <br>—<br>— | <br>50<br>50 | <br>ms<br>ms |
| Frequency Difference at which Receive PLL Goes Out of Lock | LOL | | 800 | — | — | ppm |
| Frequency Difference at which Receive PLL Goes into Lock | LOCK | | — | — | 200 | ppm |

**Table 4. AC Characteristics—RD (Receiver Output)**
($V_{DD}$ = 1.8 V +5/–10%, $T_A$ = –40 to 95 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Common Mode AC Output Voltage | | | — | — | 15 | $mV_{RMS}$ |
| Output Rise and Fall Times (RD) | $t_R$,$t_F$ | Figure 2 | 24 | — | — | ps |
| Differential Output Return Loss | SDD22 | 0.05–0.1 GHz | 20 | — | — | dB |
| | | 0.1–5.5 GHz | 8 | — | — | dB |
| | | 5.5–12 GHz | * | — | — | dB |
| Common Mode Output Return Loss | SCC22 | 0.1–15 GHz | 3 | — | — | dB |
| Deterministic Jitter | DJ | >4 MHz. See Appendix E1 in the XFP specification. | — | — | 0.09 | $UI_{PP}$ |
| Total Jitter | TJ | | — | — | 0.17 | $UI_{PP}$ |
| Eye Mask | X1 | See Figure 3. | — | 0.08 | — | UI |
| Eye Mask | X2 | See Figure 3. | — | 0.33 | — | UI |
| Eye Mask | Y1 | See Figure 3. | 190 | — | — | mV |
| Eye Mask | Y2 | See Figure 3. | — | — | 385 | mV |
| Jitter Transfer Bandwidth (Programmable) cmuBandwidth[3:0] (Register 6, bits 7:4) 0100 | $J_{BW}$ | 9.95 Gbps | — | 380 | 760 | kHz |

***Note:** Differential return loss given by equation SDD22 (dB) = 8 – 20.66 $Log_{10}$(f/5.5), with $f_{in}$ GHz.

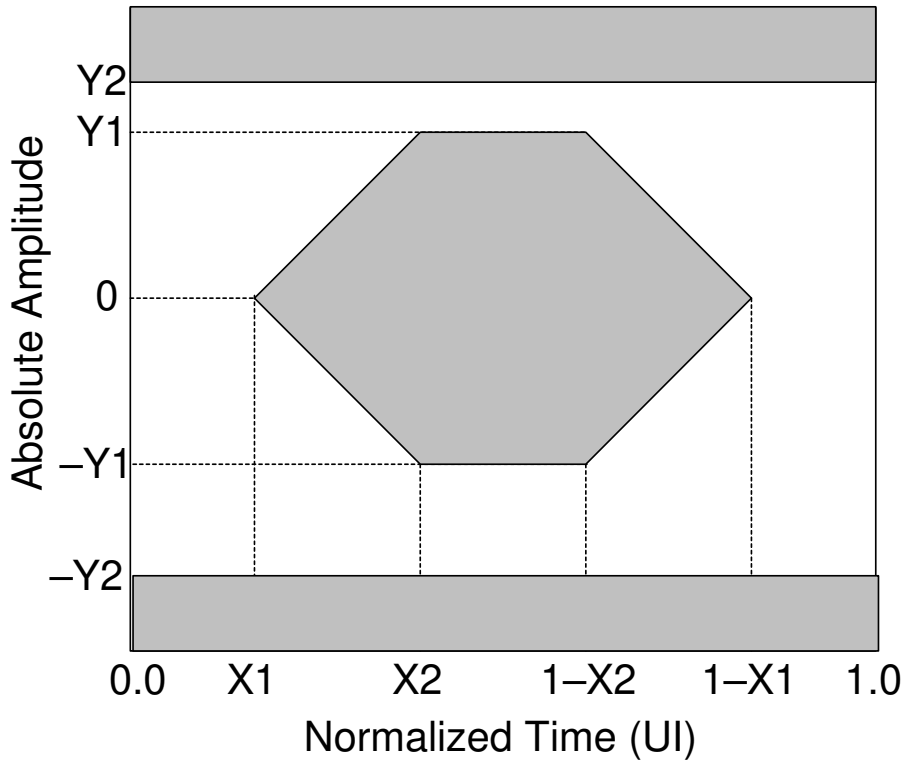



**Figure 3. Receiver Differential Output Mask (RD)**

**Table 5. AC Characteristics—TXDOUT (Transmitter Output)**
($V_{DD}$ = 1.8 V +5/–10%, $T_A$ = –40 to 95 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise + Fall Times | $t_R$, $t_F$ | Figure 2 | 20 | 25 | 30 | ps |
| Output Return Loss | | 400 kHz–10 GHz<br>10 GHz–16 GHz | 6<br>4 | —<br>— | —<br>— | dB<br>dB |
| Random RMS Jitter Generation, TXDOUT[1] | $J_{GEN(rms)}$ | OC-192, CMU mode 0 | — | 2.8 | 4.6 | $mUI_{RMS}$ |
| Total Peak-to-Peak Jitter Generation, TXDOUT[1] | $J_{GEN(PP)}$ | OC-192, CMU mode 0 | — | 36 | 60 | $mUI_{PP}$ |
| Jitter Transfer Bandwidth (Programmable)<br>CMU bandwidth [3:0]<br>(Register 134, bits 7:4) | | | | | | |
| 0000 | $J_{BW}$ | 9.95 Gbps | — | 180 | 220 | Hz |
| 0001 | | | — | 1.37 | 1.76 | kHz |
| 0010 | | | — | Not supported | | kHz |
| 0100 | | | — | 380 | 760 | kHz |
| 0101 | | | — | Not supported | | kHz |
| 0110 | | | — | Not supported | | kHz |
| Jitter Transfer Peaking | | < 120 kHz | — | | 0.03 | dB |
| Acquisition Time<br>REFCLK<br>Referenceless | $T_{AQ}$ | | <br>—<br>— | <br>—<br>— | <br>50<br>61 | <br>ms<br>ms |
| Input Reference Clock Frequency[2] | $RC_{FREQ}$ | ref clk /16 mode<br>ref clk /64 mode | 618.75<br>154.687 | 622<br>155 | 709.4<br>177.35 | MHz |
| Input Reference Clock Duty Cycle | $RC_{DUTY}$ | | 40 | — | 60 | % |
| Input Reference Clock Frequency Tolerance | $RC_{TOL}$ | | –100 | — | 100 | ppm |

**Notes:**
1. PRBS31 or SONET framed PRBS31 data. The integrated CMU filters out SONET framing effects.
2. Input reference clock frequency can be either Baud rate/16 or Baud rate/64 ±100 ppm. The typical and maximum numbers specified here correspond to /16 or /64 of the typical and maximum data rate that the device supports.

### Table 6. AC Characteristics–TD (Transmitter Input)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TX Path Data Rate | | | 9.80 | 9.95 | 11.35 | Gbps |
| Differential Input Return Loss | SDD11 | 0.05–0.1 GHz | 20 | — | — | dB |
| | | 0.1–5.5 GHz | 8 | — | — | dB |
| | | 5.5–12 GHz | See Note 1 | — | — | dB |
| Common Mode Input Return Loss (TD) | SCC11 | 0.1–15 GHz | 3 | — | — | dB |
| Total Non-DDJ[2] | | | | — | 0.45 | $UI_{PP}$ |
| Total Jitter | | TJ | | — | 0.65 | $UI_{PP}$ |
| Sinusoidal Jitter Tolerance[3] | | SJ | — | See Figure 4 | — | $UI_{PP}$ |
| Eye Mask (See Figure 5) | X1 | | — | — | 0.325 | UI |
| Eye Mask (See Figure 5) | Y1 | | 50 | — | — | mV |
| Eye Mask (See Figure 5) | Y2 | | — | — | 525 | mV |

**Notes:**
1. Return loss is given by the following equation: SDD11(dB) = 8–20.66Log10(f/5.5), with f in GHz.
2. Total jitter less ISI.
3. The jitter tolerance given in Figure 5 is in addition to the random and deterministic jitter given in this table.

### Table 7. CMU Timing Modes

| Mode | Description | Typical Jitter Gen. | Recommended CMU Jitter Transfer Bandwidth Setting |
|---|---|---|---|
| 0 | No Reference Clock or Asynchronous Reference Clock[1,2] | 3.5 $mUI_{rms}$ | 380 kHz |
| 1 | Clean, synchronous[3] | 2.5 $mUI_{rms}$ | 380 kHz |
| 2 | Clean, asynchronous[1,3] | 2.5 $mUI_{rms}$ | 1.37 kHz |

**Notes:**
1. Reference clock with frequency equal to Baud rate /64 ±100 ppm and phase noise as defined in XFP Specification 3.1, Section 3.9.
2. Since the default bandwidth for this mode is 100 kHz, Register 134 [7:4] should be written to a “4” to set the bandwidth to 380 kHz.
3. Clean reference clock with frequency equal to exactly Baud rate /64 and phase noise as defined in XFP Specification 3.1, Section 3.9.1. REFCLK input amplitude >650 mVppd.

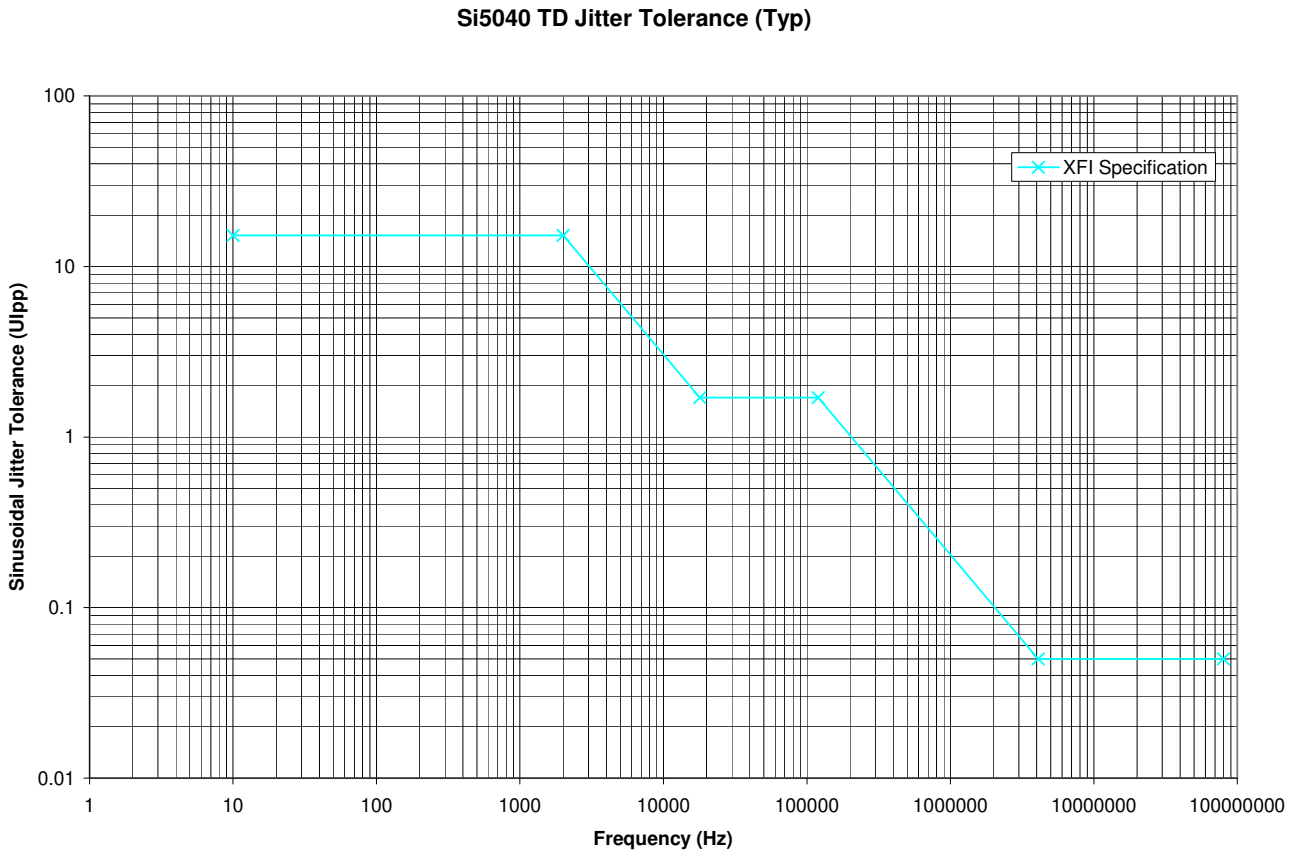



**Figure 4. XFI Sinusoidal Jitter Tolerance ($UI_{PP}$)**

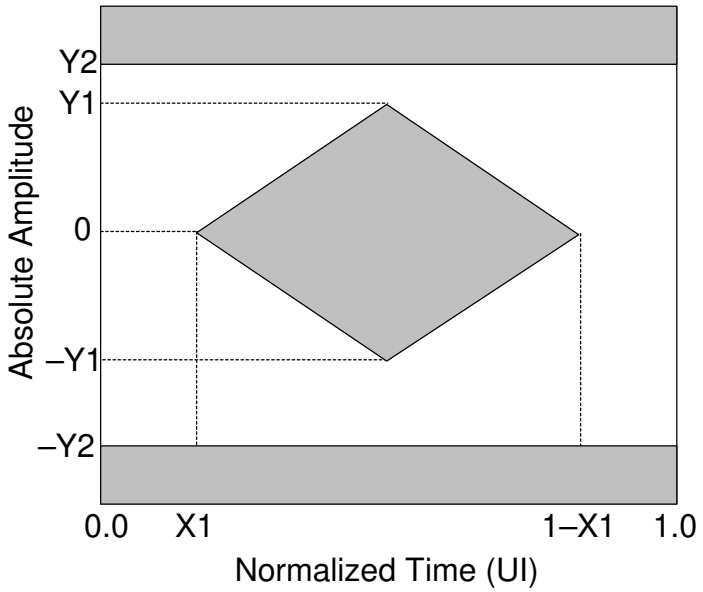



**Figure 5. Transmitter Differential Input Mask (TD)**

### Table 8. AC Characteristics—I²C Bus Lines (SD, SCK)

($V_{DD}$ = 1.8 V +5/–10%, $T_A$ = –40 to 95 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Pin Capacitance | $C_{II2C}$ | | — | — | 10 | pF |

### Table 9. Switching Characteristics—Serial Microcontroller Interface[2]

$V_{DD}$ = 1.8 V +5/–10%, $V_{DDIO}$ = 3.3 V ±10%, $T_A$ = –40 to 95 °C, $C_L$ = 20 pF

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Cycle Time SCK | $t_c$ | | 100 | — | — | ns |
| Rise Time, SCK | $t_r$ | 20–80% | — | — | 25 | ns |
| Fall Time, SCK | $t_f$ | 20–80% | — | — | 25 | ns |
| Low Time, SCK | $t_{lsc}$ | 20–20% | 30 | — | — | ns |
| High Time, SCK | $t_{hsc}$ | 80–80% | 30 | — | — | ns |
| Delay Time, SCK Fall to SD Active | $t_{d1}$ | | — | — | 25 | ns |
| Delay Time, SCK Fall to SD Transition | $t_{d2}$ | | — | — | 25 | ns |
| Delay Time, $\overline{SS}$ Rise to SD Tri-state[1] | $t_{d3}$ | | — | — | 25 | ns |
| Setup Time, $\overline{SS}$ to SCK Fall | $t_{su1}$ | | 25 | — | — | ns |
| Hold Time, $\overline{SS}$ to SCK Rise | $t_{h1}$ | | 20 | — | — | ns |
| Setup Time, SD to SCK Rise | $t_{su2}$ | | 25 | — | — | ns |
| Hold Time, SD to SCK Rise | $t_{h2}$ | | 20 | — | — | ns |
| Delay Time between Slave Selects | $t_{cs}$ | | 25 | — | — | ns |

**Notes:**

1. SD is designed to be tristated by the release of the chip select signal (the rising edge of the $\overline{SS}$).
2. All timing is referenced to the 50% level of the waveform unless otherwise noted. Input test levels are $V_{IH} = V_{DD} - 0.4$ V, $V_{IL}$ = 0.4 V

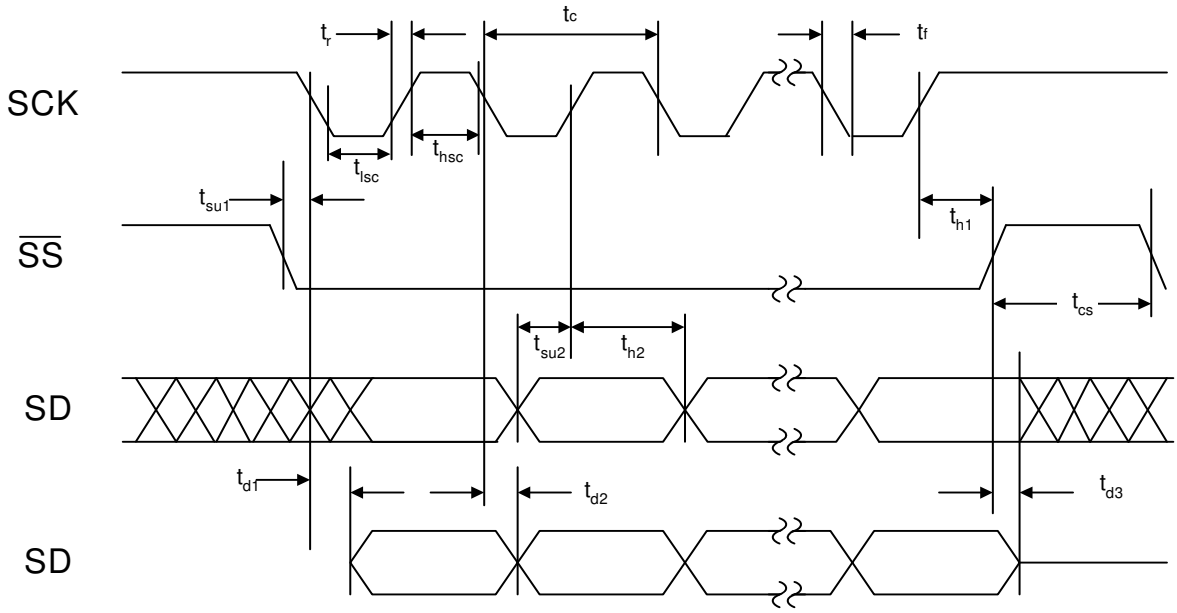



**Figure 6. Serial Microcontroller Interface Timing Diagram**

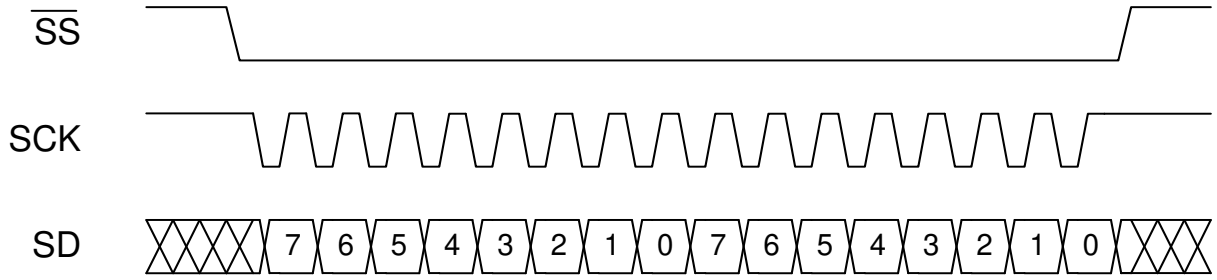



**Figure 7. SPI-Like Interface Write/Set Address Command**

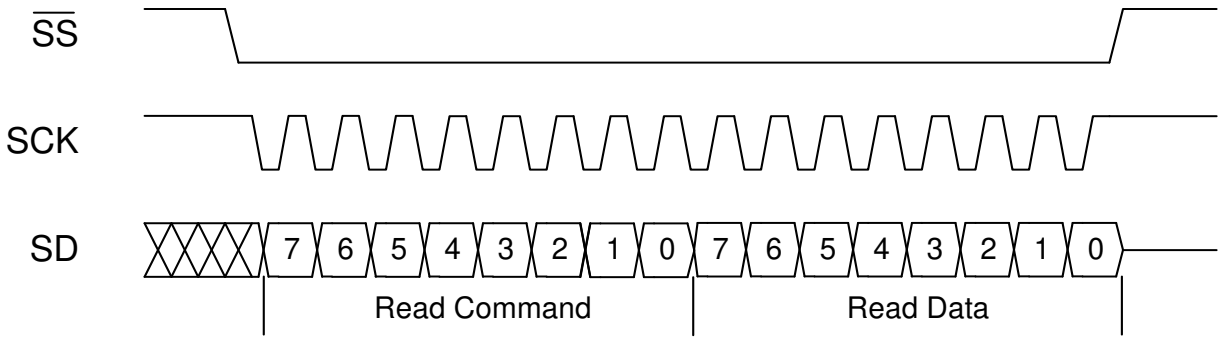



**Figure 8. SPI-Like Interface Read Command**

### Table 10. Thermal Characteristics

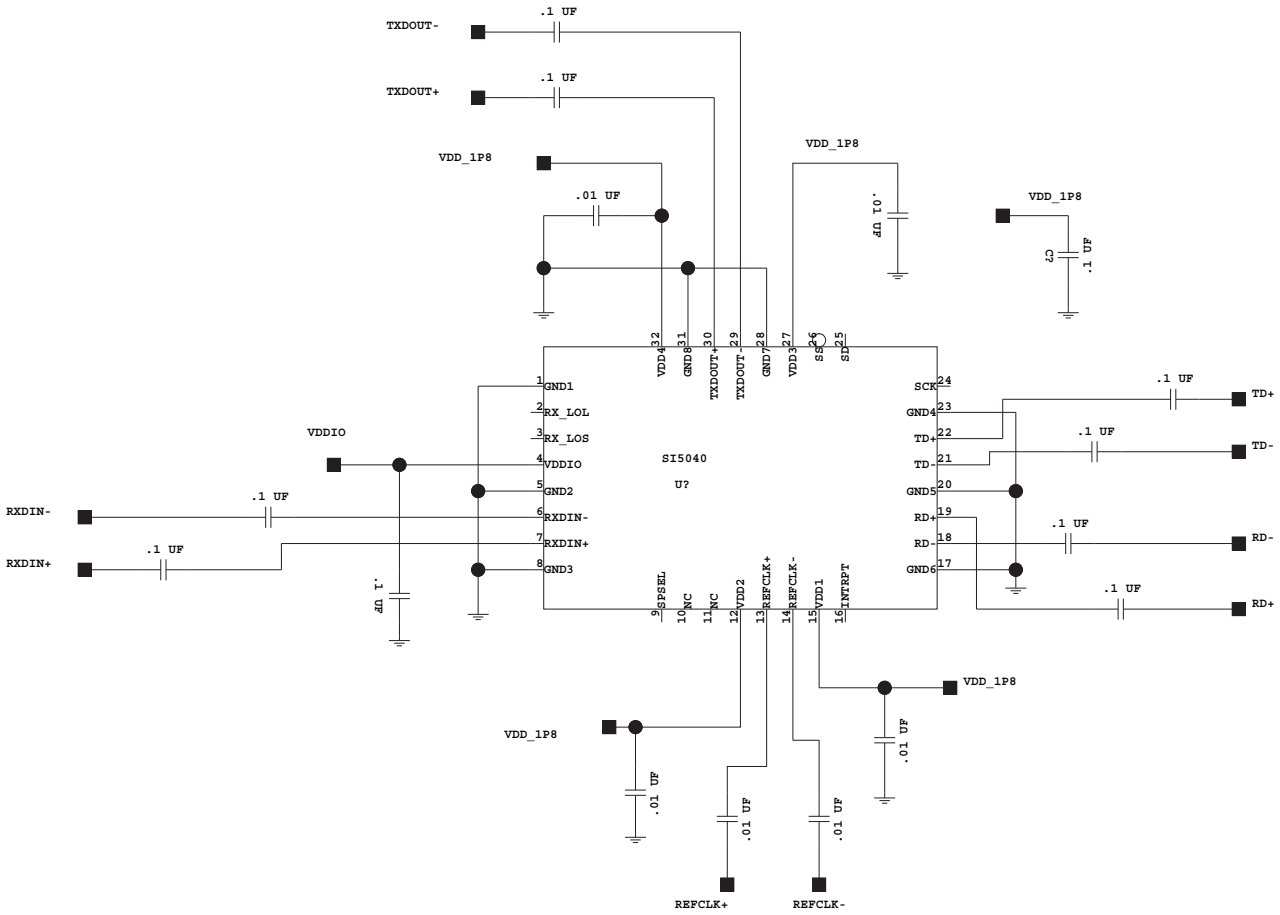
| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\varphi_{JA}$ | Still Air | 50 | °C/W |

### Table 11. Absolute Maximum Ratings*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | –0.5 to 1.98 | V |
| LVTTL Supply Voltage | $V_{DDIO}$ | –0.5 to 3.8 | V |
| Differential Input Voltages | $V_{DIF}$ | –0.3 to ($V_{DD}$+ 0.3) | V |
| Maximum Current any Output PIN | | ±50 | mA |
| Operating Junction Temperature | $T_{JCT}$ | –55 to 150 | °C |
| Storage Temperature Range | $T_{STG}$ | –55 to 150 | °C |
| ESD HBM Tolerance (100 pf, 1.5 kΩ) | High-speed pins | 2 | kV |
| | All except high-speed pins | 2 | kV |

***Note:** Permanent device damage can occur if the absolute maximum ratings are exceeded. Restrict functional operation to the conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 3. Typical Application Schematic



# 4. Functional Description

The Si5040 XFP transceiver is a single-chip, bidirectional signal conditioner for use in XFP modules as defined by the XFP multi-source agreement. The Si5040 includes independent clock and data recovery units (CDRs) and frequency-agile, jitter-attenuating clock multiplier units (CMUs) in both receive and transmit directions. The receive path includes a limiting amplifier and a programmable equalizer for direct connection to an optical receiver trans-impedance amplifier. The transmit path includes an equalizer for direct connection to the XFI channel.

The device provides data-agnostic operation over a continuous range of data rates from 9.8 to 11.35 Gbps.

Typical data rates and associated applications include the following:

- 9.8304 Gbps: Common Public Radio Interface (CPRI)
- 9.95 Gbps: SONET OC-192, SDH STM-64, 10 Gbps Ethernet WAN PHY
- 10.31 Gbps: 10 Gbps Ethernet LAN PHY
- 10.52 Gbps: 10 Gbps FibreChannel (10 GFC)
- 10.70 Gbps: OTN OTU-2 (G.709)
- 11.09 Gbps: 10 Gbps Ethernet LAN PHY with 255/237 FEC coding
- 11.32 Gbps: 10 Gbps FibreChannel with 255/237 FEC coding

Serial control and status monitoring is supported with either an SPI-like or $I^2C$ serial interface.

# 5. Receiver

The Si5040 receiver includes a programmable equalizer, a high-sensitivity limiting amplifier, clock and data recovery unit (CDR), and a FIFO/retimer function.

## 5.1. Receive Equalizer

The RX equalizer is a programmable equalizer designed to boost the high-frequency components while attenuating the low-frequency components. Figure 9 illustrates a typical frequency response of the RX equalizer when its capacitor setting (or high-frequency boost, RxEqHFBoost at Register 85, Bit [7:5]) is set to the maximum value and its resistor setting (or low-frequency gain/attenuation, RxEqGain at Register 84, Bit [7:5]) is changed to achieve different low-frequency attenuations.

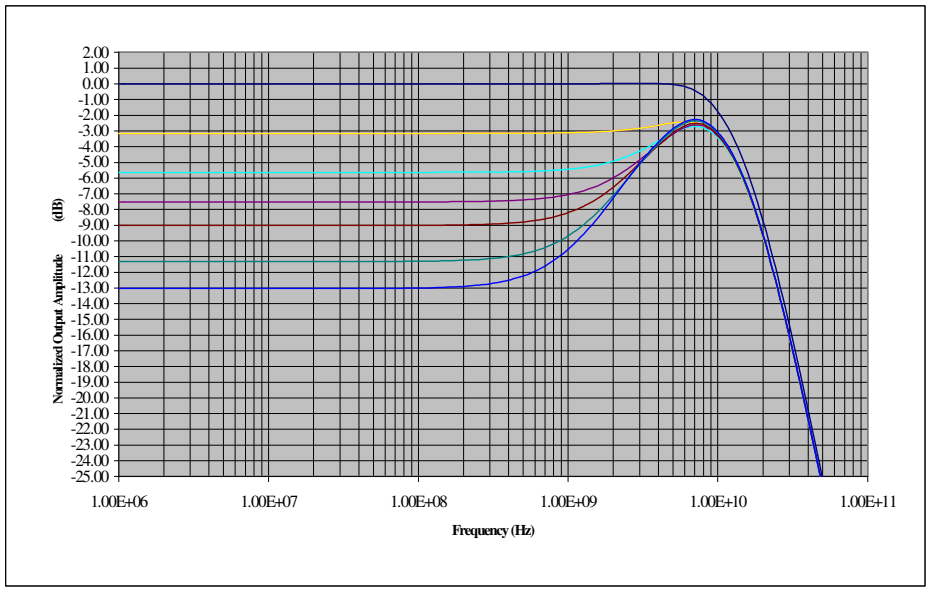



**Figure 9. Typical RX Equalizer Frequency Response**

To optimize the equalizer settings for a given application, the following procedure is recommended:

- Set RxEqHFBoost at Register 85, Bit [7:5] to 7 (Default = 4), and adjust RxEqGain at Register 84, Bit [7:5] (Default = 5), to achieve the best performance.
- Further adjust RxEqHFBoost to increase the performance further.

Note that setting RxEqGain to 0 dB bypasses the equalizer.

## 5.2. Limiting Amplifier

The Si5040 incorporates a high-sensitivity differential limiting amplifier with sufficient gain to allow direct connection to a transimpedance amplifier. The amplifier has a guaranteed sensitivity of 8 mVppd.

## 5.3. Receive Amplitude Monitor

The Si5040 limiting amplifier includes circuitry that monitors the amplitude of the receiver differential input signal (RXDIN). The amplitude value can be read from the Peakdet register (Register 16). The receiver signal amplitude monitoring circuit is also used in the generation of the loss-of-signal alarm (LOS).

## 5.4. Receiver Loss of Signal Alarm (LOS)

The Si5040 receiver generates a loss-of-signal alarm when the input signal fails to meet the selected programmable condition for loss of signal. The programmable LOS mode is controlled in the RxlosCtrl register (Register 10). The programmable modes are Analog Loss Of Signal (ALOS), Digital Loss of Signal (DLOS), and Signal Quality Monitor (SQM). As shown in Figure 15, one or more of these alarm signals is logically combined into the Receiver Loss of Signal (RX_LOS) alarm pin (Pin 3). The state of the RX_LOS alarm pin will also be reflected in the LOS bit in the RxAlarmStatus register (Register 9). LOS may also be configured to generate an interrupt. The status of the LOS interrupt bit may be read in the RxintStatus register (Register 5). The status of the various LOS modes is stored in the losStatus register (Register 11).

An ALOS alarm occurs when the peak-to-peak signal amplitude on the RXDIN input is below the threshold value set in the aLosThresh register (Register 12). The level may be set from 10 to 400 mV in 1 mV increments. The amount of hysteresis applied to ALOS is set in the aLosThresh2 register (Register 13) up to a maximum of “aLoSThresh+” 6 dB. The default value is “aLoSThresh+” 3 dB. The analog LOS function is enabled by setting bit 0 in the RxLosCtrl register (Register 10). Note that the peak-to-peak detector and ALOS detection are designed to work with pseudo-random dc-balanced data band limited to <2 GHz.

A DLOS alarm occurs when the receive bit stream consists of a run length of 1s or 0s greater than the value loaded in the RxdLosAssertThresh register (Register 17). DLOS will remain asserted until the data shows activity for a time greater than that loaded in the RxdLOSClearThresh register (Register 18). Refer to Figure 10 and Figure 11 for algorithm flowcharts.

An SQM alarm occurs when the estimate of the receive signal quality falls below the value loaded in RxsqmThresh (Register 26). The Signal Quality Monitor measures the magnitude of the horizontal eye opening of the received signal. The SQM value can be read from the RxsqmValue register (Register 25). An SQM alarm will assert if the RxsqmEn bit has been set in the RxsqmConfig register (Register 26). SQM hysteresis is set in the RxsqmDeassertThresh register (Register 27).

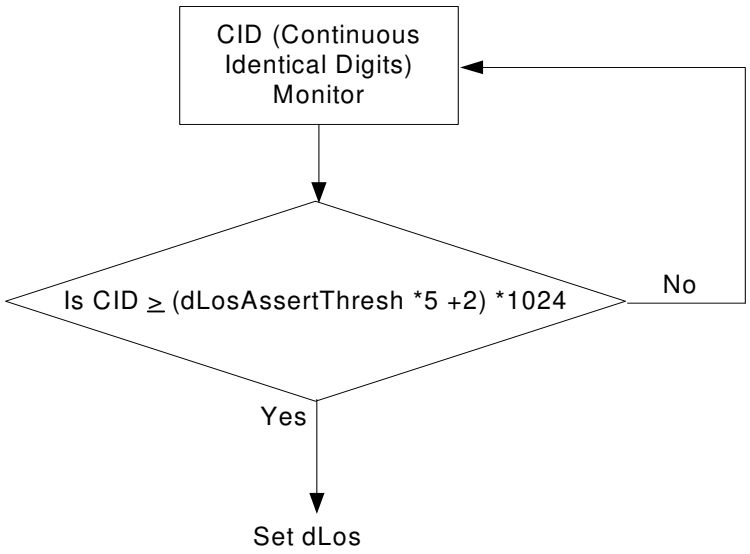



**Figure 10. Algorithm to Set dLOS**

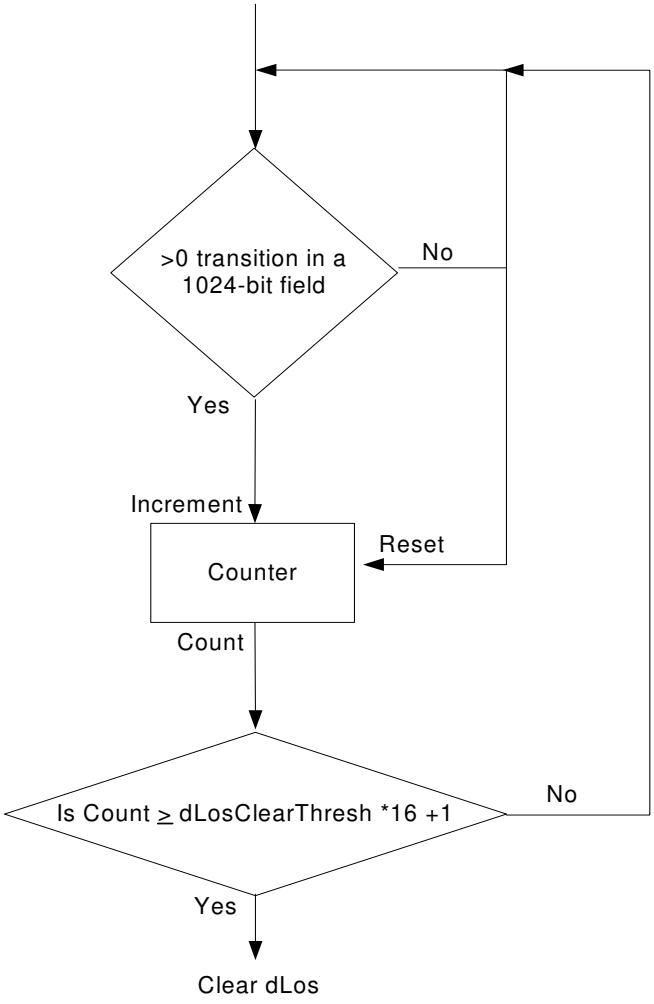



**Figure 11. Algorithm to Clear dLOS**

The receiver may be programmed to perform any of the following consequent actions upon declaring RX_LOS:

1. Lock the receiver to the applied reference clock (lock to reference): ltrOnLOS bit in Register 7.
2. Assert receiver loss of lock (LOL): lolOnLOS bit in Register 7.
3. Disable (squelch) the receive data output (RD): SquelchOnRxLOS bit in Register 28.
4. Generate a clock pattern at the receive data output (RD): clkOnLOS bit in Register 28.

For different combinations of ltrOnLOS and lolOnLOS settings in Register 7, the device may behave differently in the CDR lock acquisition process. Refer to Figure 12 and Figure 13 for more details on CDR and VCO behaviors upon declaring LOS. ltrOnLOS = 0, lolOnLOS = 0, and VCOCAL[1:0] = 10 binary by default.

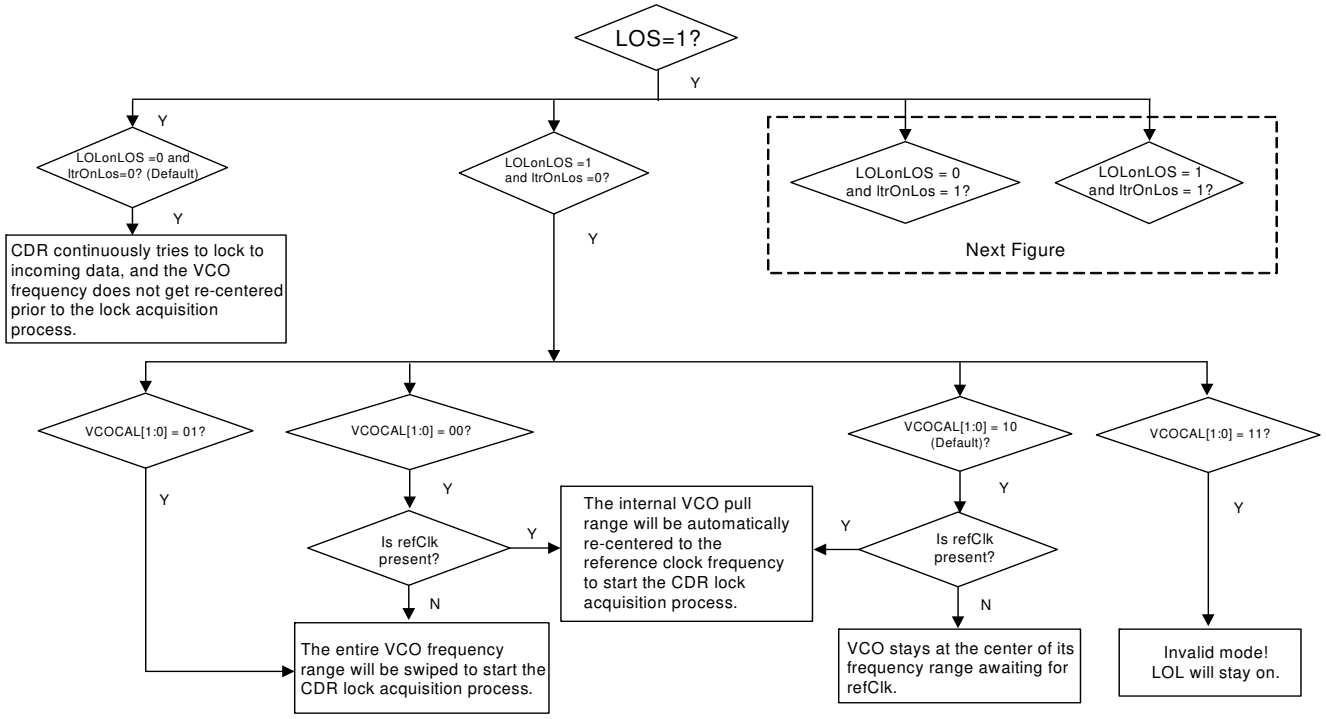



**Figure 12. CDR and VCO Behaviors Upon Declaring LOS (1 of 2)**

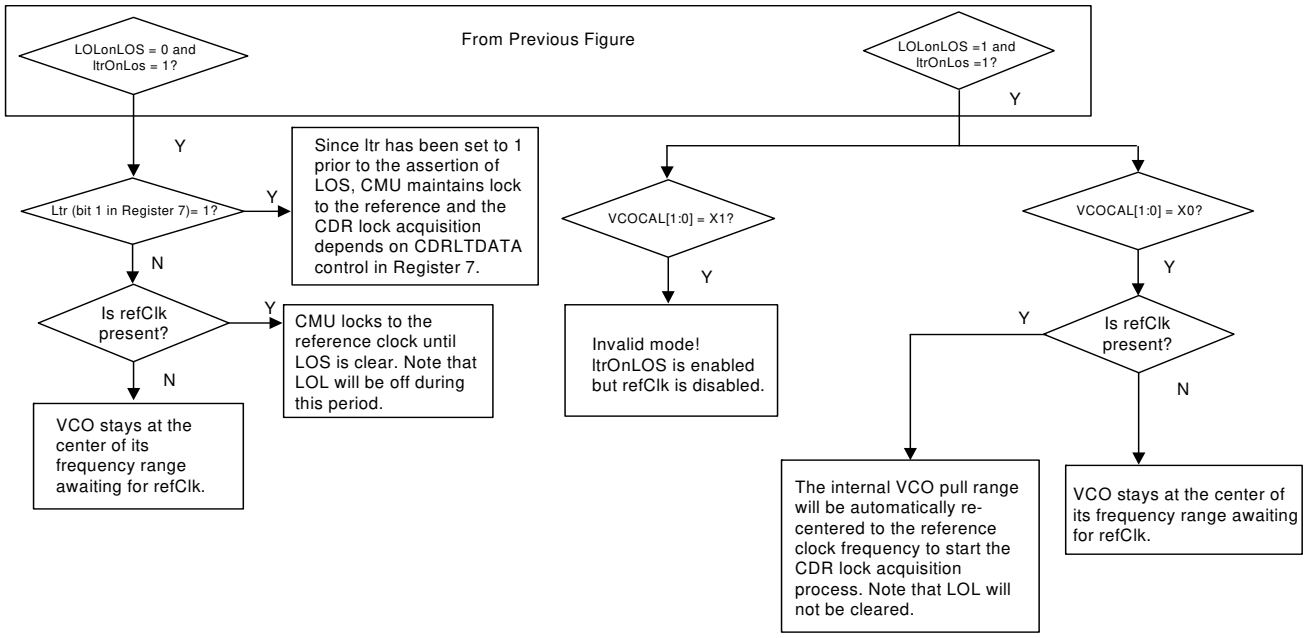



**Figure 13. CDR and VCO Behaviors Upon Declaring LOS (2 of 2)**

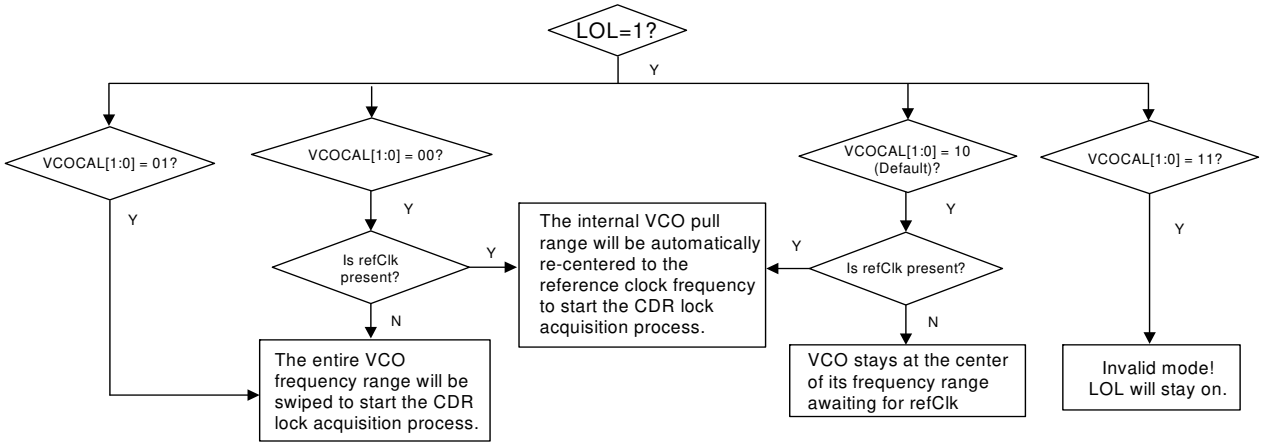



**Figure 14. Receive and Transmit CDR and VCO Behaviors Upon Declaring LOL**

## 5.5. Receiver Slice Control

In order to optimize the bit error rate performance of the system, the receiver supports automatic and manual adjustment of the 0/1 decision threshold (slice control). Four slice modes can be programmed via Register 20 as detailed below:

- AutoSlice Mode (sliceEn[2:0] = 001): The slice is automatically set without any control by the user. An internal estimate of the eye opening is used to automatically adjust the slice voltage. This mode can be used when there is no FEC processor as it continually adjusts the slice voltage. Registers 22/21 have no effect on this mode of operation.
- Constant Duty Cycle Mode (sliceEn[2:0] = 010):
  This mode continually adjusts the slice voltage to maintain a user-selected duty cycle at the limiting amplifier output. The duty cycle can be set in the sliceLVL register (Registers 22 and 21). This mode can be used when there is no FEC processor, however, if the duty cycle is dynamically controlled the recommended duty cycle step size is less than or equal to 0.1%. In an actual system the duty cycle should not be set to less than 45% or greater than 55%. For the case of maximum dispersion, an optimally-set duty cycle will typically perform slightly better than Autoslice.
- Proportional Mode (sliceEn[2:0] = 011):The slice offset is defined as a percentage of the peak-to-peak value of the input signal. The percent value is written in the sliceLVL register (Registers 22 and 21) as an offset from 50%. Due to drifts and temperature variations in the silicon, the slice offset values must be dynamically modified at a rate of 100 ms or faster. This mode is recommended only when a FEC processor is present to control the slice level.
- Absolute Mode (sliceEn[2:0] = 100): The slice offset is defined as an absolute voltage. The offset can be set in the range of –240 to +240 mV in the sliceLVL register (Registers 22 and 21). Just as in proportional mode, the slice offset values must be dynamically modified at a rate of 100ms or faster. This mode is recommended only when a FEC processor is present to control the slice level.

Autoslice and constant duty cycle are the preferred slice modes of operation for Telecom and Datacom applications.

## 5.6. Clock and Data Recovery (CDR)

The Si5040 integrates a CDR to recover the clock and data from the input signal applied to RXDIN. The CDR can be operated with or without an external reference clock. Reference or referenceless operation is programmed in the RxCalConfig register (Register 8). If a reference clock is applied to the receiver, the CDR can be forced to lock to the reference clock in the event that a loss of signal occurs. The CDR can be programmed to continue to sample the RXDIN input while the receive PLL is locked to the reference clock. These options are controlled in the RxConfig register (Register 7).

## 5.7. Reference Clock

The Si5040 will operate with or without an external reference clock. If a reference clock is applied, the receiver uses the reference clock to center the internal VCO pull range, which, in turn, reduces the acquisition time of the CDR. If the reference clock is not applied, the entire VCO frequency range will be swept for lock acquisition.

Note that since the applied reference clock is used for both the receiver and the transmitter and since the receiver may be running at a different rate than the transmitter, the user is given the option of disabling the reference clock on the receiver.

The RxrefclkEn bit in the RxConfig register (Register 7) controls this function. The receiver can be locked to the reference clock under the following programmable conditions: (RxConfig, Register 7)

1. Set LTR (bit 1).
2. Set LTR on receive loss-of-signal (LOS) (bit 5).

**Note:** If it is desired to allow the CDR to acquire lock to the incoming data while LTR at Register 7, Bit 1 is set to 1 (Lock to Reference clock enabled), set CDRLTDATA at Register 7, Bit 4 to 1 (default). If it is desired to sample the incoming data with a programmable phase and slice level while LTR is set to 1, set sliceEn[2:0] at Register 20 to 000 binary (auto slice disabled).

## 5.8. Receiver Loss of Lock (LOL)

Receiver LOL functions differently depending on whether the receiver is operating in reference or referenceless mode. By default (uselolmode Register 7, Bit 3 = 0), SQM-based LOL is used in referenceless mode, and Frequency-based LOL is used in reference mode. In reference mode however, either SQM or Frequency LOL can be used by setting Register 7, Bits 2 and 3 to the appropriate values.

### 5.8.1. SQM LOL

SQMLOL mode is selected in one of two ways. If register 7[3:2] = 11b, then SQMLOL mode is selected. If register 7[3] = 0 and register 7[1] = 0, then SQMLOL mode is selected. The SQMLOL method compares an internal jitter measure to the sqmLOLThresh (see below on how to set this threshold). When the internal jitter measure is greater than the sqmLOLThresh, RXLOL is asserted. When RxLOL is asserted the 5040 RX side will automatically start to try to acquire lock again across an input data range of 9.8–11.4 Gbps. RxLOL is deasserted when the jitter measure is less than the sqmLOLThresh. The sqmLOLThreshold must be set using registers 106, 107, 108, and 109 in the following order:

1. Write register 107 = A0h.
2. Write register 108 = 3Fh.
3. Write register 109 = B9h.
4. Write register 106 = 04h.
5. Write register 106 = 84h.

These are indexed address registers. Register 106 contains the sqmLOLThresh register address and 107-109 contain the data to be written to it. Register 106 must be written twice. The first write of 04h sets the address, and 84h applies the value in 107-109 into the sqmLOLThresh registers. The above values are recommended for all applications.

Using sqmLOLThresh values other than the default or the one given above can cause unexpected problems, such as false lock, and are not recommended.

#### 5.8.1.1. Dynamic Register Control

The dynamic control of RxLoopFAcq (Register 98) is required to ensure the locking performance of the CDR. It is required for all applications that RxLoopFAcq be set to 98h when RX LOL is asserted and to 00h when RX LOL is deasserted. Only the default value and the value given above are supported for writes to Register 98. Any read back of this register will not necessarily return the value written. If a valid reference clock is applied at pins 13,14 and rxRefclkEn = 1 (reg7[0]) and Rx VCOCAL = x0b (reg8[2:1]), then the dynamic register write to register 98 is not necessary.

In addition, for proper LOL performance, RxPDGainAcq (Register 77) must be written once to 0Dh after power is applied or a SW reset is implemented. If a valid reference clock is applied at pins 13,14 and rxRefclkEn = 1 (reg7[0]) and Rx VCOCAL = x0b (reg8[2:1]), then it is not necessary to write to register 77.

### 5.8.2. Frequency LOL

The Si5040 supports the use of a ~622 MHz or ~155 MHz (/64 or /16) reference clock. The reference clock frequency is selected in the ChipConfig1 register (Register 2). There are two ways in which FREQLOL is selected. When register7[3:2] = 10b, then FREQLOL is selected. When register7[3] = 0 and register7[1] = 1, then FREQLOL is selected. LOL is asserted if the recovered clock frequency deviates from the reference clock frequency by >±1000 ppm. LOL is de-asserted if the recovered clock is within ±200 ppm of the reference clock frequency. Refer to Figure 14 for CDR and VCO behaviors upon declaring LOL.

### 5.8.3. Acquisition Time Enhancement

The acquisition lock time for a signal applied at RXDIN can be reduced to less than 15 ms by the following register writes:

1. Write register 86 = 0011 1000 = 38h.
2. Write register 67 = 0100 0001 = 41h.
3. Write register 68 = 0000 0011 = 03h.

### 5.8.4. LOL Interrupt

LOL may be configured to generate an interrupt. The status of the LOL interrupt bit can be read from the RxintStatus register (Register 5). The status of LOL may also be read from the RxAlarmStatus register (Register 9). LOL may also be asserted upon activation of LOS (see "5.4. Receiver Loss of Signal Alarm (LOS)" on page 20 and Figure 15 on page 26). Receive data (RD) may be squelched on LOL. This option is configured in the RxdPathConfig register (Register 28).