Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

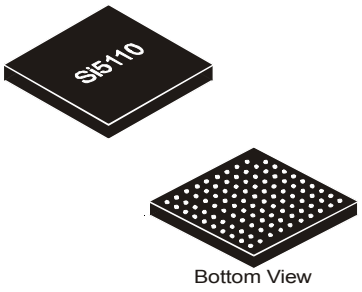
Si5110

SiPHY® OC-48/STM-16 SONET/SDH TRANSCEIVER

Features

Complete low-power, high-speed, SONET/SDH transceiver with integrated limiting amp, CDR, CMU, and MUX/DEMUX.

- Data rates supported: OC-48/STM-16 through 2.7 Gbps FEC
- Low-power operation 1.0 W (typ)
- DSPLL® based clock multiplier unit with selectable loop filter bandwidths
- Integrated limiting amplifier
- Diagnostic and line loopbacks
- SONET-compliant loop-timed operation
- Programmable slicing level and sample phase adjustment
- LVDS parallel interface
- Single supply 1.8 V operation
- 11 x 11 mm BGA package



Ordering Information:

See page 32.

Applications

- SONET/SDH transmission systems
- Optical transceiver modules
- SONET/SDH test equipment

Description

The Si5110 is a complete low-power transceiver for high-speed serial communication systems operating between OC-48 and 2.7 Gbps. The receive path consists of a fully-integrated limiting amplifier, clock and data recovery unit (CDR), and 1:4 deserializer. The transmit path combines a low-jitter clock multiplier unit (CMU) with a 4:1 serializer. The CMU uses Silicon Laboratories' DSPLL® technology to provide superior jitter performance while reducing design complexity by eliminating external loop filter components. To simplify BER optimization in long haul applications, programmable slicing and sample phase adjustment are supported. The Si5110 operates from a single 1.8 V supply over the industrial temperature range (–20 to 85 °C).

Functional Block Diagram

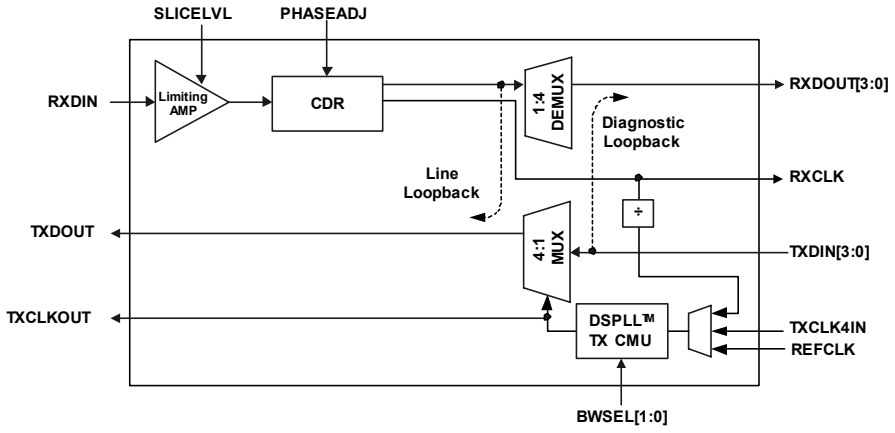
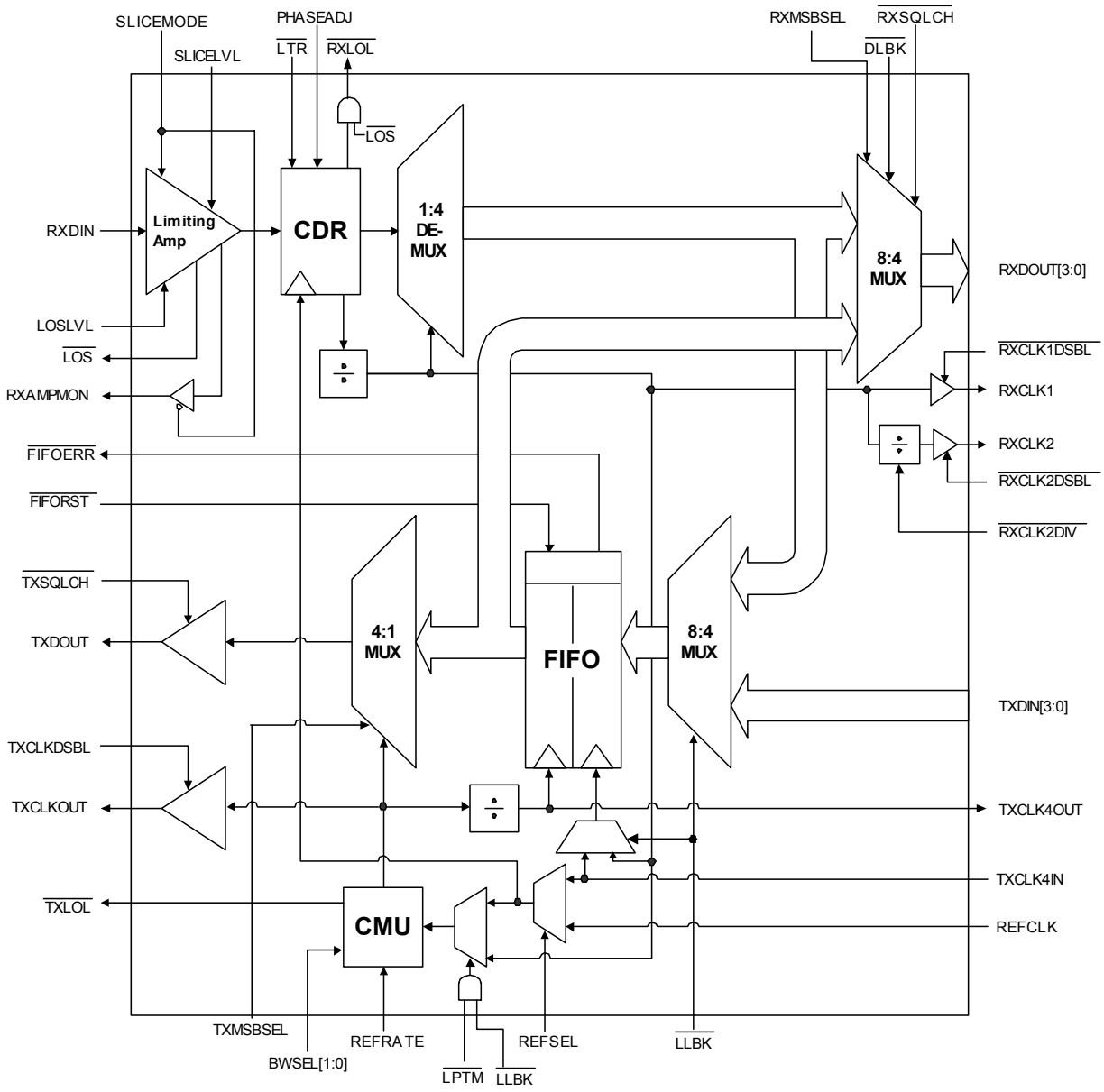


TABLE OF CONTENTS

1. Detailed Block Diagram



2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A		–20	25	85	°C
LVTTL I/O Supply Voltage	V_{DDIO}		1.71	—	3.47	V
Si5110 Supply Voltage	V_{DD}		1.71	1.8	1.89	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

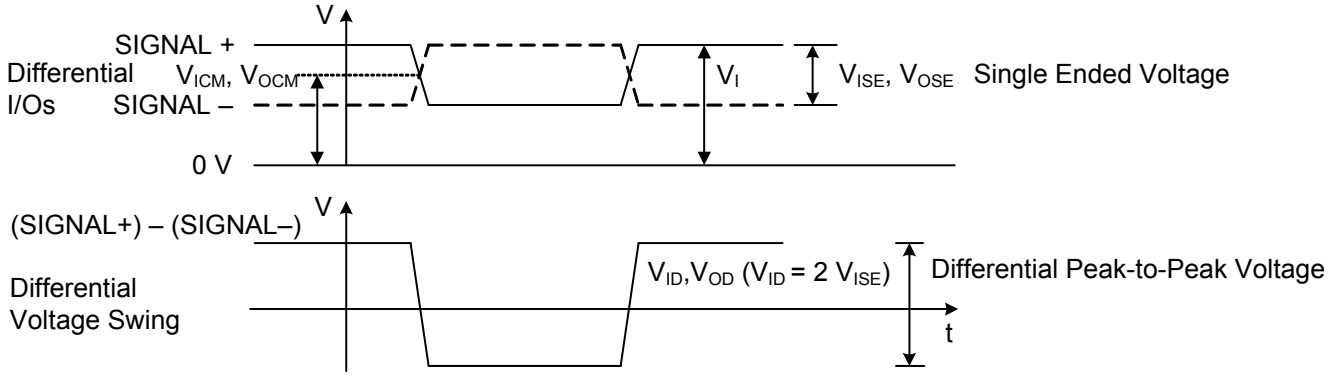


Figure 1. Differential Voltage Measurement
(RXDIN, RXDOUT, RXCLK1, RXCLK2, TXDIN, TXDOUT, TXCLKOUT, TXCLK4OUT, TXCLK4IN)

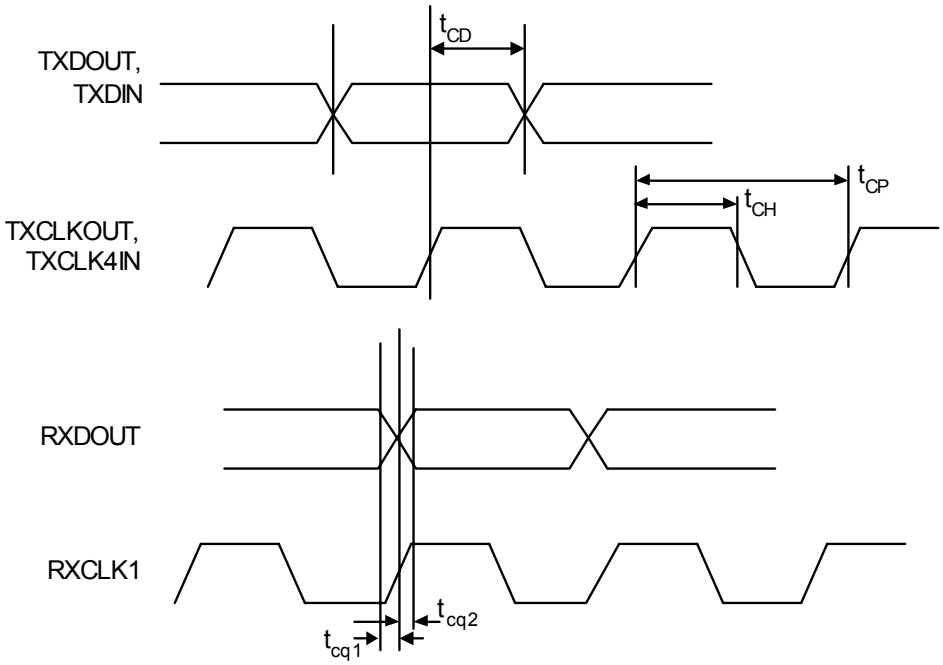


Figure 2. Data to Clock Delay

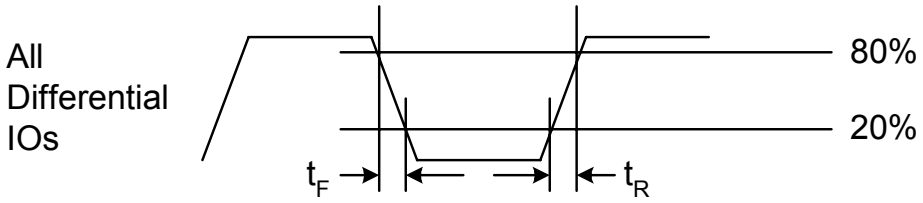


Figure 3. I/O Rise/Fall Times

Table 2. DC Characteristics
(V_{DD} = 1.8 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}	Full Duplex	—	575	640	mA
		Line/Diagnostic Loopback	—	635	700	mA
Power Dissipation	P_D	Full Duplex	—	1.0	1.2	W
		Line/Diagnostic Loopback	—	1.1	1.3	W
Voltage Reference (VREF)	V_{REF}	VREF driving 10 kΩ load	1.21	1.25	1.29	V
Common Mode Input Voltage (RXDIN)	V_{ICM}		0.4	0.5	0.6	V
Differential Input Voltage Swing (RXDIN) (at bit error rate of 10^{-12})	V_{ID}	Figure 1	30	—	2000*	mV_{PPD}
Common Mode Output Voltage (TXDOUT, TXCLKOUT)	V_{OCM}		0.7	0.9	1.1	V
Differential Output Voltage Swing (TXDOUT, TXCLKOUT), Differential pk-pk	V_{OD}	Figure 1	1000	1200	1400	mV_{PPD}
LVPECL Input Common Mode Voltage (REFCLK)	V_{ICM}		0.8	1.2	2.4	V
LVPECL Input Voltage Swing, Differential pk-pk (REFCLK)	V_{ID}	Figure 1	250	—	2400	mV_{PPD}
LVPECL Input Limits	V_{LIMIT}		0	—	2.5	V
LVDS Input Voltage Level (TXDIN, TXCLK4IN)	V_I		0.8	1.2	2.4	V
LVDS Input Voltage, Differential (TXDIN, TXCLK4IN)	V_{ID}		200	—	—	mV_{PPD}
LVDS Output Voltage Level (RXDOUT, RXCLK1, RXCLK2, TXCLK4OUT)	V_O	100 Ω Load Line-to-Line	0.925	—	1.475	V

***Note:** Voltage on RXDIN+ or RXDIN– should not exceed 1000 mV_{PP} (single-ended)

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVDS Output Voltage, Differential (RXDOUT, RXCLK1, RXCLK2, TXCLK4OUT)	V_{OD}	100 Ω Load Line-to-Line Figure 1	550	650	800	mV_{PPD}
LVDS Common Mode Output Voltage (RXDOUT, RXCLK1, RXCLK2, TXCLK4OUT)	V_{CM}		1.125	1.2	1.275	V
Input Impedance (RXDIN)	R_{IN}	Each input to common mode	42	50	58	Ω
LVDS and LVPECL Input Impedance (TXDIN, TXCLK4IN, REFCLK)	R_{IN}	Line to line	90	110	130	Ω
CML Output Impedance (TXDOUT, TXCLKOUT)	R_{OUT}	Each output to common mode	45	55	65	Ω
LVDS Output Impedance (RXDOUT, RXCLK1, RXCLK2, TXCLK4OUT)	R_{OUT}	Each output to common mode	45	55	65	Ω
Output Current Short to GND (RXDOUT, RXCLK1, RXCLK2, TXCLK4OUT)	$I_{SC(–)}$		—	12	40	mA
Input Impedance (LOSLVL, SLICELVL, PHASEADJ)	R_{IN}		100	—	—	kΩ
Output Impedance (RXAMPMON)	R_{OUT}		4	6	8	kΩ
Output Current Short to V_{DD} (RXDOUT, RXCLK1, RXCLK2, TXCLK4OUT)	$I_{SC(+)}$		–8	–6	—	mA
LVTTL Input Voltage Low	V_{IL2}	V_{DDIO} = 1.8–3.3 V	–0.3	—	0.35 V_{DDIO}	V
LVTTL Input Voltage High	V_{IH2}	V_{DDIO} = 1.8–3.3 V	0.65 V_{DDIO}	—	V_{DDIO} + 0.3	V
LVTTL Input Impedance	R_{IN}		10	—	—	kΩ
LVTTL Output Voltage Low (I_{OUT} = 2 mA)	V_{OL2}	V_{DDIO} = 1.8–3.3 V	—	—	0.4	V
LVTTL Output Voltage High (I_{OUT} = 2 mA)	V_{OH2}	V_{DDIO} = 1.8–3.3 V	V_{DDIO} – 0.45	—	—	V
***Note:** Voltage on RXDIN+ or RXDIN– should not exceed 1000 mV_{PP} (single-ended)						

Table 3. AC Characteristics (RXDIN, RXDOUT, RXCLK1, RXCLK2)
(V_{DD} = 1.8 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Data Rate (RXDIN)			2.41	—	2.7	Gbps
Output Clock Frequency (RXCLK1)	f_{clkout}		—	622	675	MHz
Output Clock Frequency (RXCLK2)	f_{clkout}	$\overline{RXCLK2DIV}$ = 1 $\overline{RXCLK2DIV}$ = 0	— —	622 155	675 169	MHz MHz
Duty Cycle (RXCLK1, RXCLK2)		tch/tcp, Figure 2	45	—	55	%
Output Rise and Fall Times (RXCLK1, RXCLK2, RXDOUT)	t_R,t_F	Figure 3	100	175	250	ps
Data Invalid Prior to RXCLK1	t_{cq1}	Figure 2	—	—	200	ps
Data Invalid After RXCLK1	t_{cq2}	Figure 2	—	—	200	ps
Input Return Loss (RXDIN)	S_{11}	≤1.25 GHz 2.5 GHz	— —	–12 –10	— —	dB dB
LOS Threshold, SLICEMODE = 0[1]	V_{LOS}	LOSLVL = 0–350 mV	0	—	250	mV
LOS Threshold Error, SLICEMODE = 0[1]			—	—	±30	%
LOS Threshold, SLICEMODE = 1[2]	V_{LOS}	LOSLVL = 0–500 mV	0	—	60	mV
LOS Threshold Error, SLICEMODE = 1[2]			—	—	±50	%
Slice Voltage, SLICEMODE = 0[3]	V_{LEVEL}	SLICELVL = 350 mV	—	–50	—	mV
		SLICELVL = 650 mV	—	40	—	mV
Slice Voltage as Percentage of Differential Input Voltage Swing (RXDIN), SLICEMODE = 1[4]	V_{LEVEL}	SLICELVL = 250 mV	—	–25	—	%
		SLICELVL = 750 mV	—	18	—	%
Slice Voltage as Percentage of Differential Input Voltage Swing (RXDIN) Error, SLICEMODE = 1[4]		SLICELVL = 200 mV	—	–25	—	%
		SLICELVL = 800 mV	—	18	—	%
Sample Phase Offset[5]		PHASEADJ = 200 mV	—	–25	—	ps
		PHASEADJ = 800 mV	—	25	—	ps
RXAMPMON Voltage Range		RXDIN = 0–1000 mV_{PPD}	0	—	550	mV
RXAMPMON Voltage Error			—	±50	—	%

Notes:
1. See Figure 4 on page 15.
2. See Figure 5 on page 16.
3. See Figure 6 on page 16.
4. See Figure 7 on page 17.
5. See Figure 8 on page 17.

Table 4. AC Characteristics (TXCLK4OUT, TXCLK4IN, TXCLKOUT, TXDIN, TXDOUT)
(V_{DD} = 1.8 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TXCLKOUT Frequency	f_{clkout}	Figure 2	2.41	—	2.7	GHz
TXCLKOUT Duty Cycle		tch/tcp, Figure 2	40	50	60	%
Output Rise Time (TXCLKOUT, TXDOUT)	t_R	Figure 3	—	50	75	ps
Output Fall Time (TXCLKOUT, TXDOUT)	t_F	Figure 3	—	50	75	ps
TXCLKOUT to TXDOUT Delay	t_{cd}	Figure 2	–42	—	–22	ps
Output Return Loss		100 kHz–2.5 GHz 2.5 GHz–4.0 GHz	— —	–12 –10	— —	dB dB
TXCLK4OUT Frequency	f_{CLKOUT}		—	622	675	MHz
TXCLK4OUT Duty Cycle		tch/tcp, Figure 2	40	—	60	%
TXCLK4OUT Rise & Fall Times	t_R,t_F		100	175	250	ps
TXDIN Setup to TXCLK4IN	t_{DSIN}		—	—	300	ps
TXDIN Hold from TXCLK4IN	t_{DHIN}		—	—	300	ps
TXCLK4IN Frequency	f_{CLKIN}		—	622	675	MHz
TXCLK4IN Duty Cycle		tch/tcp, Figure 2	40	—	60	%
TXCLK4IN Rise & Fall Times	t_R,t_F		100	—	300	ps

Table 5. AC Characteristics (Receiver PLL)
(V_{DD} = 1.8 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance (RXDIN = 100 mV_{PPD}, PRBS31) ***Note:** Instrument Limited	$J_{TOL(PP)}$	f = 10–600 Hz	15*	—	—	UI_{PP}
		f = 0.6–6 kHz	15*	—	—	UI_{PP}
		f = 6–100 kHz	9*	—	—	UI_{PP}
		f = 100 kHz–1 MHz	0.4			UI_{PP}
		f = 1–20 MHz	0.3	—	—	UI_{PP}
Acquisition Time	T_{AQ}		—	—	2	ms
Input Reference Clock Frequency (REFSEL = 1)	RC_{FREQ}	REFRATE = 1	—	155	169	MHz
		REFRATE = 0	—	78	84.4	MHz
Reference Clock Duty Cycle	RC_{DUTY}		40	50	60	%
Reference Clock Frequency Tolerance	RC_{TOL}		–100	—	100	ppm
Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock)	$\overline{LOL}$		610	732	860	ppm
Frequency Difference at which Receive PLL goes into Lock (REFCLK compared to the divided down VCO clock)	LOCK		—	366	240	ppm
Note: Bellcore specifications: GR-253-CORE, Issue 3, September 2000.						

Table 6. AC Characteristics (Transmitter Clock Multiplier)[1]
(V_{DD} = 1.8 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Transfer Bandwidth OCH48: 2.48832 Gbps FEC: 2.666676 Gbps	J_{BW}	BWSEL[1:0] = 00 BWSEL[1:0] = 01 BWSEL[1:0] = 10 BWSEL[1:0] = 11	— — — —	— — — —	12 50 120 200	kHz kHz kHz kHz
Jitter Transfer Peaking			—	0.05	0.1	dB
Acquisition Time	T_{AQ}	Valid REFCLK BWSEL[1:0] = 11	—	—	20	ms
Input Reference Clock Frequency	RC_{FREQ}	REFRATE = 1	—	155	169	MHz
		REFRATE = 0	—	78	84.4	MHz
Input Reference Clock Duty Cycle	RC_{DUTY}		40	—	60	%
Input Reference Clock Frequency Tolerance	RC_{TOL}		–100	—	100	ppm
Random rms Jitter Generation, TXCLKOUT (PRBS 31)[2]	$J_{GEN(rms)}$	BWSEL[1:0] = 00 BWSEL[1:0] = 01 BWSEL[1:0] = 10 BWSEL[1:0] = 11		2.6 2.0 1.7 1.7	3.7 2.6 2.1 2.1	mUI_{rms} mUI_{rms} mUI_{rms} mUI_{rms}
Random Peak-to-Peak Jitter Generation, TXCLKOUT (PRBS 31)[2]	$J_{GEN(PP)}$	BWSEL[1:0] = 00 BWSEL[1:0] = 01 BWSEL[1:0] = 10 BWSEL[1:0] = 11		25 23 22 21	36 32 28 27	mUI_{PP} mUI_{PP} mUI_{PP} mUI_{PP}

Notes:
1. Bellcore specifications: GR-253-CORE, Issue 3, September 2000.
2. Full duplex, REFCLK = 155 MHz.

Table 7. Absolute Maximum Ratings

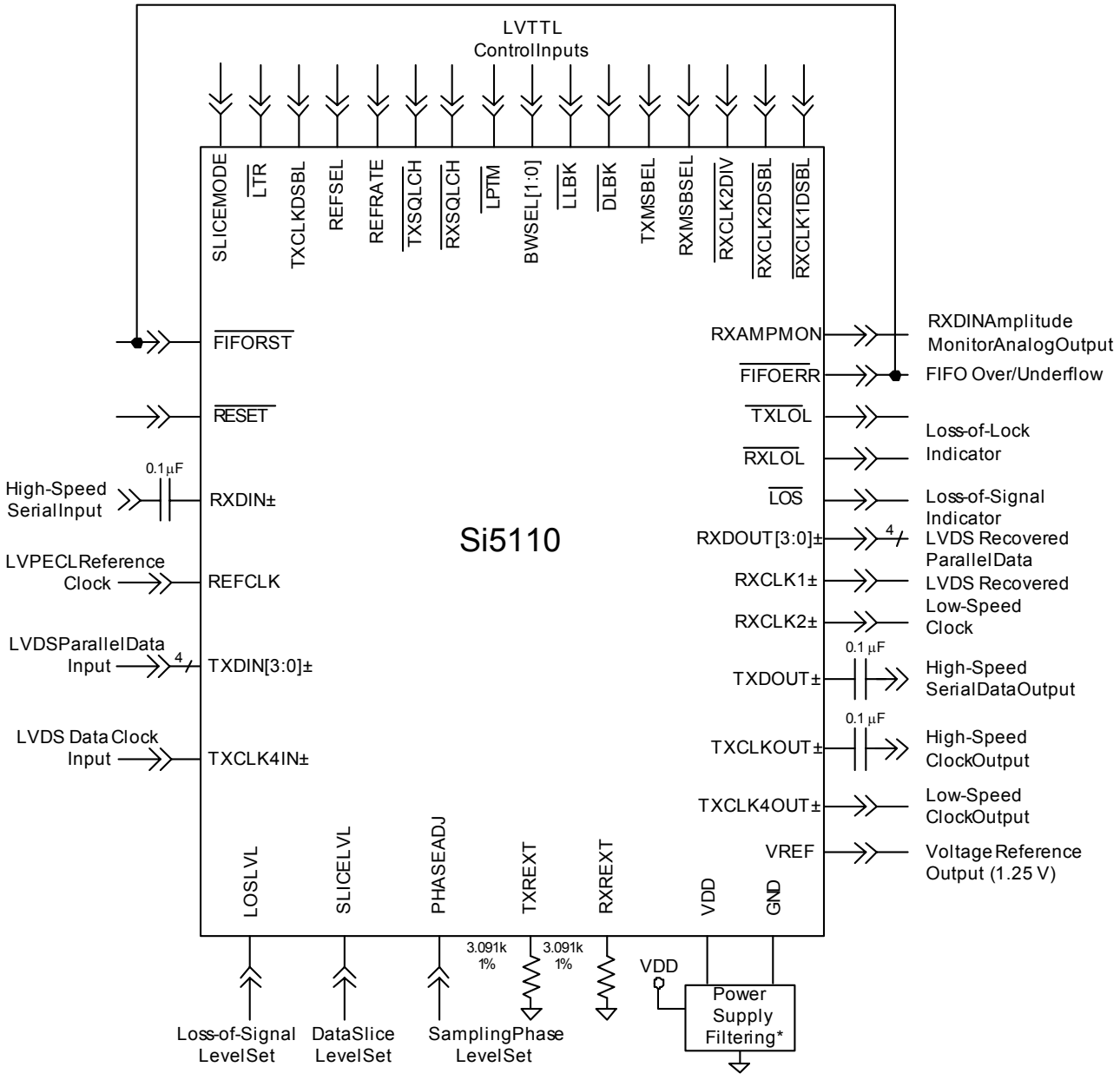
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.2	V
LVTTL I/O Supply Voltage	V_{DDIO}	–0.5 to 4.0	V
Differential Input Voltage (LVDS Input)	V_{DIF}	5	V
Differential Input Voltage (LVDS Output)	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Differential Input Voltage (LVTTL Input)	V_{DIF}	2.4	V
Differential Input Voltage (LVTTL Output)	V_{DIF}	5	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM (2.5 GHz Pins)		1	kV
ESD HBM Tolerance (100 pF, 1.5 kΩ)		2	kV

Note: Permanent device damage can occur if the above Absolute Maximum Ratings are exceeded. Restrict functional operation to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	31	°C/W

3. Typical Application Schematic



Note* See 15. "Power Supply Filtering" on page 20.

4. Functional Description

The Si5110 transceiver is a low-power, fully-integrated serializer/deserializer that provides significant margin to all SONET/SDH jitter specifications. The device operates from 2.4–2.7 Gbps making it suitable for OC-48/STM-16 applications, and OC-48/STM-16 applications that use 255/238 or 255/237 forward error correction (FEC) coding. The low-speed receive/transmit interface uses a low-power parallel LVDS interface.

5. Receiver

The receiver within the Si5110 includes a precision limiting amplifier, a jitter-tolerant clock and data recovery unit (CDR), and 1:4 demultiplexer. Programmable data slicing level and sampling phase adjustment are provided to support bit-error-rate (BER) optimization for long haul applications.

5.1. Receiver Differential Input Circuitry

The receiver serial input provides proper termination and biasing through two resistor dividers internal to the device. The active circuitry has high-impedance inputs and provides sufficient gain for the clock and data recovery unit to recover the serial data. The input bias levels are optimized for jitter tolerance and input sensitivity and are typically not dc compatible with standard I/Os; simply ac couple the data lines as shown in Figure 10.

5.2. Limiting Amplifier

The Si5110 incorporates a limiting amplifier with sufficient gain to directly accept the output of transimpedance amplifiers.

The limiting amplifier provides sufficient gain to fully saturate with input signals that are greater than 30 mV peak-to-peak differential. In addition, input signals up to 2 V peak-to-peak differential do not cause any performance degradation.

5.2.1. Receiver Signal Amplitude Monitoring

The Si5110 limiting amplifier includes circuitry that monitors the amplitude of the receiver differential input signal (RXDIN). The RXAMPMON output provides an analog output signal that is proportional to the input signal amplitude. The signal is enabled when SLICEMODE is asserted. The voltage on the RXAMPMON output is nominally equal to one-half of the differential peak-to-peak signal amplitude of RXDIN as shown in Equation 1.

$$V_{RXAMPMON} \approx (V_{RXDIN(PP)} \times .566)$$

Equation 1

The receiver signal amplitude monitoring circuit is also used in the generation of the loss-of-signal alarm ($\overline{LOS}$).

5.2.2. Loss-of-Signal Alarm ($\overline{LOS}$)

The Si5110 can be configured to activate a loss-of-signal alarm output ($\overline{LOS}$) when the RXDIN input amplitude drops below a programmable threshold level. An appropriate level of hysteresis prevents unnecessary switching on $\overline{LOS}$.

The $\overline{LOS}$ threshold level is set by applying a dc voltage to the LOSLVL input. The mapping of the voltage on the LOSLVL pin to the $\overline{LOS}$ threshold level depends on the state of the SLICEMODE input. (The SLICEMODE input is used to select either Absolute Slice mode or Proportional Slice mode operation.)

The LOSLVL mapping for Absolute Slice Mode (SLICEMODE = 0) is given in Figure 4 on page 15. The linear region of the assert can be approximated by the following equation:

$$V_{LOS} \approx V_{LOSLVL} \times 0.958$$

Equation 2

where V_{LOS} is the differential pk-pk $\overline{LOS}$ threshold referred to the RXDIN input, and V_{LOSLVL} is the voltage applied to the LOSLVL pin. The linear region of the de-assert curve can be approximated by the following equation:

$$V_{LOS} \approx V_{LOSLVL} \times 0.762$$

Equation 3

The LOSLVL mapping for Proportional Slice mode (SLICEMODE = 1) is given in Figure 5 on page 16. The linear region of the assert can be approximated by the following equation:

$$V_{LOS} \approx V_{LOSLVL} \times 0.61$$

Equation 4

where V_{LOS} is the differential pk-pk $\overline{LOS}$ threshold referred to the RXDIN input, and V_{LOSLVL} is the voltage applied to the LOSLVL pin.

The linear region of the assert curve can be approximated be the following equation:

$$V_{LOS} \approx V_{LOSLVL} \times 0.72$$

Equation 5

The $\overline{\text{LOS}}$ detection circuitry is disabled by tieing the LOSLVL input to VREF. This forces the $\overline{\text{LOS}}$ output high.

5.2.3. Slice Level Adjustment

The limiting amplifier allows adjustment of the 0/1 decision threshold, or slice level, to allow optimization of bit-error-rates (BER) for demanding applications such as long-haul links. The Si5110 provides two different modes of slice level adjustment: Absolute Slice mode and Proportional Slice mode. The mode is selected using the SLICEMODE input.

In either mode, the slice level is set by applying a dc voltage to the SLICELVL input. The mapping of the voltage on the SLICELVL pin to the 0/1 decision threshold voltage (or slice voltage) depends on the selected mode of operation.

The SLICELVL mapping for Absolute Slice mode (SLICEMODE = 0) is given in Figure 6 on page 16. The linear region of this curve can be approximated by the following equation:

$$V_{LEVEL} \approx ((V_{SLICELVL} - (VREF \times 0.4)) \times 0.375) - 0.005$$

Equation 6

where V_{LEVEL} is the effective slice level referred to the RXDIN input, $V_{SLICELVL}$ is the voltage applied to the SLICELVL pin, and VREF is the reference voltage provided by the Si5110 on the VREF output pin (nominally 1.25 V).

The SLICELVL mapping for Proportional Slice mode (SLICEMODE = 1) is given in Figure 7 on page 17. The linear region of this curve can be approximated by the following equation:

$$V_{LEVEL} = [(V_{SLICELVL} - (VREF \times 0.4)) \times (V_{RXDIN(PP)} \times 0.95)] - [0.03 \times V_{RXDIN(PP)}]$$

Equation 7

where V_{LEVEL} is the effective slice level referred to the RXDIN input, $V_{SLICELVL}$ is the voltage applied to the SLICELVL pin, VREF is the reference voltage provided by the Si5110 on the VREF output pin, and $V_{RXDIN(PP)}$ is the peak-to-peak voltage level of the receive data signal applied to the RXDIN input.

The slice level adjustment function can be disabled by tieing the SLICELVL input to VREF. When slice level adjustment is disabled, the effective slice level is set to 0 mV relative to internally biased input common mode voltage for RXDIN.

5.3. Clock and Data Recovery (CDR)

The Si5110 uses an integrated CDR to recover clock and data from a non-return to zero (NRZ) signal input on RXDIN. The recovered clock is used to regenerate the incoming data by sampling the output of the limiting amplifier at the center of the NRZ bit period.

5.3.1. Sample Phase Adjustment

In applications where data eye distortions are introduced by the transmission medium, it may be desirable to recover data by sampling at a point that is not at the center of the data eye. The Si5110 provides a sample phase adjustment capability that allows adjustment of the CDR sampling phase across the NRZ data period. When sample phase adjustment is enabled, the sampling instant used for data recovery can be moved over a range of approximately ±22 ps relative to the center of the incoming NRZ bit period.

The sample phase is set by applying a dc voltage to the PHASEADJ input. The mapping of the voltage present on the PHASEADJ input to the sample phase sampling offset is given in Figure 8. The linear region of this curve can be approximated by the following equation:

$$\text{Phase Offset} \approx 85\ \text{ps/V} \times (V_{PHASEADJ} - (0.4 \times VREF))$$

Equation 8

where Phase Offset is the sampling offset in picoseconds from the center of the data eye, $V_{PHASEADJ}$ is the voltage applied to the PHASEADJ pin, and VREF is the reference voltage provided by the Si5110 on the VREF output pin (nominally 1.25 V). A positive phase offset adjusts the sampling point to lead the default sampling point (the center of the data eye) and a negative phase offset adjusts the sampling point to lag the default sampling point.

Data recovery using a sampling phase offset is disabled by tieing the PHASEADJ input to VREF. This forces a phase offset of 0 ps to be used for data recovery.

5.3.2. Receiver Lock Detect

The Si5110 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. This circuit compares the frequency of a divided down version of the recovered clock with the frequency of the supplied reference clock. The Si5110 will use either REFCLK or TXCLK4IN as the reference clock input signal, depending on the state of the REFSEL input. If the (divided) recovered clock frequency deviates from that of the reference clock by more than the amount specified in Table 5 on page 9, the CDR is declared out of lock, and the loss-of-lock ($\overline{\text{RXLOL}}$) pin is asserted. In this state, the CDR attempts to reacquire lock with the incoming data stream. During

reacquisition, the recovered clock frequency (RXCLK1 and RXCLK2) drifts over a range of approximately ±1000 ppm relative to the supplied reference clock unless LTR is asserted. The RXLOL output remains asserted until the frequency of the (divided) recovered clock differs from the reference clock frequency by less than the amount specified in Table 5 on page 9.

The RXLOL output will be asserted automatically if a valid reference clock is not detected.

The RXLOL output will also be asserted whenever the loss of signal alarm (LOS) is active, provided that the LTR input is set high (i.e., provided that the device is not configured for Lock-to-Reference mode).

5.3.3. Lock-to-Reference

The lock-to-reference (LTR) input can be utilized to ensure the presence of a stable output clock during a loss-of-signal alarm (LOS). When LTR is asserted, the CDR is prevented from phase locking to the data signal and the CDR locks the RXCLKOUT1 and RXCLKOUT2 outputs to the reference clock. In typical applications, the LOS output is tied to the LTR input to force a stable output clock during a loss-of-signal condition.

5.4. Deserialization

The Si5110 uses a 1:4 demultiplexer to deserialize the high-speed input. The deserialized data is output on a 4-bit parallel data bus, RXDOUT[3:0], aligned with the rising edge of RXCLK1.

5.4.1. Serial Input to Parallel Output Relationship

The Si5110 provides the capability to select the order in which the received serial data is mapped to the parallel output bus RXDOUT[3:0]. The mapping of the receive bits to the output data word is controlled by the RXMSBSEL input. When RXMSBSEL is set low, the first bit received is output on RXDOUT0, and the following bits are output in order on RXDOUT1 through RXDOUT3. When RXMSBSEL is set high, the first bit received is output on RXDOUT3, and the following bits are output in order on RXDOUT2 through RXDOUT0.

5.5. Voltage Reference Output

The Si5110 provides an output voltage reference that can be used by external circuitry to set the LOS threshold, slicing level, or sampling phase adjustment input voltage levels. One possible implementation uses a resistor divider to set the control voltage for the LOSLVL, SLICELVL, or PHASEADJ inputs. An alternative is the use of digital-to-analog converters (DACs) to set the control voltages. Using this approach, VREF is used to set the range of the DAC outputs. The voltage on the VREF output is nominally 1.25 V.

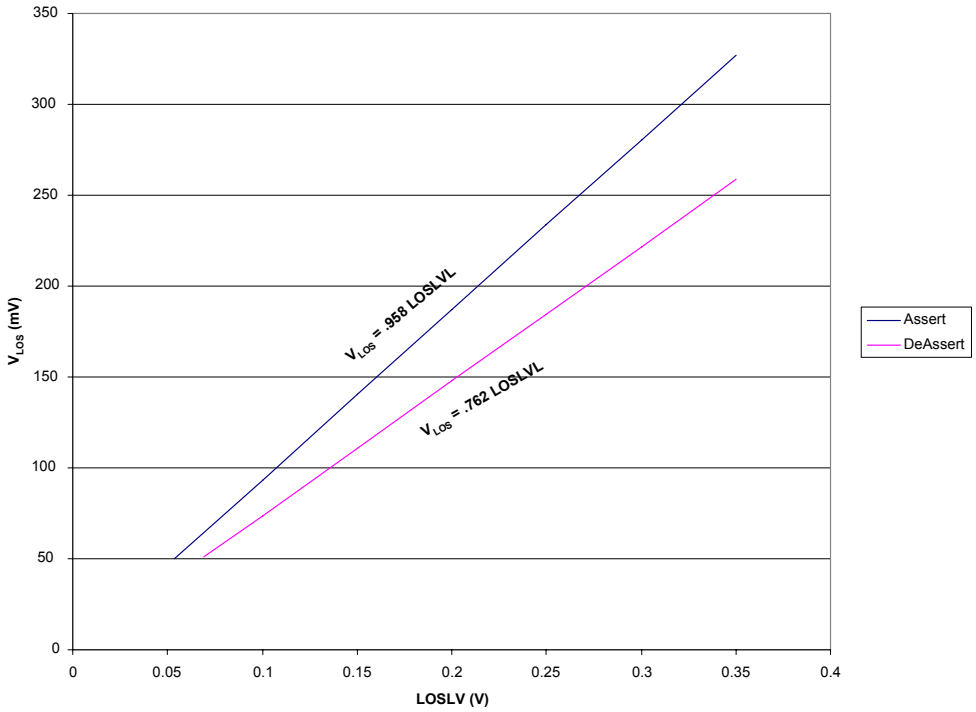


Figure 4. Typical LOSLVL Transfer Curve, Absolute Slice Mode (SLICEMODE = 0)

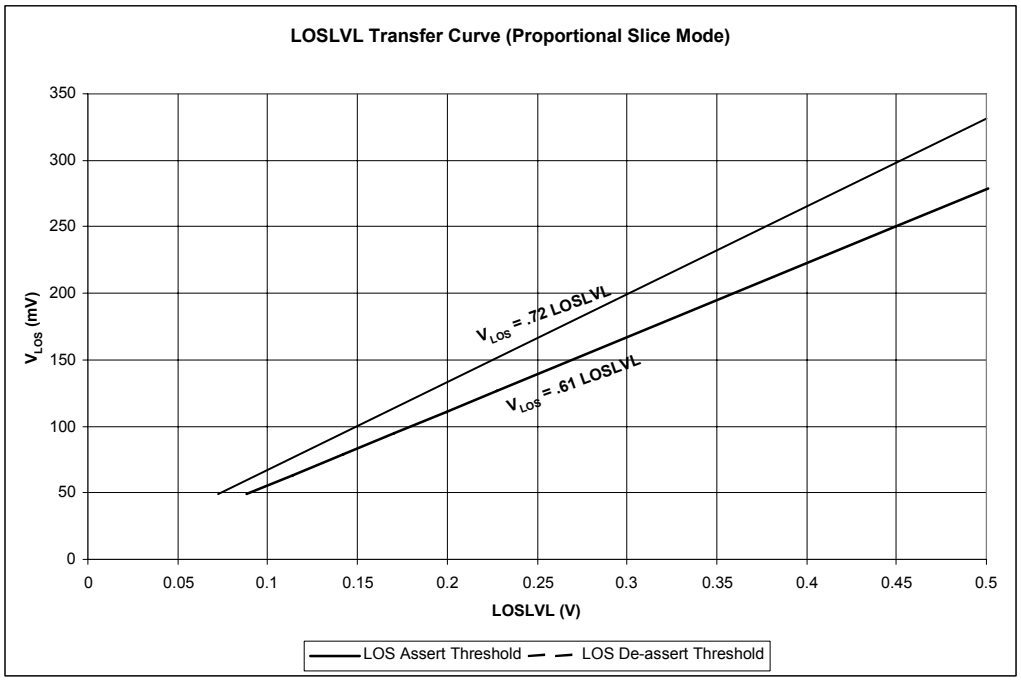


Figure 5. Typical LOSLVL Transfer Curve, Proportional Slice Mode (SLICEMODE = 1)

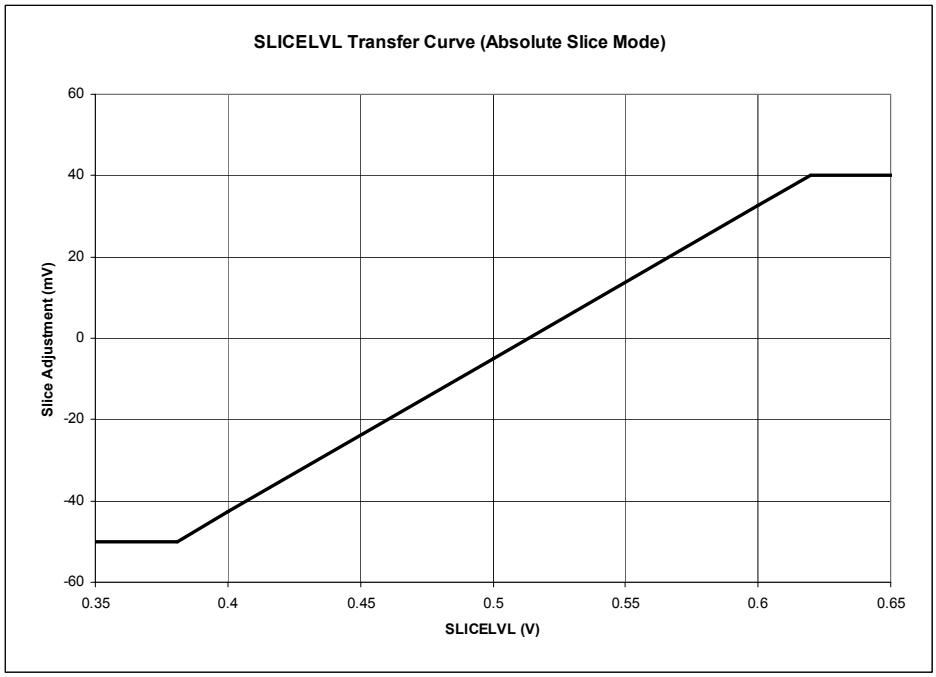


Figure 6. Typical SLICELVL Transfer Curve, Absolute Slice Mode (SLICEMODE = 0)

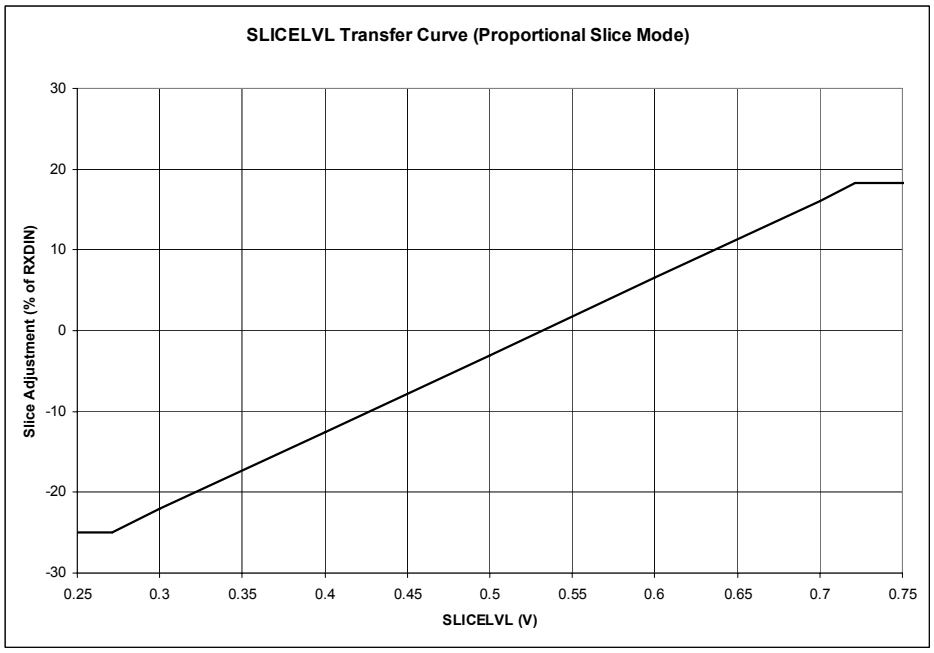


Figure 7. Typical SLICELVL Transfer Curve, Proportional Slice Mode (SLICEMODE = 1)

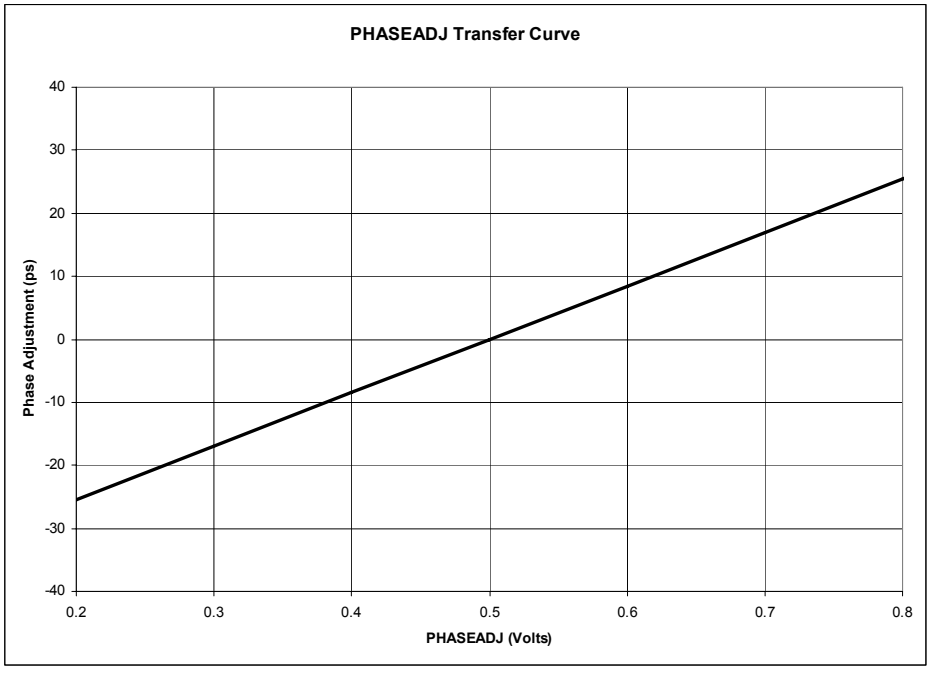


Figure 8. Typical PHASEADJ Transfer Curve

5.6. Auxiliary Clock Output

To support the widest range of system timing configurations, The Si5110 provides a primary clock output on RXCLK1 and a secondary clock output (RXCLK2). The RXCLK2 output can be configured to provide a clock that is 1/4th or 1/16th the frequency of the high-speed recovered clock. The divide ratio which determines the RXCLK2 output frequency is selected by RXCLK2DIV.

5.7. Receive Data Squelch

During some system error conditions, such as $\overline{\text{LOS}}$, it may be desirable to force the receive data output to zero in order to avoid propagation of erroneous data into the downstream electronics. The Si5110 provides a data squelching control input, $\overline{\text{RXSQLCH}}$, for this purpose.

When the $\overline{\text{RXSQLCH}}$ input is low, the data outputs RXDOUT[3:0] are forced to a zero state. The $\overline{\text{RXSQLCH}}$ input is ignored when the device is operating in Diagnostic Loopback mode ($\overline{\text{DLBK}}$ = 0).

6. Transmitter

The transmitter consists of a low jitter clock multiplier unit (CMU) with a 4:1 serializer. The CMU uses a phase-locked loop (PLL) architecture based on Silicon Laboratories' proprietary DSPLL technology. This technology generates ultra-low jitter clock and data outputs that provide significant margin to the SONET/SDH specifications. The DSPLL architecture also utilizes a digitally implemented loop filter that eliminates the need for external loop filter components. As a result, sensitive noise coupling nodes that typically degrade jitter performance in crowded PCB environments are removed.

The DSPLL also reduces the complexity and relaxes the performance requirements for reference clock distribution circuitry for OC-48/STM-16 optical port cards. The DSPLL provides selectable wideband and narrowband loop filter settings that allow the jitter attenuation characteristics of the CMU to be optimized for the jitter content of the supplied reference clock. This allows the CMU to operate with reference clocks that have relatively high jitter content.

Unlike traditional analog PLL implementations, the loop filter bandwidth of the Si5110 transmitter CMU is controlled by a digital filter inside the DSPLL circuit allowing the bandwidth to be changed without changing any external component values.

6.1. DSPLL® Clock Multiplier Unit

The Si5110's clock multiplier unit (CMU) uses Silicon Laboratories proprietary DSPLL technology to achieve optimal jitter performance. The DSPLL implementation utilizes a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage-controlled oscillator (VCO). The DSPLL implementation requires no external loop filter components. Eliminating sensitive noise entry points makes the DSPLL implementation less susceptible to board-level noise sources and makes SONET/SDH jitter compliance easier to attain in the application.

The transmit CMU multiplies the frequency of the selected reference clock up to the serial transmit data rate. The $\overline{\text{TXLOL}}$ output signal provides an indication of the transmit CMU lock status. When the CMU has achieved lock with the selected reference, the $\overline{\text{TXLOL}}$ output is deasserted (driven high). The $\overline{\text{TXLOL}}$ signal will be asserted, indicating a transmit CMU loss-of-lock condition, when a valid clock signal is not detected on the selected reference clock input. The $\overline{\text{TXLOL}}$ signal will also be asserted during the transmit CMU frequency calibration. Calibration is performed automatically when the Si5110 is powered on, when a valid clock signal is detected on the selected reference clock input following a period when no valid clock was present, or when the frequency of the selected reference clock is outside of the transmit CMU's PLL lock range or after RESET is deasserted.

6.1.1. Programmable Loop Filter Bandwidth

The digitally implemented loop filter allows for four transmit CMU loop bandwidth settings that provide wideband or narrowband jitter transfer characteristics. The filter bandwidth is selected via the BWSEL[1:0] control inputs. The loop bandwidth choices are listed in Table 6. Unlike traditional PLL implementations, changing the loop filter bandwidth of the Si5110 is accomplished without the need to change external component values.

Lower loop bandwidth settings (Narrowband operation) make the Si5110 more tolerant to jitter on the reference clock source. As a result, circuitry used to generate and distribute the physical layer reference clocks can be simplified without compromising margin to the SONET/SDH jitter specifications.

Higher loop bandwidth settings (Wideband operation) are useful in applications where the reference clock is provided by a low jitter source like the Si5364 Clock Synchronization IC or Si5320 Precision Clock

Multiplier/Jitter Attenuator IC. Wideband operation allows the DSPLL to more closely track the precision reference source, resulting in the best possible jitter performance.

6.2. Serialization

The Si5110 serialization circuitry is comprised of a FIFO and a parallel to serial shift register. Low-speed data on the parallel 4-bit input bus, TXDIN[3:0], is latched into the FIFO on the rising edge of TXCLK4IN. Data is clocked out of the FIFO and into the shift register by TXCLK4OUT. The high-speed serial data stream TXDOUT is clocked out of the shift register by TXCLKOUT. The TXCLK4OUT clock is provided as an output signal to support data word transfers between the Si5110 and upstream devices using a counter clocking scheme.

6.2.1. Input FIFO

The Si5110 FIFO decouples the timing of the data transferred into the device via TXCLK4IN from the data transferred into the shift register via TXCLK4OUT. The FIFO is eight parallel words deep and accommodates any static phase delay that may be introduced between TXCLK4OUT and TXCLK4IN in counter clocking schemes. Furthermore, the FIFO accommodates a bounded phase drift, or wander, between TXCLK4IN and TXCLK4OUT of up to three parallel data words.

The FIFO circuitry indicates an overflow or underflow condition by asserting the $\overline{\text{FIFOERR}}$ signal. This output can be used to re-center the FIFO read/write pointers by tieing it directly to the $\overline{\text{FIFORST}}$ input.

The $\overline{\text{FIFORST}}$ signal causes re-centering of the FIFO read/write pointers. The Si5110 also automatically re-centers the read/write pointers after the device is powered on, after an external reset via the $\overline{\text{RESET}}$ input, and each time the DSPLL transitions from an out-of-lock state to a locked state (when $\overline{\text{TXLOL}}$ transitions from low to high).

6.2.2. Parallel Input To Serial Output Relationship

The Si5110 provides the capability to select the order in which the data received on the parallel input bus TXDIN[3:0] is transmitted serially on the high-speed serial data output TXDOUT. Data on the parallel bus will be transmitted MSB first or LSB first depending on the setting of the TXMSBSEL input. When TXMSBSEL is set low, TXDIN0 is transmitted first, followed in order by TXDIN1 through TXDIN3. When TXMSBSEL is set high, TXDIN3 is transmitted first, followed in order by TXDIN2 through TXDIN0. This feature can simplify printed circuit board (PCB) routing in applications where ICs are mounted on both sides of the PCB.

6.2.3. Transmit Data Squelch

To prevent the transmission of corrupted data into the network, the Si5110 provides a control pin that can be used to force the high-speed serial data output TXDOUT to zero. When the $\overline{\text{TXSQLCH}}$ input is set low, the TXDOUT signal is forced to a zero state. The $\overline{\text{TXSQLCH}}$ input is ignored when the device is operating in Line Loopback mode ($\overline{\text{LLBK}}$ = 0).

6.2.4. Clock Disable

The Si5110 provides a clock disable pin, TXCLKDSBL, that can be used to disable the high-speed serial data clock output, TXCLKOUT. When the TXCLKDSBL pin is asserted, the positive and negative terminals of CLKOUT are tied internally to 1.5 V through 50 Ω on-chip resistors.

This feature can be used to reduce power consumption in applications that do not use the high-speed transmit data clock.

7. Loop Timed Operation

The Si5110 can be configured to provide SONET/SDH compliant loop timed operation. When the $\overline{\text{LPTM}}$ input is set low, the transmit clock and data timing is derived from the CDR recovered clock output. This is achieved by dividing down the recovered clock and using it as a reference source for the transmit CMU. This results in transmit clock and data signals that are locked to the timing recovered from the received data path. A narrow-band loop filter setting is recommended for this mode of operation.

8. Diagnostic Loopback

The Si5110 provides a Diagnostic Loopback mode that establishes a loopback path from the serializer output to the deserializer input. This provides a mechanism for looping back data input via the low speed transmit interface TXDIN[3:0] to the low speed receive data interface RXDOUT[3:0]. This mode is enabled when the $\overline{\text{DLBK}}$ input is set low.

Note: Setting both $\overline{\text{DLBK}}$ and $\overline{\text{LLBK}}$ low simultaneously is not supported.

9. Line Loopback

The Si5110 provides a Line Loopback mode that establishes a loopback path from the high-speed receive input to the high-speed transmit output. This provides a mechanism for looping back the high-speed data and clock recovered from RXDIN to the transmit data output TXDOUT and transmit clock TXCLKOUT. This mode is enabled when the $\overline{\text{LLBK}}$ input is set low.

Note: Setting both $\overline{\text{DLBK}}$ and $\overline{\text{LLBK}}$ low simultaneously is not supported.

10. Bias Generation Circuitry

The Si5110 uses two external resistors, RXREXT and TXREXT, to set internal bias currents for the receive and transmit sections of the device, respectively. The external resistors allow precise generation of bias currents, which can significantly reduce power consumption. The bias generation circuitry requires two 3.09 kΩ (1%) resistors each connected between RXREXT and GND, and between TXREXT and GND.

11. Reference Clock

The Si5110 supports operation with one of two possible reference clock sources. In the first configuration, an external reference clock is connected to the REFCLK input. The second configuration uses the parallel data clock, TXCLK4IN, as the reference clock source. The REFSEL input is used to select whether the REFCLK or the TXCLK4IN input will be used as the reference clock.

When REFCLK is selected as the reference clock source (REFSEL = 1), two possible reference clock frequencies are supported. The reference clock frequency provided on the REFCLK input can be either 1/16th or 1/32nd the desired transceiver data rate. The REFCLK frequency is selected using the REFRATE input.

The TXCLK4IN clock frequency is equal to 1/4th the transceiver data rate. When TXCLK4IN is selected as the reference clock source (REFSEL = 0), the REFRATE input has no effect.

The CMU in the Si5110's transmit section multiplies the provided reference up to the serial transmit data rate. When the CMU has achieved lock with the selected reference, the $\overline{\text{TXLOL}}$ output is deasserted (driven high).

The CDR in the receive section of the Si5110 uses the selected reference clock to center the receiver PLL frequency in order to speed lock acquisition. When the receive CDR locks to the data input, the $\overline{\text{RXLOL}}$ signal is deasserted (driven high).

12. Reset

The Si5110 is reset by holding the $\overline{\text{RESET}}$ pin low for at least 1 μs. When $\overline{\text{RESET}}$ is asserted, the input FIFO pointers are reset and the digital control circuitry is initialized.

When $\overline{\text{RESET}}$ transitions high to start normal operation, the transmit CMU calibration is performed.

13. Transmit Differential Output Circuit

The Si5110 utilizes a current-mode logic (CML) architecture to drive the high-speed serial output clock and data on TXCLKOUT and TXDOUT. An example of output termination with ac coupling is shown in Figure 9. In applications where direct dc coupling is possible, the 0.1 μF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is listed in Table 2 on page 6.

14. Internal Pullups and Pulldowns

On-chip 30 kΩ resistors are used to individually set the LVTTL inputs if these inputs are left disconnected. The specific default state of each input is enumerated in 17. "Pin Descriptions: Si5110" on page 25.

15. Power Supply Filtering

The transmitter generated jitter is most sensitive to power supply noise below its PLL loop-bandwidth (BWSEL setting). The power supply noise of interest is bounded between the SONET/SDH generated jitter specification of 12 kHz (for 2.48832 Gbps) and the PLL loop-bandwidth. Integrated supply noise from 1/10th the SONET/SDH specification (1.2 kHz) to 10x the loop-bandwidth should be suppressed to a level appropriate for each design. Below the PLL loop-bandwidth, the typical generated jitter due to supply noise is approximately 2.5 mUIpp per 1 mVrms; this parameter can be used as a guideline for calculating the output jitter and supply filtering requirements. The receiver does not place additional power supply constraints beyond those listed for the transmitter.

Please contact Silicon Laboratories' applications engineering for recommendations on bypass capacitors and their placement.

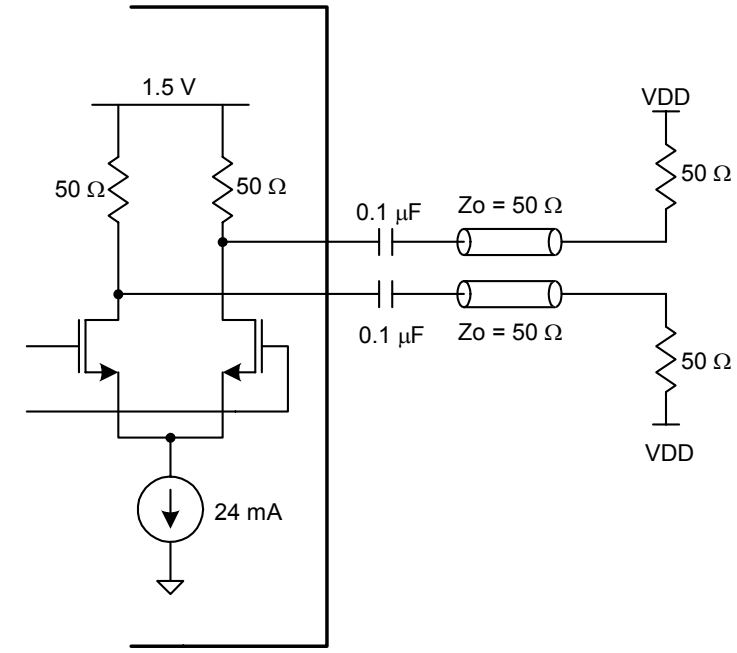


Figure 9. CML Output Driver Termination (TXCLKOUT, TXDOUT)

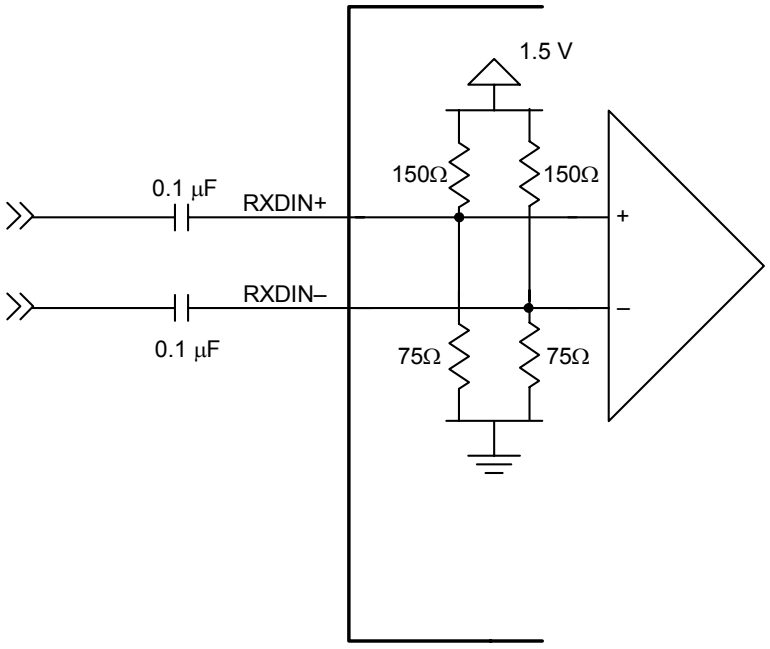


Figure 10. Receiver Differential Input Circuitry

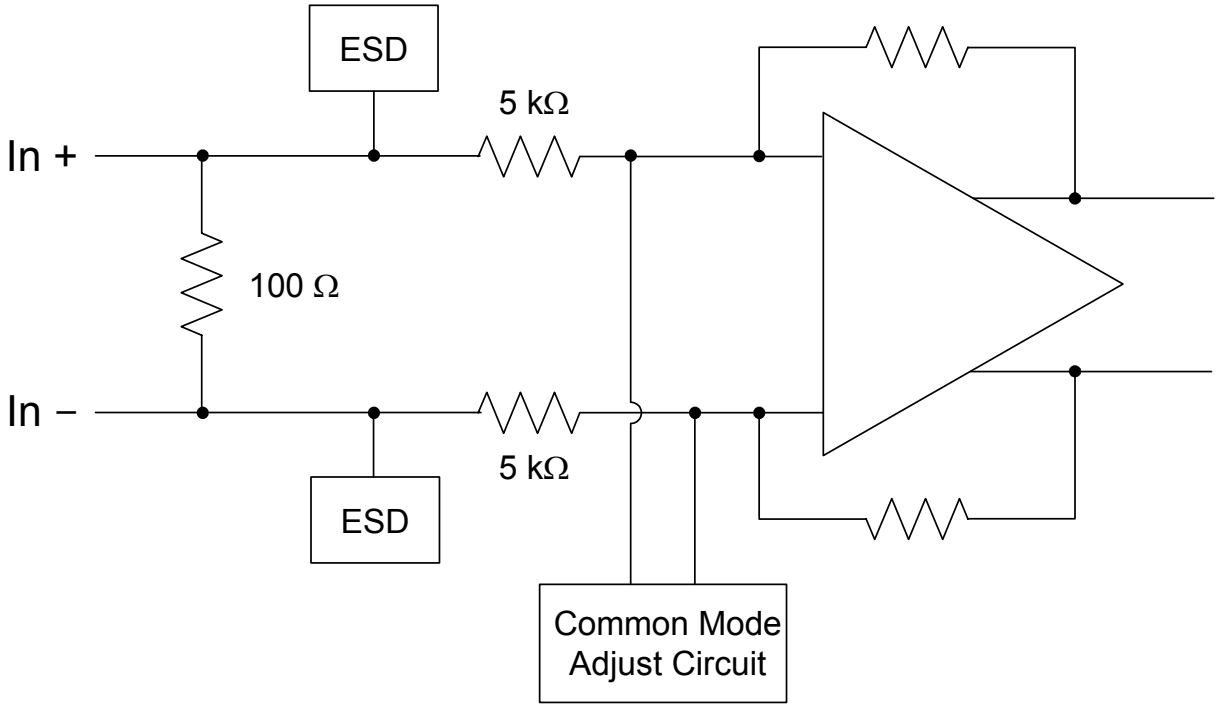


Figure 11. LVDS Differential Input Circuitry

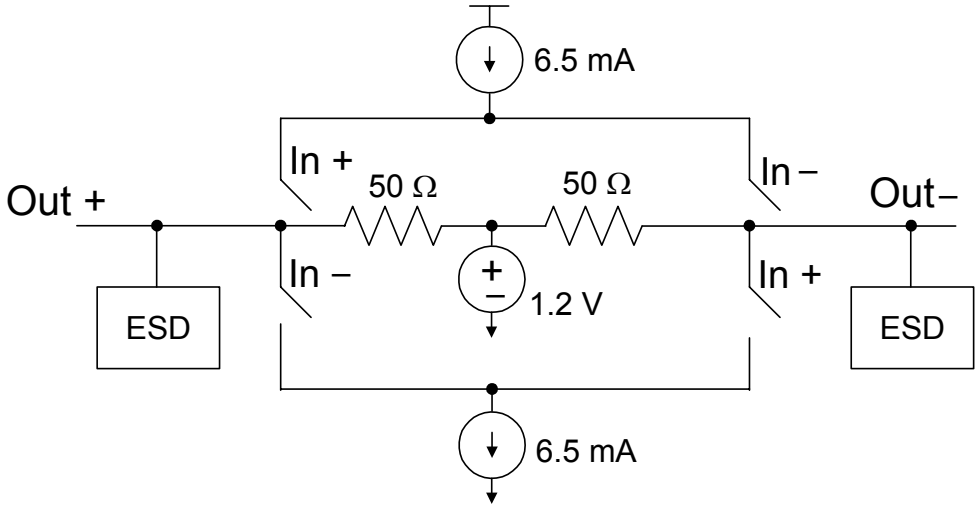


Figure 12. LVDS Driver Termination (RXDOUT, TXCLK4OUT)

16. Si5110 Pinout: 99 BGA

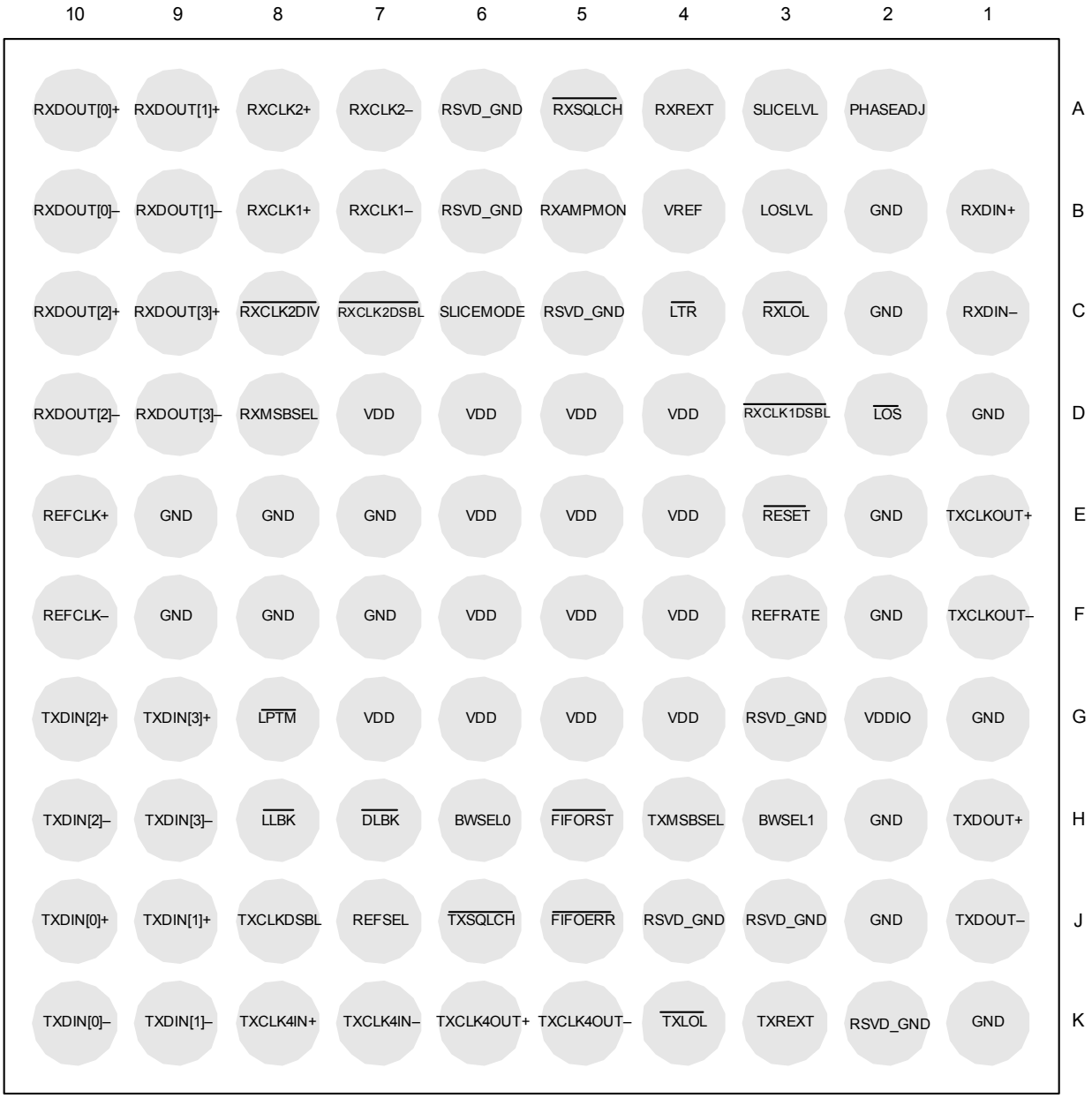


Figure 13. Si5110 Pin Configuration (Bottom View)

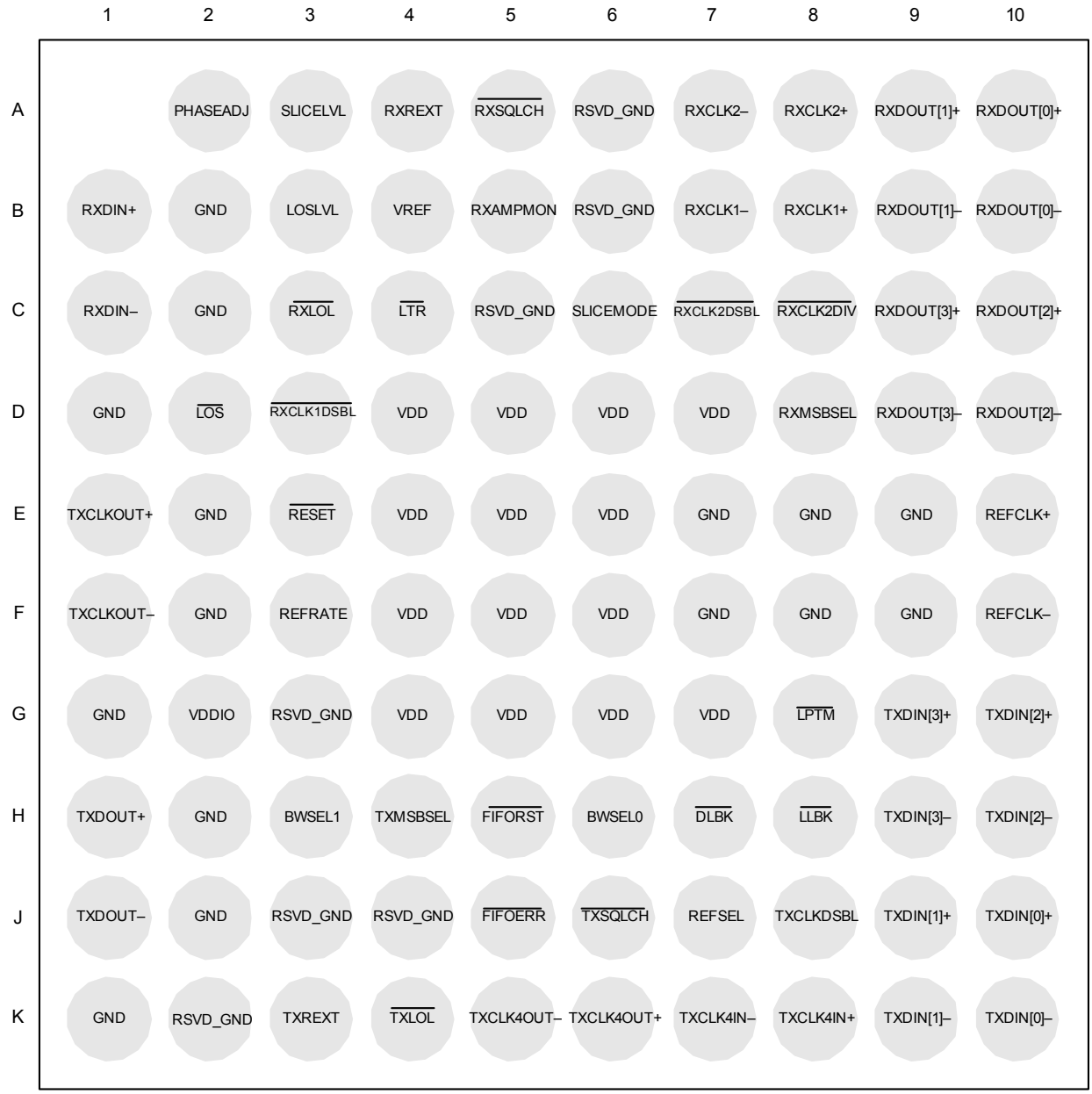


Figure 14. Si5110 Pin Configuration (Transparent Top View)

17. Pin Descriptions: Si5110

Pin Number(s)	Name	I/O	Signal Level	Description
H3 H6	BWSEL1 BWSEL0	I	LVTTL	**Transmit DSPLL Bandwidth Select.** The inputs select loop bandwidth of the Transmit Clock Multiplier DSPLL as listed in Table 6. **Note:** Both inputs have an internal pulldown.
H7	$\overline{\text{DLBK}}$	I	LVTTL	**Diagnostic Loopback.** When this input is low, the transmit clock and data are looped back for output on RXDOUT, RXCLK1 and RXCLK2. This pin should be held high for normal operation. **Note:** This input has an internal pullup.
J5	$\overline{\text{FIFOERR}}$	O	LVTTL	**FIFO Error.** This output is asserted (driven low) when a FIFO overflow/underflow has occurred. This output is low until reset by asserting FIFORST.
H5	$\overline{\text{FIFORST}}$	I	LVTTL	**FIFO RESET.** When this input is low, the read/write FIFO pointers are reset to their initial state. **Note:** This input has an internal pullup.
B2, C2, D1, E2, E7–9, F2, F7–9, G1, H2, J2, K1	GND	GND		**Supply Ground.** Connect to system GND. Ensure a very low impedance path for optimal performance.
H8	$\overline{\text{LLBK}}$	I	LVTTL	**Line Loopback.** When this input is low, the recovered clock and data are looped back for output on TXDOUT, and TXCLKOUT. Set this pin high for normal operation. **Note:** This input has an internal pullup.
D2	$\overline{\text{LOS}}$	O	LVTTL	**Loss-of-Signal.** This output is asserted (driven low) when the peak-to-peak signal amplitude on RXDIN is below the threshold set via LOSLVL.
B3	LOSLVL	I		**LOS Threshold Level.** Applying an analog voltage to this pin allows adjustment of the Threshold used to declare $\overline{\text{LOS}}$. Tieing this input to VREF disables $\overline{\text{LOS}}$ detection and forces the $\overline{\text{LOS}}$ output high.