



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



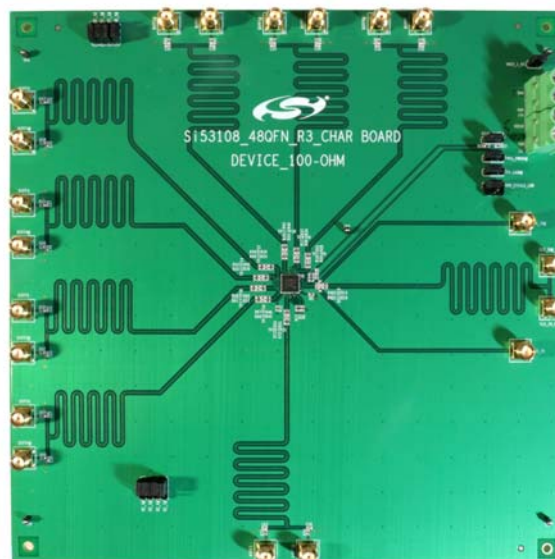
Si53108 EVALUATION BOARD USER'S GUIDE

Description

The Si53108-EVB can be used to evaluate the Si53108-A01AGM, an 8-output PCIe Gen1/2/3 buffer that can operate in either fanout or zero delay mode.

Features

- 10-inch traces to evaluate signal integrity
- The signal traces of the input and outputs have a single-ended impedance of 50 ohms, and differential impedance of 100 ohms.
- The series resistance on the outputs are set to match to this impedance design.
- DC pin controls per data sheet specification.
- Ability to measure input to output propagation delay.
- Ability to measure PCIe clock jitter.
- Ability to program features of Si53108-A01AGM via I²C interface.



Si53108-EVB

1. Schematics

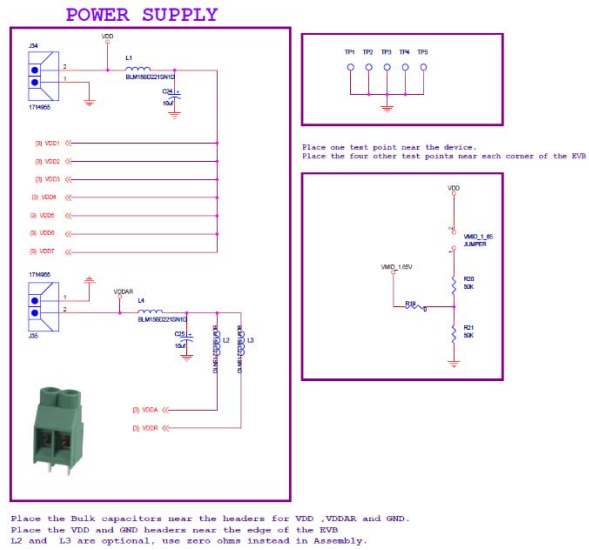
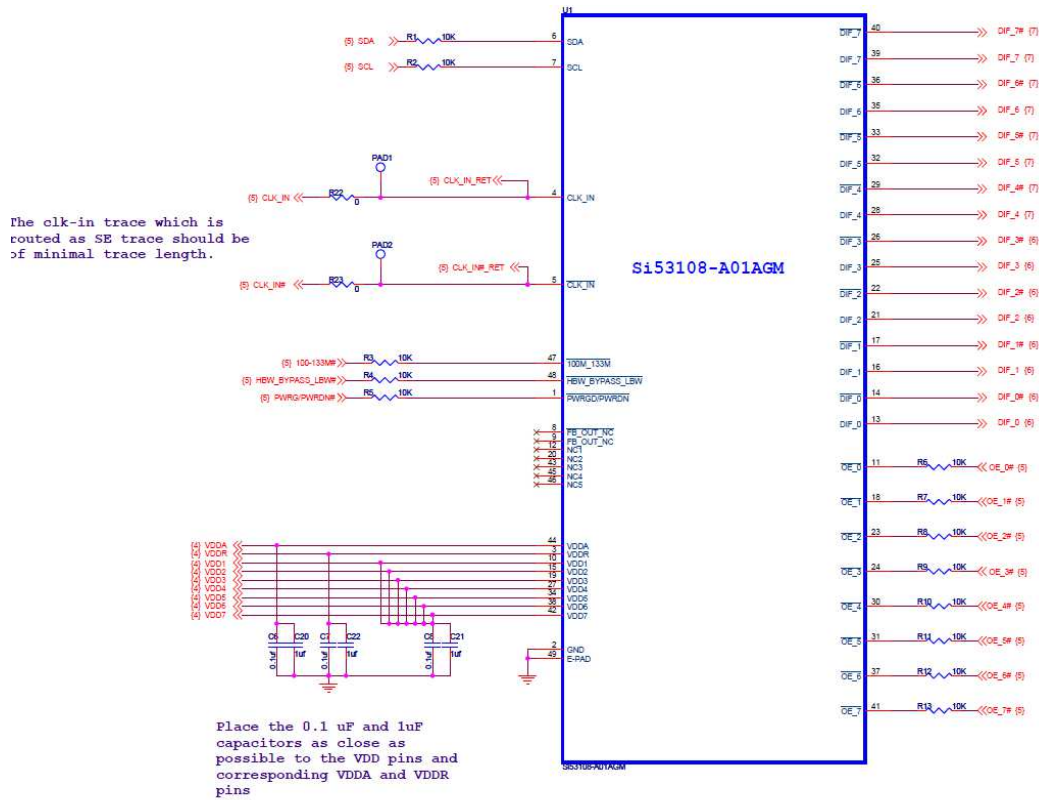


Figure 1. Schematic 1

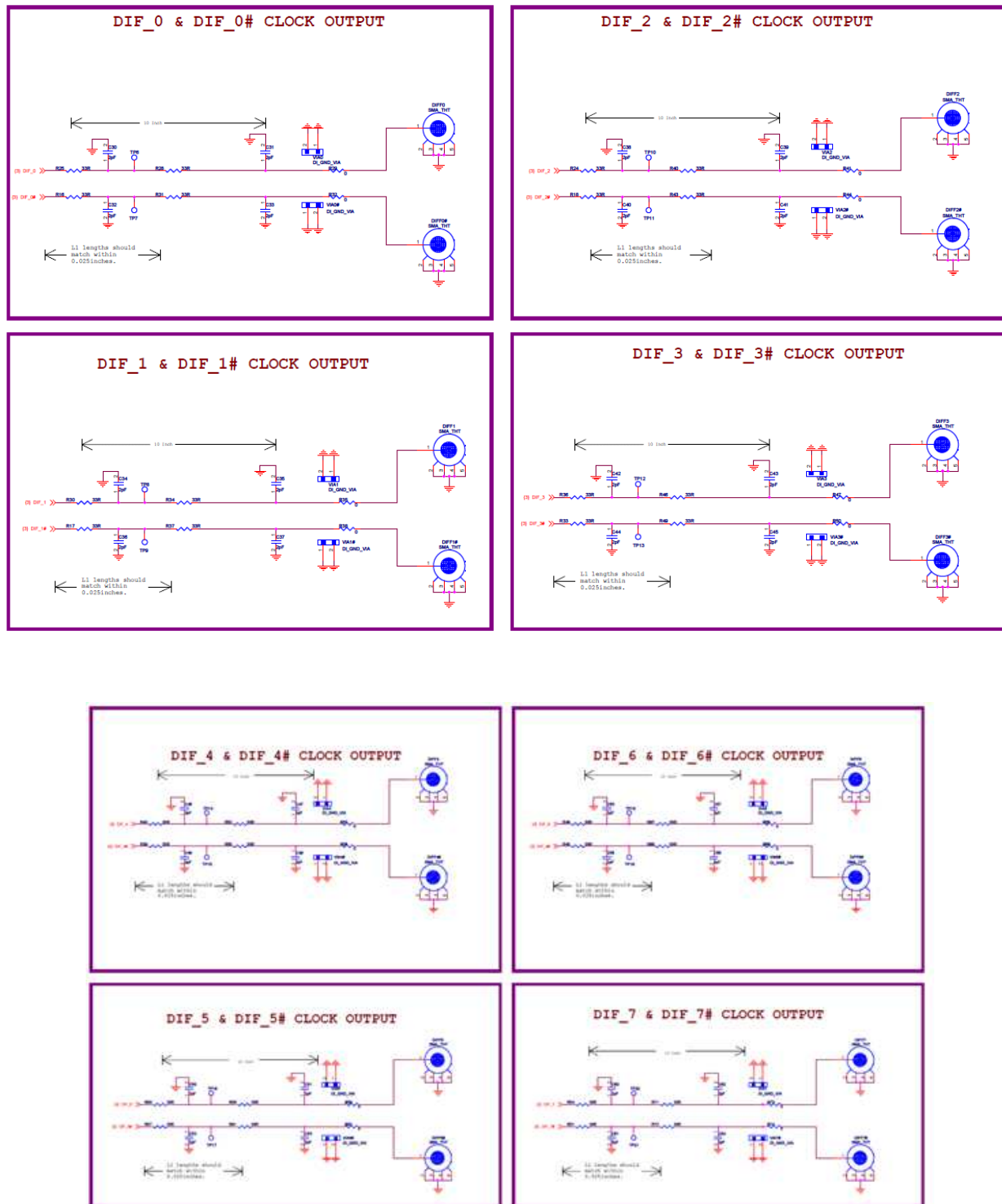


Figure 2. Schematic 2

2. Input and Power Supply Sequencing

The Si53108-A01AGM should be powered up with supply at both the VDD and VDD_IO nodes (at the jumpers available on the EVB). A 100MHz or 133MHz HCSL input clock should be applied to pins 8 and 9. There is no internal or on-board resistive termination, therefore HCSL termination needs to be provided at the input if needed by the driver. The input clock should be applied only after the supplies are stable.

3. Quick Start Guide:

1. Enable supply on the VDD pin.
2. Enable supply on the VDDIO pin.
3. Apply input clock on the SMA connectors CLK_IN/CLK_IN# and measure the return path clock on CLK_IN_RET, CLK_IN#_RET.

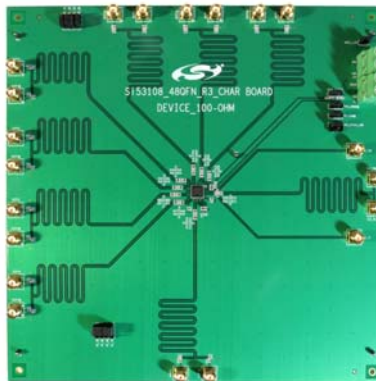


Figure 4. Clock Return Path

- a. The input clock measured at J32, J33 needs a 50-ohm termination on the scope.
 - b. The attenuation will be 1:10 after the above termination. Appropriate scaling (10x) needs to be set at the scope to adjust for the scaling.
4. The output clocks are now set up and can be measured on an oscilloscope or frequency domain measurement instrument.

4. Usage of the EVB

1. Once the EVB has been set up, the following can be evaluated:
2. Signal integrity of the device when driving 10-inch, 100-ohm differential traces.
3. Effect of capacitance load on output signal integrity.
4. Output-to-output skew over 10-inch traces.
5. Input-to-output propagation delay in BYPASS, HBW, and LBW modes using the input clock return path.
6. Measuring the power consumption of the device.
7. Modification of the device settings via the I²C interface.

5. Bill of Materials

| Item | Quantity | Reference | Part | PCB Footprint | Part Number | Description | Manufacturer | Comments |
|------|----------|------------------------|---------|---------------|-------------|---------------------------------|--------------|------------------------------------|
| 1 | 20 | DIFF_10_DIFF1_DIFF29 | SMA_TH1 | SMA_TH1 | LT12SAGF4GT | Vertical PCB Thru Hole SMA Jack | UGHTHORSE | Component Reference 305-PD-13-1158 |
| 2 | 20 | DIFF_2_DIFF1_DIFF3 | | | | | | |
| 3 | 20 | DIFF_3_DIFF1_DIFF4 | | | | | | |
| 4 | 20 | DIFF_4_DIFF1_DIFF5 | | | | | | |
| 5 | 20 | DIFF_5_DIFF1_DIFF6 | | | | | | |
| 6 | 20 | DIFF_6_DIFF1_DIFF7 | | | | | | |
| 7 | 20 | DIFF_7_DIFF1_DIFF8 | | | | | | |
| 8 | 20 | DIFF_8_DIFF1_DIFF9 | | | | | | |
| 9 | 20 | DIFF_9_DIFF1_DIFF10 | | | | | | |
| 10 | 20 | DIFF_10_DIFF1_DIFF11 | | | | | | |
| 11 | 20 | DIFF_11_DIFF1_DIFF12 | | | | | | |
| 12 | 20 | DIFF_12_DIFF1_DIFF13 | | | | | | |
| 13 | 20 | DIFF_13_DIFF1_DIFF14 | | | | | | |
| 14 | 20 | DIFF_14_DIFF1_DIFF15 | | | | | | |
| 15 | 20 | DIFF_15_DIFF1_DIFF16 | | | | | | |
| 16 | 20 | DIFF_16_DIFF1_DIFF17 | | | | | | |
| 17 | 20 | DIFF_17_DIFF1_DIFF18 | | | | | | |
| 18 | 20 | DIFF_18_DIFF1_DIFF19 | | | | | | |
| 19 | 20 | DIFF_19_DIFF1_DIFF20 | | | | | | |
| 20 | 20 | DIFF_20_DIFF1_DIFF21 | | | | | | |
| 21 | 20 | DIFF_21_DIFF1_DIFF22 | | | | | | |
| 22 | 20 | DIFF_22_DIFF1_DIFF23 | | | | | | |
| 23 | 20 | DIFF_23_DIFF1_DIFF24 | | | | | | |
| 24 | 20 | DIFF_24_DIFF1_DIFF25 | | | | | | |
| 25 | 20 | DIFF_25_DIFF1_DIFF26 | | | | | | |
| 26 | 20 | DIFF_26_DIFF1_DIFF27 | | | | | | |
| 27 | 20 | DIFF_27_DIFF1_DIFF28 | | | | | | |
| 28 | 20 | DIFF_28_DIFF1_DIFF29 | | | | | | |
| 29 | 20 | DIFF_29_DIFF1_DIFF30 | | | | | | |
| 30 | 20 | DIFF_30_DIFF1_DIFF31 | | | | | | |
| 31 | 20 | DIFF_31_DIFF1_DIFF32 | | | | | | |
| 32 | 20 | DIFF_32_DIFF1_DIFF33 | | | | | | |
| 33 | 20 | DIFF_33_DIFF1_DIFF34 | | | | | | |
| 34 | 20 | DIFF_34_DIFF1_DIFF35 | | | | | | |
| 35 | 20 | DIFF_35_DIFF1_DIFF36 | | | | | | |
| 36 | 20 | DIFF_36_DIFF1_DIFF37 | | | | | | |
| 37 | 20 | DIFF_37_DIFF1_DIFF38 | | | | | | |
| 38 | 20 | DIFF_38_DIFF1_DIFF39 | | | | | | |
| 39 | 20 | DIFF_39_DIFF1_DIFF40 | | | | | | |
| 40 | 20 | DIFF_40_DIFF1_DIFF41 | | | | | | |
| 41 | 20 | DIFF_41_DIFF1_DIFF42 | | | | | | |
| 42 | 20 | DIFF_42_DIFF1_DIFF43 | | | | | | |
| 43 | 20 | DIFF_43_DIFF1_DIFF44 | | | | | | |
| 44 | 20 | DIFF_44_DIFF1_DIFF45 | | | | | | |
| 45 | 20 | DIFF_45_DIFF1_DIFF46 | | | | | | |
| 46 | 20 | DIFF_46_DIFF1_DIFF47 | | | | | | |
| 47 | 20 | DIFF_47_DIFF1_DIFF48 | | | | | | |
| 48 | 20 | DIFF_48_DIFF1_DIFF49 | | | | | | |
| 49 | 20 | DIFF_49_DIFF1_DIFF50 | | | | | | |
| 50 | 20 | DIFF_50_DIFF1_DIFF51 | | | | | | |
| 51 | 20 | DIFF_51_DIFF1_DIFF52 | | | | | | |
| 52 | 20 | DIFF_52_DIFF1_DIFF53 | | | | | | |
| 53 | 20 | DIFF_53_DIFF1_DIFF54 | | | | | | |
| 54 | 20 | DIFF_54_DIFF1_DIFF55 | | | | | | |
| 55 | 20 | DIFF_55_DIFF1_DIFF56 | | | | | | |
| 56 | 20 | DIFF_56_DIFF1_DIFF57 | | | | | | |
| 57 | 20 | DIFF_57_DIFF1_DIFF58 | | | | | | |
| 58 | 20 | DIFF_58_DIFF1_DIFF59 | | | | | | |
| 59 | 20 | DIFF_59_DIFF1_DIFF60 | | | | | | |
| 60 | 20 | DIFF_60_DIFF1_DIFF61 | | | | | | |
| 61 | 20 | DIFF_61_DIFF1_DIFF62 | | | | | | |
| 62 | 20 | DIFF_62_DIFF1_DIFF63 | | | | | | |
| 63 | 20 | DIFF_63_DIFF1_DIFF64 | | | | | | |
| 64 | 20 | DIFF_64_DIFF1_DIFF65 | | | | | | |
| 65 | 20 | DIFF_65_DIFF1_DIFF66 | | | | | | |
| 66 | 20 | DIFF_66_DIFF1_DIFF67 | | | | | | |
| 67 | 20 | DIFF_67_DIFF1_DIFF68 | | | | | | |
| 68 | 20 | DIFF_68_DIFF1_DIFF69 | | | | | | |
| 69 | 20 | DIFF_69_DIFF1_DIFF70 | | | | | | |
| 70 | 20 | DIFF_70_DIFF1_DIFF71 | | | | | | |
| 71 | 20 | DIFF_71_DIFF1_DIFF72 | | | | | | |
| 72 | 20 | DIFF_72_DIFF1_DIFF73 | | | | | | |
| 73 | 20 | DIFF_73_DIFF1_DIFF74 | | | | | | |
| 74 | 20 | DIFF_74_DIFF1_DIFF75 | | | | | | |
| 75 | 20 | DIFF_75_DIFF1_DIFF76 | | | | | | |
| 76 | 20 | DIFF_76_DIFF1_DIFF77 | | | | | | |
| 77 | 20 | DIFF_77_DIFF1_DIFF78 | | | | | | |
| 78 | 20 | DIFF_78_DIFF1_DIFF79 | | | | | | |
| 79 | 20 | DIFF_79_DIFF1_DIFF80 | | | | | | |
| 80 | 20 | DIFF_80_DIFF1_DIFF81 | | | | | | |
| 81 | 20 | DIFF_81_DIFF1_DIFF82 | | | | | | |
| 82 | 20 | DIFF_82_DIFF1_DIFF83 | | | | | | |
| 83 | 20 | DIFF_83_DIFF1_DIFF84 | | | | | | |
| 84 | 20 | DIFF_84_DIFF1_DIFF85 | | | | | | |
| 85 | 20 | DIFF_85_DIFF1_DIFF86 | | | | | | |
| 86 | 20 | DIFF_86_DIFF1_DIFF87 | | | | | | |
| 87 | 20 | DIFF_87_DIFF1_DIFF88 | | | | | | |
| 88 | 20 | DIFF_88_DIFF1_DIFF89 | | | | | | |
| 89 | 20 | DIFF_89_DIFF1_DIFF90 | | | | | | |
| 90 | 20 | DIFF_90_DIFF1_DIFF91 | | | | | | |
| 91 | 20 | DIFF_91_DIFF1_DIFF92 | | | | | | |
| 92 | 20 | DIFF_92_DIFF1_DIFF93 | | | | | | |
| 93 | 20 | DIFF_93_DIFF1_DIFF94 | | | | | | |
| 94 | 20 | DIFF_94_DIFF1_DIFF95 | | | | | | |
| 95 | 20 | DIFF_95_DIFF1_DIFF96 | | | | | | |
| 96 | 20 | DIFF_96_DIFF1_DIFF97 | | | | | | |
| 97 | 20 | DIFF_97_DIFF1_DIFF98 | | | | | | |
| 98 | 20 | DIFF_98_DIFF1_DIFF99 | | | | | | |
| 99 | 20 | DIFF_99_DIFF1_DIFF100 | | | | | | |
| 100 | 20 | DIFF_100_DIFF1_DIFF101 | | | | | | |
| 101 | 20 | DIFF_101_DIFF1_DIFF102 | | | | | | |
| 102 | 20 | DIFF_102_DIFF1_DIFF103 | | | | | | |
| 103 | 20 | DIFF_103_DIFF1_DIFF104 | | | | | | |
| 104 | 20 | DIFF_104_DIFF1_DIFF105 | | | | | | |
| 105 | 20 | DIFF_105_DIFF1_DIFF106 | | | | | | |
| 106 | 20 | DIFF_106_DIFF1_DIFF107 | | | | | | |
| 107 | 20 | DIFF_107_DIFF1_DIFF108 | | | | | | |
| 108 | 20 | DIFF_108_DIFF1_DIFF109 | | | | | | |
| 109 | 20 | DIFF_109_DIFF1_DIFF110 | | | | | | |
| 110 | 20 | DIFF_110_DIFF1_DIFF111 | | | | | | |
| 111 | 20 | DIFF_111_DIFF1_DIFF112 | | | | | | |
| 112 | 20 | DIFF_112_DIFF1_DIFF113 | | | | | | |
| 113 | 20 | DIFF_113_DIFF1_DIFF114 | | | | | | |
| 114 | 20 | DIFF_114_DIFF1_DIFF115 | | | | | | |
| 115 | 20 | DIFF_115_DIFF1_DIFF116 | | | | | | |
| 116 | 20 | DIFF_116_DIFF1_DIFF117 | | | | | | |
| 117 | 20 | DIFF_117_DIFF1_DIFF118 | | | | | | |
| 118 | 20 | DIFF_118_DIFF1_DIFF119 | | | | | | |
| 119 | 20 | DIFF_119_DIFF1_DIFF120 | | | | | | |
| 120 | 20 | DIFF_120_DIFF1_DIFF121 | | | | | | |
| 121 | 20 | DIFF_121_DIFF1_DIFF122 | | | | | | |
| 122 | 20 | DIFF_122_DIFF1_DIFF123 | | | | | | |
| 123 | 20 | DIFF_123_DIFF1_DIFF124 | | | | | | |
| 124 | 20 | DIFF_124_DIFF1_DIFF125 | | | | | | |
| 125 | 20 | DIFF_125_DIFF1_DIFF126 | | | | | | |
| 126 | 20 | DIFF_126_DIFF1_DIFF127 | | | | | | |
| 127 | 20 | DIFF_127_DIFF1_DIFF128 | | | | | | |
| 128 | 20 | DIFF_128_DIFF1_DIFF129 | | | | | | |
| 129 | 20 | DIFF_129_DIFF1_DIFF130 | | | | | | |
| 130 | 20 | DIFF_130_DIFF1_DIFF131 | | | | | | |
| 131 | 20 | DIFF_131_DIFF1_DIFF132 | | | | | | |
| 132 | 20 | DIFF_132_DIFF1_DIFF133 | | | | | | |
| 133 | 20 | DIFF_133_DIFF1_DIFF134 | | | | | | |
| 134 | 20 | DIFF_134_DIFF1_DIFF135 | | | | | | |
| 135 | 20 | DIFF_135_DIFF1_DIFF136 | | | | | | |
| 136 | 20 | DIFF_136_DIFF1_DIFF137 | | | | | | |
| 137 | 20 | DIFF_137_DIFF1_DIFF138 | | | | | | |
| 138 | 20 | DIFF_138_DIFF1_DIFF139 | | | | | | |
| 139 | 20 | DIFF_139_DIFF1_DIFF140 | | | | | | |
| 140 | 20 | DIFF_140_DIFF1_DIFF141 | | | | | | |
| 141 | 20 | DIFF_141_DIFF1_DIFF142 | | | | | | |
| 142 | 20 | DIFF_142_DIFF1_DIFF143 | | | | | | |
| 143 | 20 | DIFF_143_DIFF1_DIFF144 | | | | | | |
| 144 | 20 | DIFF_144_DIFF1_DIFF145 | | | | | | |
| 145 | 20 | DIFF_145_DIFF1_DIFF146 | | | | | | |
| 146 | 20 | DIFF_146_DIFF1_DIFF147 | | | | | | |
| 147 | 20 | DIFF_147_DIFF1_DIFF148 | | | | | | |
| 148 | 20 | DIFF_148_DIFF1_DIFF149 | | | | | | |
| 149 | 20 | DIFF_149_DIFF1_DIFF150 | | | | | | |
| 150 | 20 | DIFF_150_DIFF1_DIFF151 | | | | | | |
| 151 | 20 | DIFF_151_DIFF1_DIFF152 | | | | | | |
| 152 | 20 | DIFF_152_DIFF1_DIFF153 | | | | | | |
| 153 | 20 | DIFF_153_DIFF1_DIFF154 | | | | | | |
| 154 | 20 | DIFF_154_DIFF1_DIFF155 | | | | | | |
| 155 | 20 | DIFF_155_DIFF1_DIFF156 | | | | | | |
| 156 | 20 | DIFF_156_DIFF1_DIFF157 | | | | | | |
| 157 | 20 | DIFF_157_DIFF1_DIFF158 | | | | | | |
| 158 | 20 | DIFF_158_DIFF1_DIFF159 | | | | | | |
| 159 | 20 | DIFF_159_DIFF1_DIFF160 | | | | | | |
| 160 | 20 | DIFF_160_DIFF1_DIFF161 | | | | | | |
| 161 | 20 | DIFF_161_DIFF1_DIFF162 | | | | | | |
| 162 | 20 | DIFF_162_DIFF1_DIFF163 | | | | | | |
| 163 | 20 | DIFF_163_DIFF1_DIFF164 | | | | | | |
| 164 | 20 | DIFF_164_DIFF1_DIFF165 | | | | | | |
| 165 | 20 | DIFF_165_DIFF1_DIFF166 | | | | | | |
| 166 | 20 | DIFF_166_DIFF1_DIFF167 | | | | | | |
| 167 | 20 | DIFF_167_DIFF1_DIFF168 | | | | | | |
| 168 | 20 | DIFF_168_DIFF1_DIFF169 | | | | | | |
| 169 | 20 | DIFF_169_DIFF1_DIFF170 | | | | | | |
| 170 | 20 | DIFF_170_DIFF1_DIFF171 | | | | | | |
| 171 | 20 | DIFF_171_DIFF1_DIFF172 | | | | | | |
| 172 | 20 | DIFF_172_DIFF1_DIFF173 | | | | | | |
| 173 | 20 | DIFF_173_DIFF1_DIFF174 | | | | | | |
| 174 | 20 | DIFF_174_DIFF1_DIFF175 | | | | | | |
| 175 | 20 | DIFF_175_DIFF1_DIFF176 | | | | | | |
| 176 | 20 | | | | | | | |



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro



Timing Portfolio
www.silabs.com/timing



SW/HW
www.silabs.com/CBPro



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOModem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>