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Si5324

Any-Frequency Precision Clock Multiplier/ Jitter Attenuator

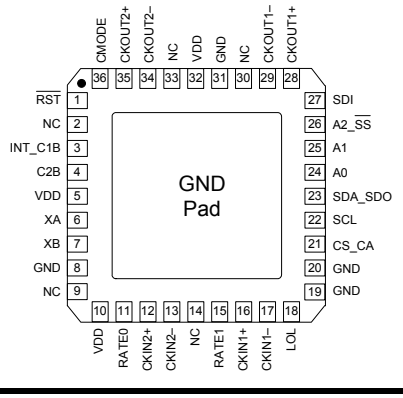
Features

- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs as low as 290 fs rms (12 kHz–20 MHz), 320 fs rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (4– 525 Hz)
- Meets ITU-T G.8251 and Telcordia GR-253-CORE jitter specification
- Hitless input clock switching with phase build-out
- Freerun, Digital Hold operation
- Configurable signal format per output (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236, 239/237, 66/64, 239/238, 15/14, 253/221, 255/238)
- LOL, LOS, FOS alarm outputs
- I^2C or SPI programmable
- On-chip voltage regulator with high PSNR
- Single supply 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS-compliant

Ordering Information:

See page 64.

Pin Assignments



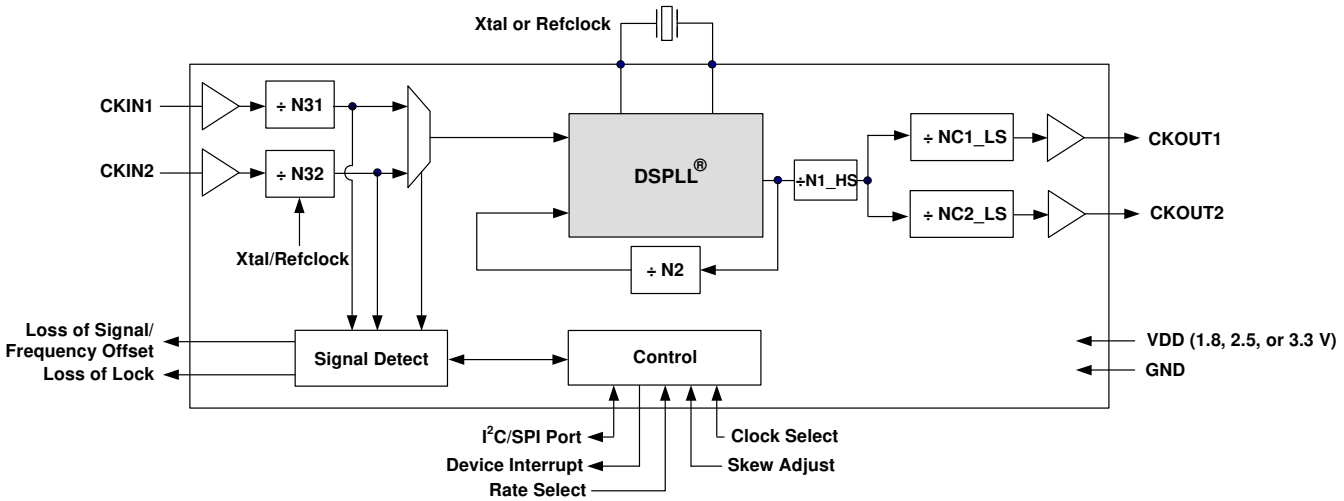
Applications

- Broadcast video –3G/HD/SD-SDI, Genlock
- Packet Optical Transport Systems (P-OTS), MSPP
- OTN/OTU-1/2/3/4 Asynchronous Demapping (Gapped Clock)
- SONET OC-48/192/768, SDH/STM-16/64/256 line cards
- 1/2/4/8/10G Fibre Channel line cards
- GbE/10/40/100G Synchronous Ethernet (LAN/WAN)
- Data converter clocking
- Wireless base stations
- Test and measurement

Description

The Si5324 is a low-bandwidth, jitter-attenuating, precision clock multiplier for applications requiring sub 1 ps jitter performance with loop bandwidths between 4 Hz and 525 Hz. The Si5324 accepts two input clocks ranging from 2 kHz to 710 MHz and generates two output clocks ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The two outputs are divided down separately from a common source. The Si5324 can also use its external reference as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. The Si5324 input clock frequency and clock multiplication ratio are programmable via an I^2C or SPI interface. The Si5324 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. The Si5324 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Supply Voltage during Normal Operation	V_{DD}	3.3 V Nominal	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.						

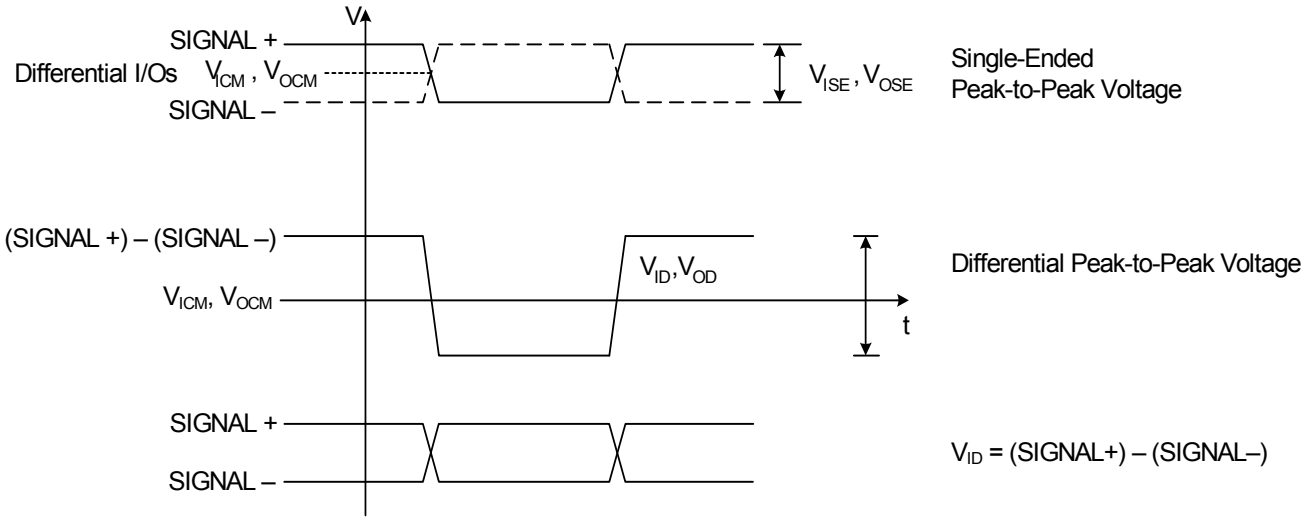


Figure 1. Differential Voltage Characteristics

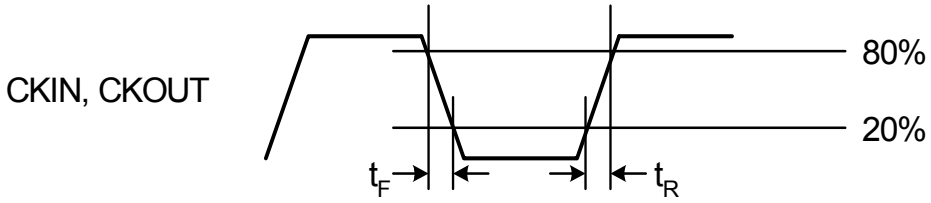


Figure 2. Rise/Fall Time Characteristics

Table 2. DC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1]	I_{DD}	LVPECL Format 622.08 MHz Out Both CKOUTs Enabled	—	251	279	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	217	243	mA
		CMOS Format 19.44 MHz Out Both CKOUTs Enabled	—	204	234	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	194	220	mA
		Disable Mode	—	165	—	mA
CKINn Input Pins[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
		3.3 V ± 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		fCKIN > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clocks (CKOUTn)[3,5]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD}-0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	ICMOS[1:0] = 11 V_{DD} = 1.8 V	—	7.5	—	mA
		ICMOS[1:0] = 10 V_{DD} = 1.8 V	—	5.5	—	mA
		ICMOS[1:0] = 01 V_{DD} = 1.8 V	—	3.5	—	mA
		ICMOS[1:0] = 00 V_{DD} = 1.8 V	—	1.75	—	mA
		ICMOS[1:0] = 11 V_{DD} = 3.3 V	—	32	—	mA
		ICMOS[1:0] = 10 V_{DD} = 3.3 V	—	24	—	mA
		ICMOS[1:0] = 01 V_{DD} = 3.3 V	—	16	—	mA
		ICMOS[1:0] = 00 V_{DD} = 3.3 V	—	8	—	mA
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3-Level Input Pins[4]						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}	See Note 4	–20	—	—	µA
Input Mid Current	I_{IMM}	See Note 4	–2	—	+2	µA
Input High Current	I_{IHH}	See Note 4	—	—	20	µA
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.97 V	V_{DD} – 0.4	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 3. AC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin XA (XB with cap to GND)						
Input Resistance	XA_{RIN}	RATE[1:0] = LM, ML, MH, or HM, ac coupled	—	12	—	kΩ
Input Voltage Swing	XA_{VPP}	RATE[1:0] = LM, ML, MH, or HM, ac coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Voltage Swing	XA/XB_{VPP}	RATE[1:0] = LM, ML, MH, or HM	0.5	—	2.4	V_{PP}
CKINn Input Pins						
Input Frequency	CKN_F		0.002	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins (See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F	N1 ≥ 6	0.002	—	945	MHz
		N1 = 5	970	—	1134	MHz
		N1 = 4	1.213	—	1.4	GHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz

Notes:

1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan, the XAXB reference frequency, and LOCKT setting (see application note, “AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs”. Visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.
3. LOCKT = 3.3 ms

Table 3. AC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.97 C_{LOAD} = 5 pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	+/-40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1			µs
Reset to Microprocessor Access Ready	t_{READY}				10	ms
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1	—	—	4.5 x N3	T_{CKIN}
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference	—	10	—	ms

Notes:
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan, the XAXB reference frequency, and LOCKT setting (see application note, “AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs”. Visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.
3. LOCKT = 3.3 ms

Table 3. AC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Device Skew						
Output Clock Skew	t_{SKEW}	↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format PHASEOFFSET = 0 CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1	—	—	100	ps
Phase Change due to Temperature Variation[1]	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps
PLL Performance **(fin = fout = 622.08 MHz; BW = 7 Hz; LVPECL, XAXB = 114.285 MHz)**						
Lock Time[2] Si5324E-C-GM[3]	t_{LOCKMP}	Start of ICAL to ↓ of LOL	—	1	1.5	s
Si5324A/B/C/D-C-GM			—	0.8	1.0	
Settle Time[2] Si5324E-C-GM	t_{SETTLE}	Start of ICAL to Fout within 5 ppm of final value	—	1.2	1.5	s
Si5324A/B/C/D-C-GM			—	4.2	5.0	
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk

Notes:
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan, the XAXB reference frequency, and LOCKT setting (see application note, “AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs”. Visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.
3. LOCKT = 3.3 ms

Table 3. AC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Noise fout = 622.08 MHz	CKO_{PN}	100 Hz Offset	—	–90	—	dBc/Hz
		1 kHz Offset	—	–106	—	dBc/Hz
		10 kHz Offset	—	–121	—	dBc/Hz
		100 kHz Offset	—	–132	—	dBc/Hz
		1 MHz Offset	—	–132	—	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	–88	–76	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–93	–70	dBc

Notes:
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan, the XAXB reference frequency, and LOCKT setting (see application note, “AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs”. Visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.
3. LOCKT = 3.3 ms

Table 4. Microprocessor Control
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I^2C Bus Lines (SDA, SCL)						
Input Voltage Low	VIL_{I2C}		—	—	0.25 x V_{DD}	V
Input Voltage High	VIH_{I2C}		0.7 x V_{DD}	—	V_{DD}	V
Hysteresis of Schmitt trigger inputs	$VHYS_{I2C}$	V_{DD} = 1.8V	0.1 x V_{DD}	—	—	V
		V_{DD} = 2.5 or 3.3 V	0.05 x V_{DD}	—	—	V
Output Voltage Low	VOL_{I2C}	V_{DD} = 1.8 V IO = 3 mA	—	—	0.2 x V_{DD}	V
		V_{DD} = 2.5 or 3.3 V IO = 3 mA	—	—	0.4	V

Table 4. Microprocessor Control (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SPI Specifications						
Duty Cycle, SCLK	t_{DC}	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	t_c		100	—	—	ns
Rise Time, SCLK	t_r	20–80%	—	—	25	ns
Fall Time, SCLK	t_f	20–80%	—	—	25	ns
Low Time, SCLK	t_{lsc}	20–20%	30	—	—	ns
High Time, SCLK	t_{hsc}	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	t_{d3}		—	—	25	ns
Setup Time, SS to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SS to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Slave Selects	t_{cs}		25	—	—	ns

Table 5. Jitter Generation

Parameter	Symbol	Test Condition*		Min	Typ	Max	GR-253-Specification	Unit
		Measurement Filter	DSPLL BW[2]					
Jitter Gen OC-192	JGEN	0.02–80 MHz	120 Hz	—	4.2	6.2	30	ps_{PP}
				—	.27	.42	N/A	ps_{rms}
		4–80 MHz	120 Hz	—	3.7	6.4	10	ps_{PP}
				—	.14	0.31	N/A	ps_{rms}
		0.05–80 MHz	120 Hz	—	4.4	6.9	10	ps_{PP}
				—	.26	0.41	1.0	ps rms
Jitter Gen OC-48	JGEN	0.12–20 MHz	120 Hz	—	3.5	5.4	40.2	ps_{PP}
				—	.27	0.41	4.02	ps rms

***Note:** Test conditions:

1. fIN = fOUT = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 120 Hz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. V_{DD} = 2.5 V
7. T_A = 85 °C

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

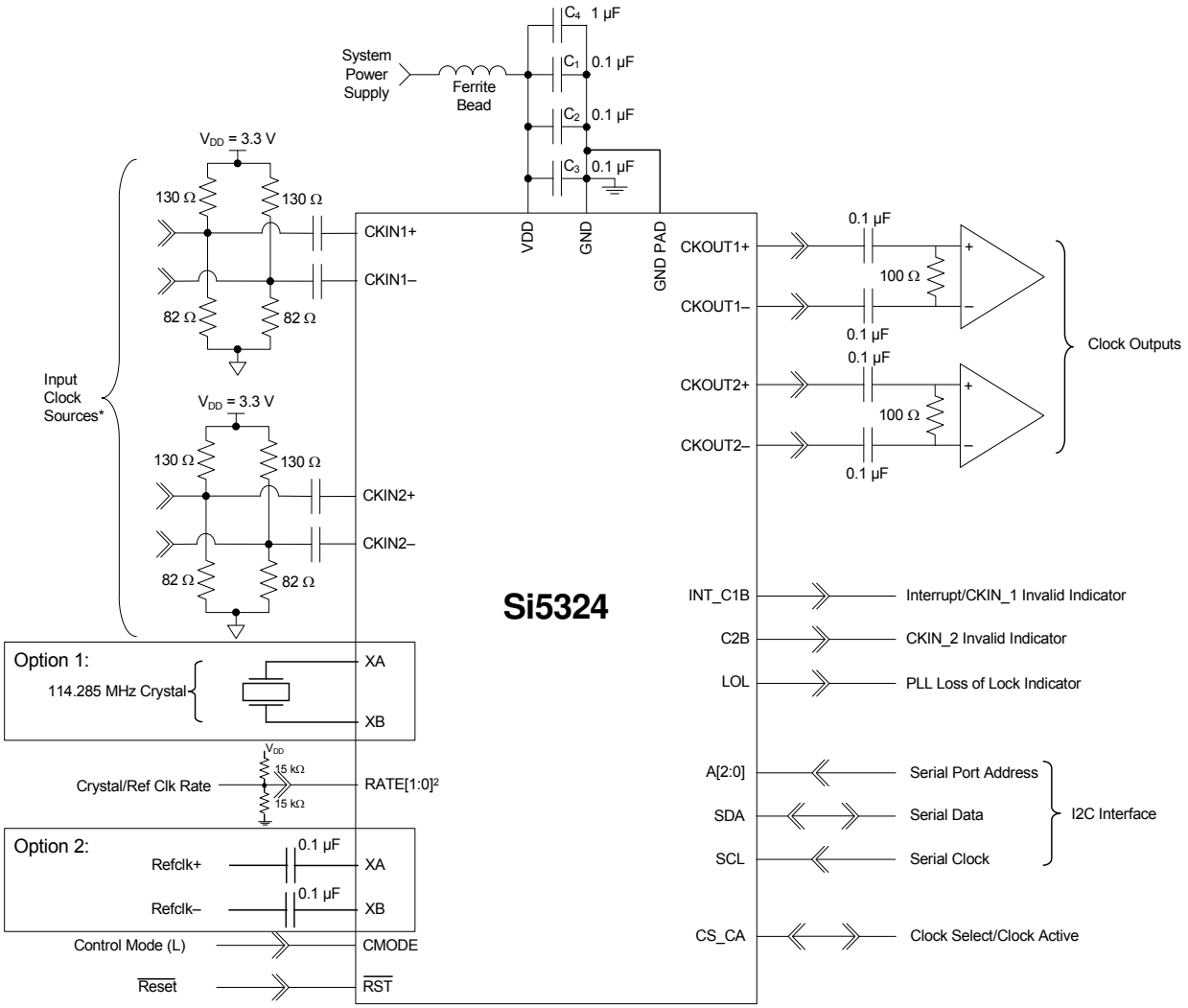
Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	32	C°/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	14	C°/W

Table 7. Absolute Maximum Ratings*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		–0.5	—	3.8	V
LVCMOS Input Voltage	V_{DIG}		–0.3		V_{DD}+0.3	V
CKINn Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Operating Junction Temperature	T_{JCT}		–55	—	150	ºC
Storage Temperature Range	T_{STG}		–55	—	150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–			750	—	—	V
ESD MM Tolerance; CKIN+/CKIN–			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			

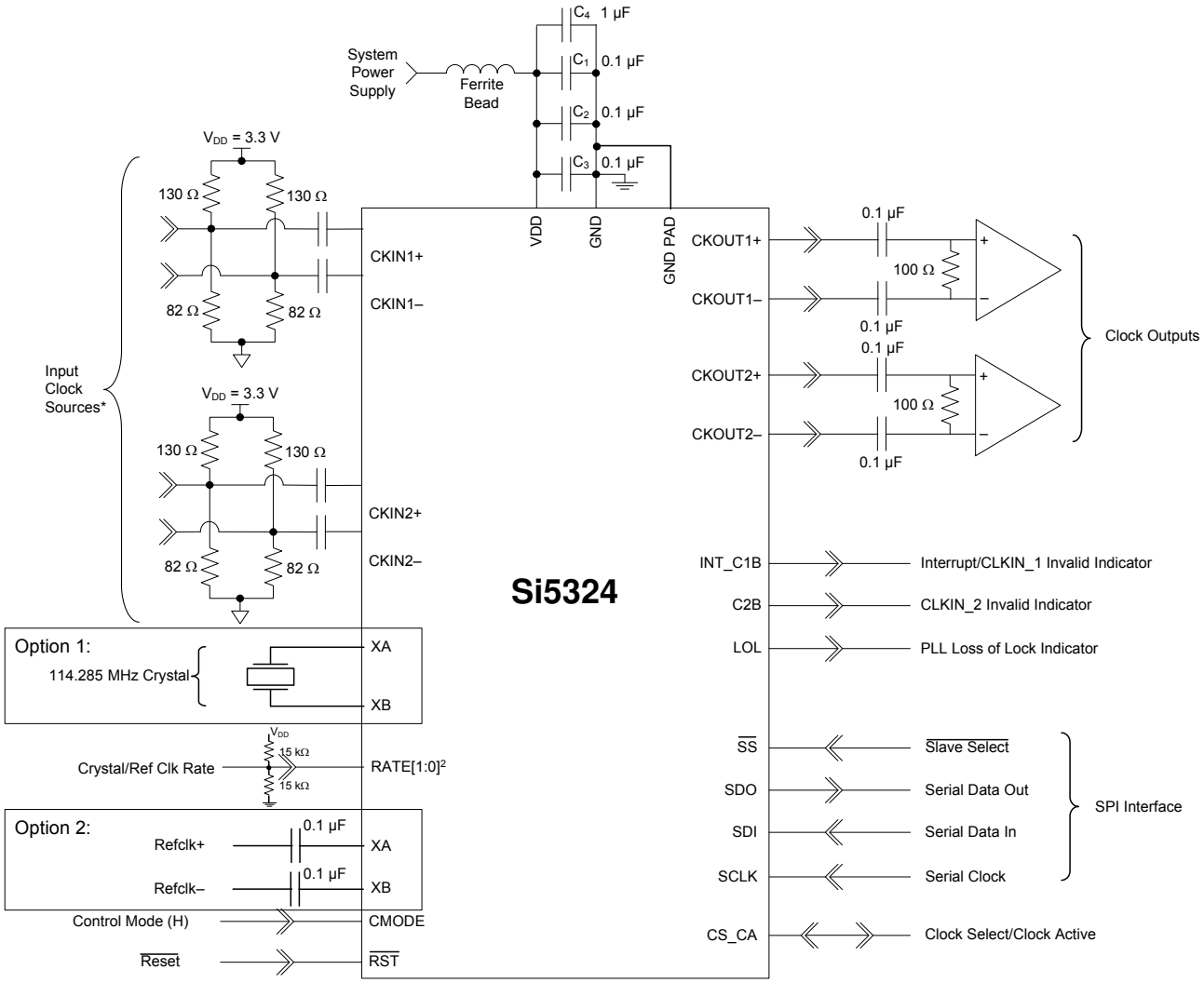
***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2. Typical Application Circuits



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).

Figure 3. Si5324 Typical Application Circuit (I^2C Control Mode)



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).

Figure 4. Si5324 Typical Application Circuit (SPI Control Mode)

3. Functional Description

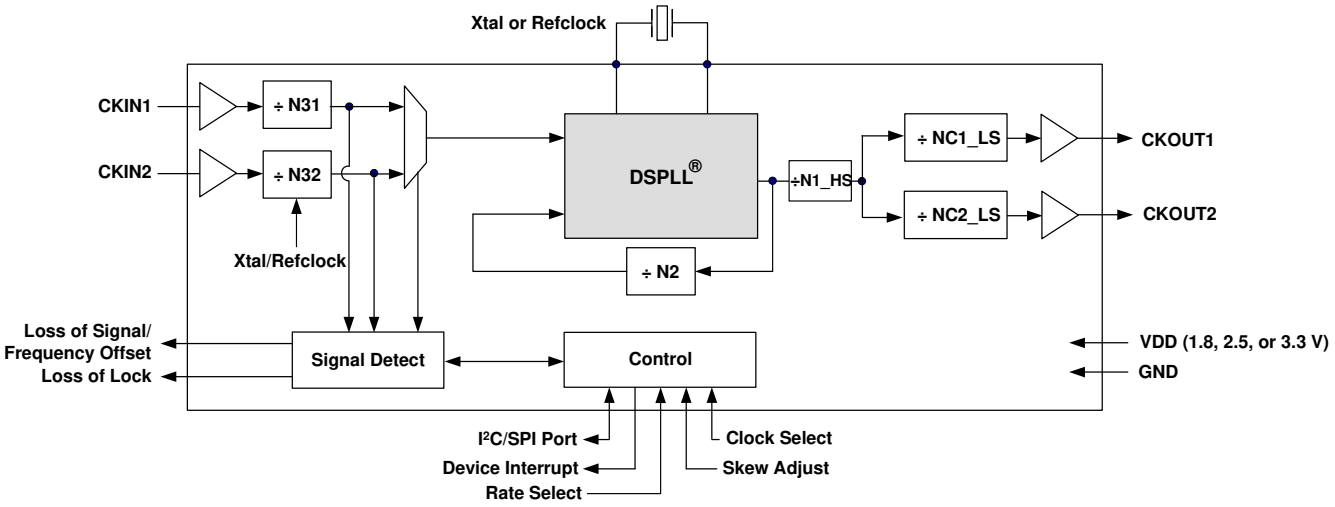


Figure 5. Si5324 Functional Block Diagram

The Si5324 is a low loop bandwidth, jitter-attenuating clock multiplier for high performance applications. The Si5324 accepts two input clocks ranging from 2 kHz to 710 MHz and generates two output clocks ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The Si5324 can also use its external reference as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for each input clock and output clock, so the Si5324 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5324 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing.

The Si5324 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5324 PLL loop bandwidth is digitally programmable and supports a range from 4 Hz to 525 Hz. A fast lock feature is available to reduce lock times inherent with low loop bandwidth PLLs. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5324 supports hitless switching between the two synchronous input clocks in compliance with Telcordia GR-253-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (maximum 200 ps phase change). Manual and automatic revertive and non-revertive input clock switching options are available. The Si5324 monitors both input clocks for loss-of-signal (LOS) and provides a LOS alarm when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. Due to the low loop bandwidth of the part, the LOL indicator clears before the loop fully settles (see "AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs" for additional details).

The Si5324 also monitors frequency offset alarms (FOS), which indicate if an input clock is within a specified frequency ppm accuracy relative to the frequency of an XA/XB reference clock. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported.

The Si5324 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average frequency that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5324 has two differential clock outputs. The signal format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. When configured for CMOS, four clock outputs are available. If not required, the second clock output can be powered down to minimize power consumption. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. The DSPLL*sim* software utility determines the phase offset resolution for a given combination of input clock and multiplication ratio. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply with best-in-class PSNR.

3.1. External Reference

An external, high quality 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal or external reference is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Specific recommendations can be found in the Family Reference Manual.

In digital hold, the DSPLL remains locked and tracks the external reference. Note that crystals can have temperature sensitivities.

Due to the low bandwidth capabilities of this part, any low-frequency wander or instability on the external reference will transfer to the output clocks. To address this issue, a stable external reference, TXCO, OCXO, or thermally-isolated crystal is recommended.

For example, with a 20 ppm oscillator as the reference on the XA/XB pins, temperature changes cause the oscillator to change frequency slightly. Although the Si5324 is locked to its input on CLKIN, it also uses the XA/XB as a reference.

If there is a need to use a reference oscillator instead of a crystal, Silicon Labs does not recommend using MEMS based oscillators. Instead, Silicon Labs recommends the Si530EB121M109DG, which is a very low-jitter/wander, LVPECL, 2.5 V crystal oscillator. The very low loop BW of the Si5324 means that it can be susceptible to XAXB reference sources that have high wander. Experience has shown that in spite of having low jitter, some MEMs oscillators have high wander, and these devices should be avoided. Contact Silicon Labs for details.

3.2. Additional Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5324. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories offers a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing (see “AN803: Lock and Settling Time Considerations for Si5324/27/69/74 Any-Frequency Jitter Attenuating Clock ICs” for additional details).

3.3. Typical Phase Noise Performance

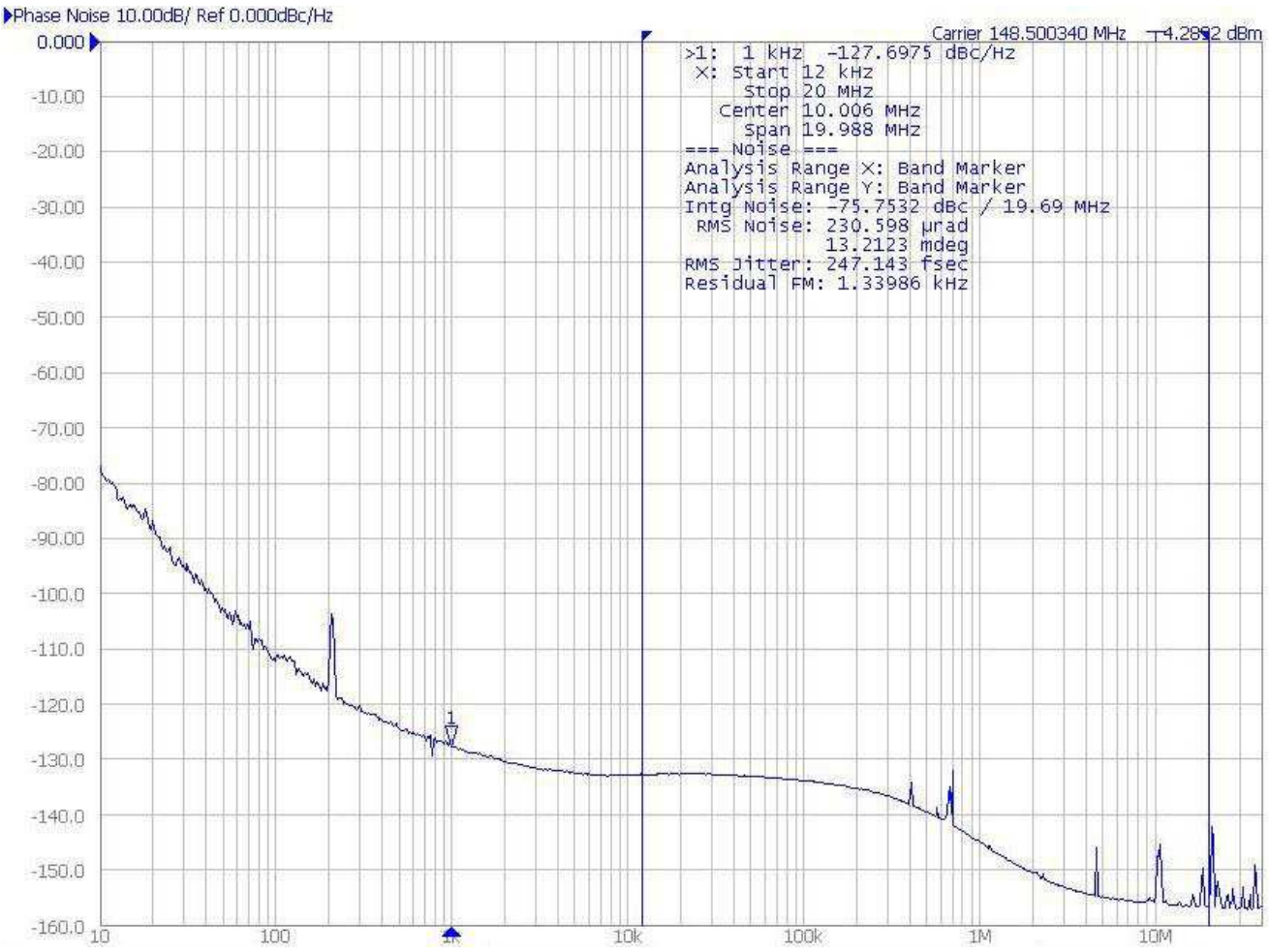


Figure 6. Broadcast Video

Table 8. Broadcast Video Jitter[1]

Jitter Bandwidth[2]	Jitter (Peak-Peak)	Jitter (RMS)
10 Hz to 20 MHz	5.24 ps	484 fs

Notes:
1. Number of samples: 8.91E9.
2. Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.

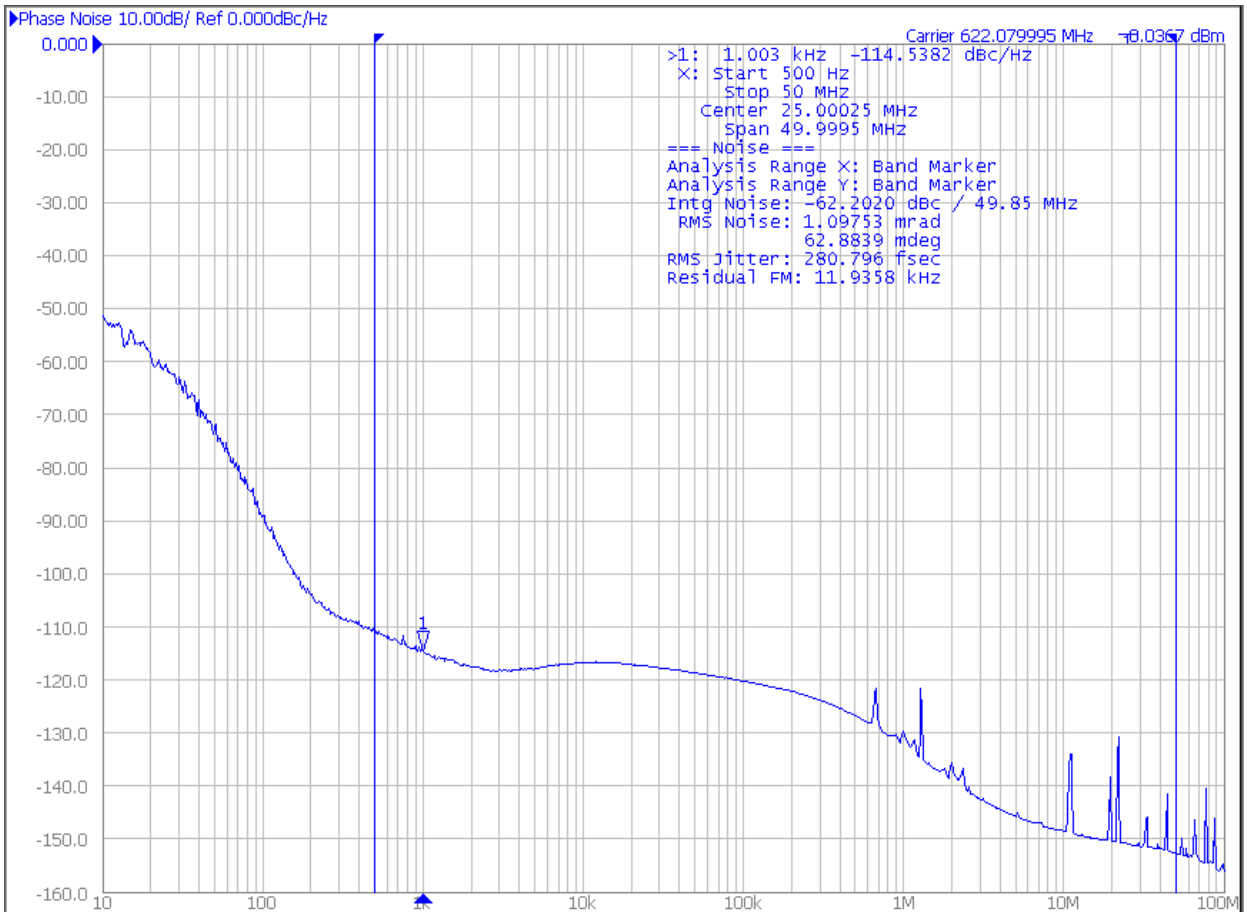


Figure 7. OTN/SONET/SDH Phase Noise

Note: Phase noise plot uses brick wall integration.

Table 9. SONET Jitter

Jitter Bandwidth*	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	266 fs
SONET_OC192_A, 20 kHz to 80 MHz	283 fs
SONET_OC192_B, 4 MHz to 80 MHz	155 fs
SONET_OC192_C, 50 kHz to 80 MHz	275 fs
Brick Wall_800 Hz to 80 MHz	287 fs
***Note:** Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.	

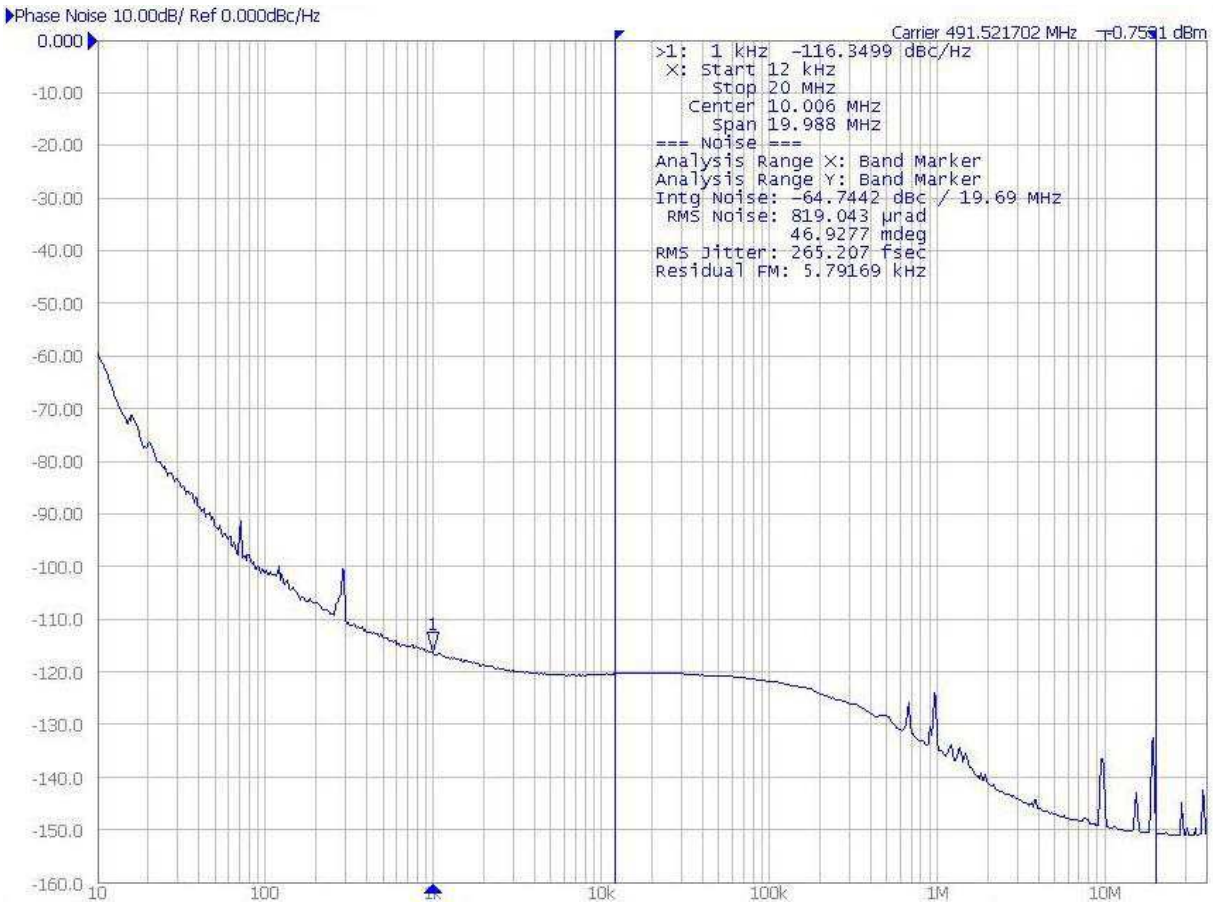


Figure 8. Wireless Base Station Phase Noise

Table 10. Wireless Base Station Jitter*

Jitter Bandwidth	Jitter (peak-peak)	Jitter (RMS)
10 Hz to 20 MHz	7.28 ps	581 fs
Note: Number of samples: 8.91E9		

4. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, e.g. Register 64, should never be written to.

Register	D7	D6	D5	D4	D3	D2	D1	D0
0		FREE_RUN	CKOUT_ ALWAYS_ON				BYPASS_REG	
1					CK_PRIOR2[1:0]		CK_PRIOR1[1:0]	
2	BWSEL_REG[3:0]							
3	CKSEL_REG[1:0]		DHOLD	SQ_ICAL				
4	AUTOSEL_REG[1:0]			HST_DEL[4:0]				
5	ICMOS[1:0]							
6			SFOUT2_REG[2:0}			SFOUT1_REG[2:0]		
7						FOSREFSEL[2:0]		
8	HLOG_2[1:0]		HLOG_1[1:0]					
9	HIST_AVG[4:0]							
10					DSBL2_ REG	DSBL1_ REG		
11							PD_CK2	PD_CK1
19	FOS_EN	FOS_THR[1:0]		VALTIME[1:0]		LOCK[T2:0]		
20					CK2_BAD_PIN	CK1_ BAD_ PIN	LOL_PIN	INT_PIN
21							CK1_ACTV_PIN	CKSEL_PIN
22					CK_ACTV_ POL	CK_BAD_ POL	LOL_POL	INT_POL
23						LOS2_MSK	LOS1_MSK	LOSX_MSK
24						FOS2_MSK	FOS1_MSK	LOL_MSK
25	N1_HS[2:0]							
31					NC1_LS[19:16]			
32	NC1_LS[15:8]							
33	NC1_LS[7:0]							
34					NC2_LS[19:16]			
35	NC2_LS[15:8]							
36	NC2_LS[7:0]							
40	N2_HS[2:0]				N2_LS[19:16]			
41	N2_LS[15:8]							
42	N2_LS[7:0]							
43						N31[18:16]		
44	N31[15:8]							
45	N31[7:0]							
46						N32[18:16]		

Register	D7	D6	D5	D4	D3	D2	D1	D0
47	N32[15:8]							
48	N32[7:0]							
55			CLKIN2RATE[2:0]			CLKIN1RATE[2:0]		
128							CK2_ACTV_REG	CK1_ACTV_REG
129						LOS2_INT	LOS1_INT	LOSX_INT
130		DIGHOLD-VALID				FOS2_INT	FOS1_INT	LOL_INT
131						LOS2_FLG	LOS1_FLG	LOSX_FLG
132					FOS2_FLG	FOS1_FLG	LOL_FLG	
134	PARTNUM_RO[11:4]							
135	PARTNUM_RO[3:0]				REVID_RO[3:0]			
136	RST_REG	ICAL						
137								FASTLOCK
138							LOS2_EN [1:1]	LOS1_EN [1:1]
139			LOS2_EN[0:0]	LOS1_EN[0:0]			FOS2_EN	FOS1_EN
142	INDEPENDENTSKEW1[7:0]							
143	INDEPENDENTSKEW2[7:0]							

Table 11. CKOUT_ALWAYS_ON and SQ_ICAL Truth Table

CKOUT_ALWAYS_ON	SQ_ICAL	Results
0	0	CKOUT OFF until after the first ICAL
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)
1	0	CKOUT always ON, including during an ICAL
1	1	CKOUT always ON, including during an ICAL. Use these settings to preserve output-to-output skew