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ANY-FREQUENCY PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Features

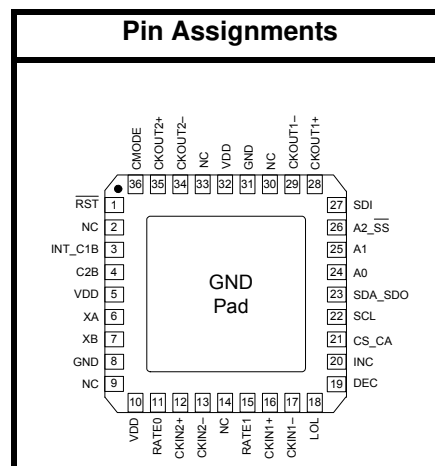
- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Dual clock inputs with manual or automatically controlled hitless switching (LVPECL, LVDS, CML, CMOS)
- Dual clock outputs with selectable signal format
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236)
- LOL, LOS, FOS alarm outputs
- Digitally-controlled output phase adjustment
- I²C or SPI programmable
- On-chip voltage regulator for 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

Applications

- SONET/SDH OC-48/OC-192/STM-16/STM-64 line cards
- ITU G.709 and custom FEC line cards
- GbE/10GbE, 1/2/4/8/10G Fibre Channel line cards
- GbE/10GbE Synchronous Ethernet
- Optical modules
- Wireless basestations
- Data converter clocking
- xDSL
- PDH clock synthesis
- Test and measurement
- Broadcast video

Description

The Si5326 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5326 accepts two input clocks ranging from 2 kHz to 710 MHz and generates two output clocks ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The two outputs are divided down separately from a common source. The Si5326 can also use its crystal oscillator as a clock source for frequency synthesis. The Si5326 input clock frequency and clock multiplication ratio are programmable through an I²C or SPI interface. The Si5326 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5326 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.



Si5326

Functional Block Diagram

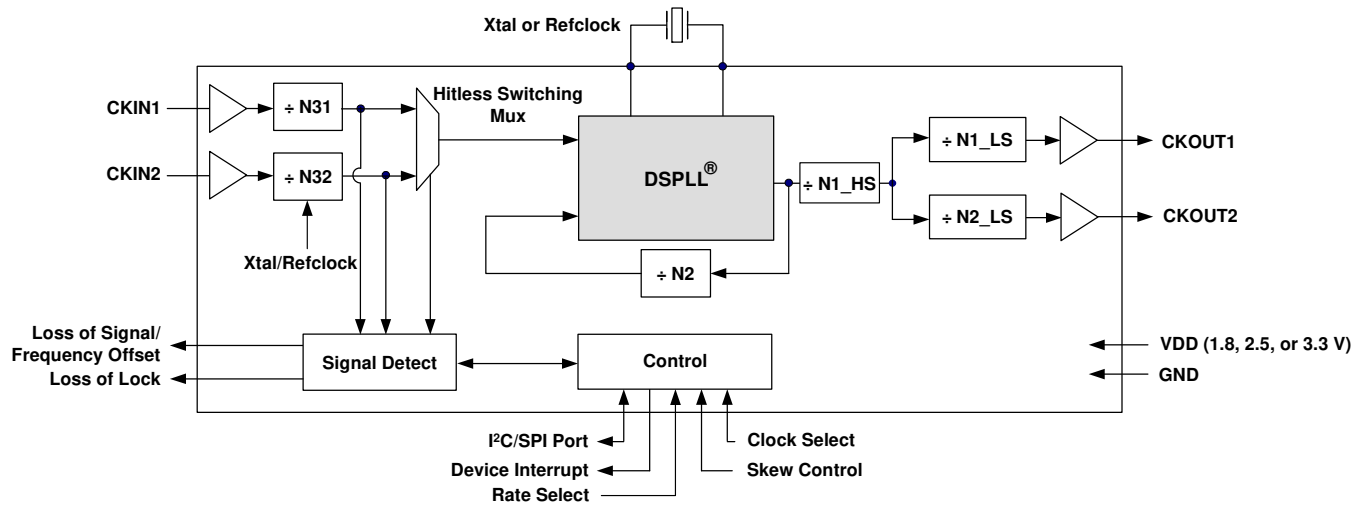


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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		-40	25	85	C
Supply Voltage during Normal Operation	V_{DD}	3.3 V Nominal	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

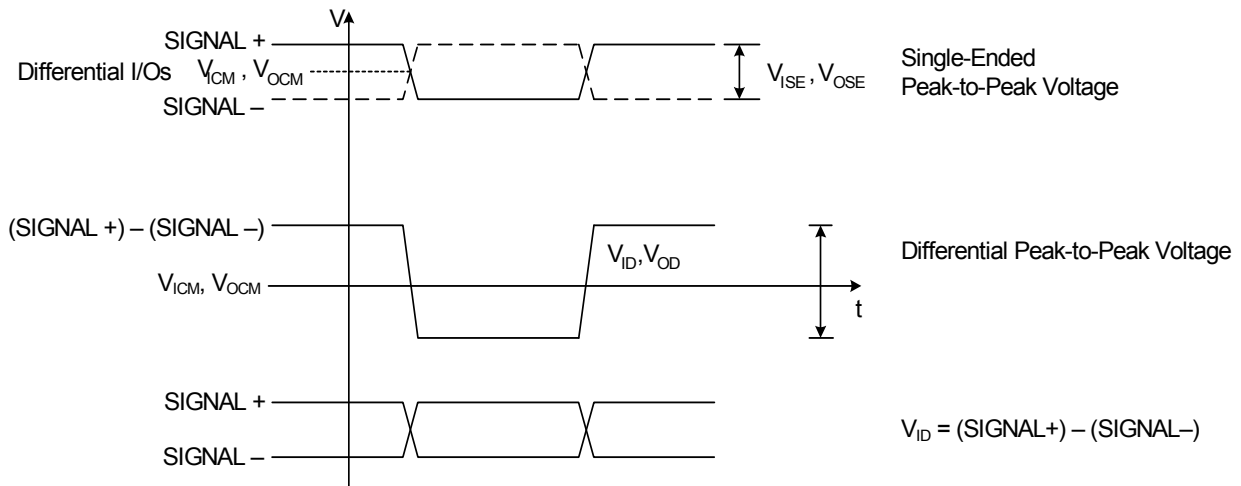


Figure 1. Differential Voltage Characteristics

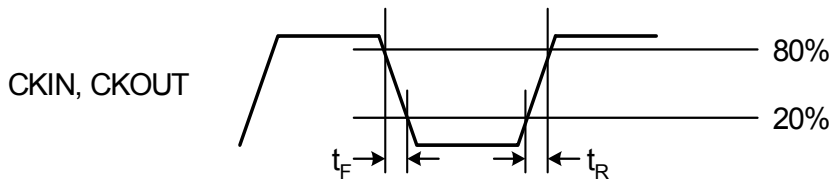


Figure 2. Rise/Fall Time Characteristics

Table 2. DC Characteristics $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current ¹	I_{DD}	LVPECL Format 622.08 MHz Out Both CKOUTs Enabled	—	251	279	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	217	243	mA
		CMOS Format 19.44 MHz Out Both CKOUTs Enabled	—	204	234	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	194	220	mA
		Disable Mode	—	165	—	mA
CKINn Input Pins²						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V \pm 5%	0.9	—	1.4	V
		2.5 V \pm 10%	1	—	1.7	V
		3.3 V \pm 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	k Ω
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	$f_{CKIN} < 212.5 \text{ MHz}$ See Figure 1.	0.2	—	—	V_{PP}
		$f_{CKIN} > 212.5 \text{ MHz}$ See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	$f_{CKIN} < 212.5 \text{ MHz}$ See Figure 1.	0.2	—	—	V_{PP}
		$f_{CKIN} > 212.5 \text{ MHz}$ See Figure 1.	0.25	—	—	V_{PP}
Output Clocks (CKOUTn)³						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
Notes:						
1. Current draw is independent of supply voltage						
2. No under- or overshoot is allowed.						
3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$.						
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						
5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$.						

Table 2. DC Characteristics (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	$V_{DD}-0.36$	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	$V_{DD} = 1.71 \text{ V}$ CMOS	$0.8 \times V_{DD}$	—	—	V

Notes:

1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$.

Table 2. DC Characteristics (Continued) $(V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Drive Current (CMOS driving into CKO _{VOL} for output low or CKO _{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO _{IO}	ICMOS[1:0] =11 $V_{DD} = 1.8 \text{ V}$	—	7.5	—	mA
		ICMOS[1:0] =10 $V_{DD} = 1.8 \text{ V}$	—	5.5	—	mA
		ICMOS[1:0] =01 $V_{DD} = 1.8 \text{ V}$	—	3.5	—	mA
		ICMOS[1:0] =00 $V_{DD} = 1.8 \text{ V}$	—	1.75	—	mA
		ICMOS[1:0] =11 $V_{DD} = 3.3 \text{ V}$	—	32	—	mA
		ICMOS[1:0] =10 $V_{DD} = 3.3 \text{ V}$	—	24	—	mA
		ICMOS[1:0] =01 $V_{DD} = 3.3 \text{ V}$	—	16	—	mA
		ICMOS[1:0] =00 $V_{DD} = 3.3 \text{ V}$	—	8	—	mA
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	$V_{DD} = 1.71 \text{ V}$	—	—	0.5	V
		$V_{DD} = 2.25 \text{ V}$	—	—	0.7	V
		$V_{DD} = 2.97 \text{ V}$	—	—	0.8	V
Input Voltage High	V_{IH}	$V_{DD} = 1.89 \text{ V}$	1.4	—	—	V
		$V_{DD} = 2.25 \text{ V}$	1.8	—	—	V
		$V_{DD} = 3.63 \text{ V}$	2.5	—	—	V
Notes:						
1. Current draw is independent of supply voltage						
2. No under- or overshoot is allowed.						
3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$.						
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						
5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$.						

Table 2. DC Characteristics (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3-Level Input Pins⁴						
Input Voltage Low	V_{ILL}		—	—	$0.15 \times V_{DD}$	V
Input Voltage Mid	V_{IMM}		$0.45 \times V_{DD}$	—	$0.55 \times V_{DD}$	V
Input Voltage High	V_{IHH}		$0.85 \times V_{DD}$	—	—	V
Input Low Current	I_{ILL}	See Note 4	-20	—	—	μA
Input Mid Current	I_{IMM}	See Note 4	-2	—	+2	μA
Input High Current	I_{IHH}	See Note 4	—	—	20	μA
LVC MOS Output Pins						
Output Voltage Low	V_{OL}	$I_O = 2 \text{ mA}$ $V_{DD} = 1.71 \text{ V}$	—	—	0.4	V
Output Voltage Low		$I_O = 2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$	—	—	0.4	V
Output Voltage High	V_{OH}	$I_O = -2 \text{ mA}$ $V_{DD} = 1.71 \text{ V}$	$V_{DD} - 0.4$	—	—	V
Output Voltage High		$I_O = -2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$	$V_{DD} - 0.4$	—	—	V
Disabled Leakage Current	I_{OZ}	RSTb = 0	-100	—	100	μA
Notes: <ol style="list-style-type: none"> 1. Current draw is independent of supply voltage 2. No under- or overshoot is allowed. 3. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$. 4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details. 5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$. 						

Table 3. Microprocessor Control $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I²C Bus Lines (SDA, SCL)						
Input Voltage Low	$V_{IL_{I2C}}$		—	—	$0.25 \times V_{DD}$	V
Input Voltage High	$V_{IH_{I2C}}$		$0.7 \times V_{DD}$	—	V_{DD}	V
Input Current	I_{I2C}	$V_{IN} = 0.1 \times V_{DD}$ to $0.9 \times V_{DD}$	-10	—	10	μA
Hysteresis of Schmitt trigger inputs	$V_{HYS_{I2C}}$	$V_{DD} = 1.8\text{V}$	$0.1 \times V_{DD}$	—	—	V
		$V_{DD} = 2.5 \text{ or } 3.3 \text{ V}$	$0.05 \times V_{DD}$	—	—	V
Output Voltage Low	$V_{OL_{I2C}}$	$V_{DD} = 1.8 \text{ V}$ $I_O = 3 \text{ mA}$	—	—	$0.2 \times V_{DD}$	V
		$V_{DD} = 2.5 \text{ or } 3.3 \text{ V}$ $I_O = 3 \text{ mA}$	—	—	0.4	V

Table 3. Microprocessor Control (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 V \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SPI Specifications						
Duty Cycle, SCLK	t_{DC}	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	t_c		100	—	—	ns
Rise Time, SCLK	t_r	20–80%	—	—	25	ns
Fall Time, SCLK	t_f	20–80%	—	—	25	ns
Low Time, SCLK	t_{lsc}	20–20%	30	—	—	ns
High Time, SCLK	t_{hsc}	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	t_{d3}		—	—	25	ns
Setup Time, SS to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SS to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Slave Selects	t_{cs}		25	—	—	ns

Table 4. AC Specifications $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin XA (XB with cap to GND)						
Input Resistance	XA_{RIN}	RATE[1:0] = LM, ML, MH, or HM, ac coupled	—	12	—	$k\Omega$
Input Voltage Swing	XA_{VPP}	RATE[1:0] = LM, ML, MH, or HM, ac coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Voltage Swing	XA/XB_{VPP}	RATE[1:0] = LM, ML, MH, or HM	0.5	—	1.2	V_{PP} , each.
CKINn Input Pins						
Input Frequency	CKN_F		0.002	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins						
(See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F	$N1 \geq 6$	0.002	—	945	MHz
		$N1 = 5$	970	—	1134	MHz
		$N1 = 4$	1.213	—	1.4	GHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output $V_{DD} = 1.71$ $C_{LOAD} = 5 \text{ pF}$	—	—	8	ns

Table 4. AC Specifications (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 V \pm 10\%$, $T_A = -40$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO _{TRF}	CMOS Output $V_{DD} = 2.97$ $C_{LOAD} = 5$ pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO _{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	+/-40	ps
LVC MOS Input Pins						
Minimum Reset Pulse Width	t _{RSTMN}		1			μ s
Reset to Microprocessor Access Ready	t _{READY}				10	ms
Input Capacitance	C _{in}		—	—	3	pF
LVC MOS Output Pins						
Rise/Fall Times	t _{RF}	$C_{LOAD} = 20$ pf See Figure 2	—	25	—	ns
LOS _n Trigger Window	LOS _{TRIG}	From last CKIN _n \uparrow to \downarrow Internal detection of LOS _n $N3 \neq 1$	—	—	4.5 x N3	T _{CKIN}
Time to Clear LOL after LOS Cleared	t _{CLRLOL}	\downarrow LOS to \downarrow LOL Fold = F _{new} Stable Xa/XB reference	—	10	—	ms
Device Skew						
Output Clock Skew	t _{SKEW}	\uparrow of CKOUT _n to \uparrow of CKOUT _m , CKOUT _n and CKOUT _m at same frequency and signal format PHASEOFFSET = 0 CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1	—	—	100	ps
Phase Change due to Temperature Variation	t _{TEMP}	Max phase changes from -40 to +85 °C	—	300	500	ps

Table 4. AC Specifications (Continued)(V_{DD} = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T_A = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance (f _{in} =f _{out} = 622.08 MHz; BW=120 Hz; LVPECL)						
Lock Time	t _{LOCKMP}	Start of ICAL to ↓ of LOL	—	35	1200	ms
Output Clock Phase Change	t _{P_STEP}	After clock switch f ₃ ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J _{PK}		—	0.05	0.1	dB
Jitter Tolerance	J _{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise f _{out} = 622.08 MHz	CKO _{PN}	1 kHz Offset	—	-106	-87	dBc/Hz
		10 kHz Offset	—	-121	-100	dBc/Hz
		100 kHz Offset	—	-132	-104	dBc/Hz
		1 MHz Offset	—	-132	-119	dBc/Hz
Subharmonic Noise	SP _{SUBH}	Phase Noise @ 100 kHz Offset	—	-88	-76	dBc
Spurious Noise	SP _{SPUR}	Max spur @ n x F ₃ (n ≥ 1, n x F ₃ < 100 MHz)	—	-93	-70	dBc

Table 5. Jitter Generation

Parameter	Symbol	Test Condition*		Min	Typ	Max	GR-253-Specification	Unit
		Measurement Filter	DSPLL BW ²					
Jitter Gen OC-192	JGEN	0.02–80 MHz	120 Hz	—	4.2	6.2	30	ps _{pp}
				—	.27	.42	N/A	ps _{rms}
		4–80 MHz	120 Hz	—	3.7	6.4	10	ps _{pp}
				—	.14	0.31	N/A	ps _{rms}
		0.05–80 MHz	120 Hz	—	4.4	6.9	10	ps _{pp}
				—	.26	0.41	1.0	ps _{rms}
Jitter Gen OC-48	JGEN	0.12–20 MHz	120 Hz	—	3.5	5.4	40.2	ps _{pp}
				—	.27	0.41	4.02	ps _{rms}

***Note:** Test conditions:
1. f_{IN} = f_{OUT} = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 120 Hz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. V_{DD} = 2.5 V
7. T_A = 85 °C

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ _{JA}	Still Air	32	C°/W
Thermal Resistance Junction to Case	θ _{JC}	Still Air	14	C°/W

Table 7. Absolute Limits

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		-0.5	—	3.8	V
LVC MOS Input Voltage	V_{DIG}		-0.3		$V_{DD}+0.3$	V
CKINn Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Operating Junction Temperature	T_{JCT}		-55	—	150	°C
Storage Temperature Range	T_{STG}		-55	—	150	°C
ESD HBM Tolerance (100 pF, 1.5 k Ω); All pins except CKIN+/CKIN-			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN-			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 k Ω); CKIN+/CKIN-			750	—	—	V
ESD MM Tolerance; CKIN+/CKIN-			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			

2. Typical Phase Noise Performance

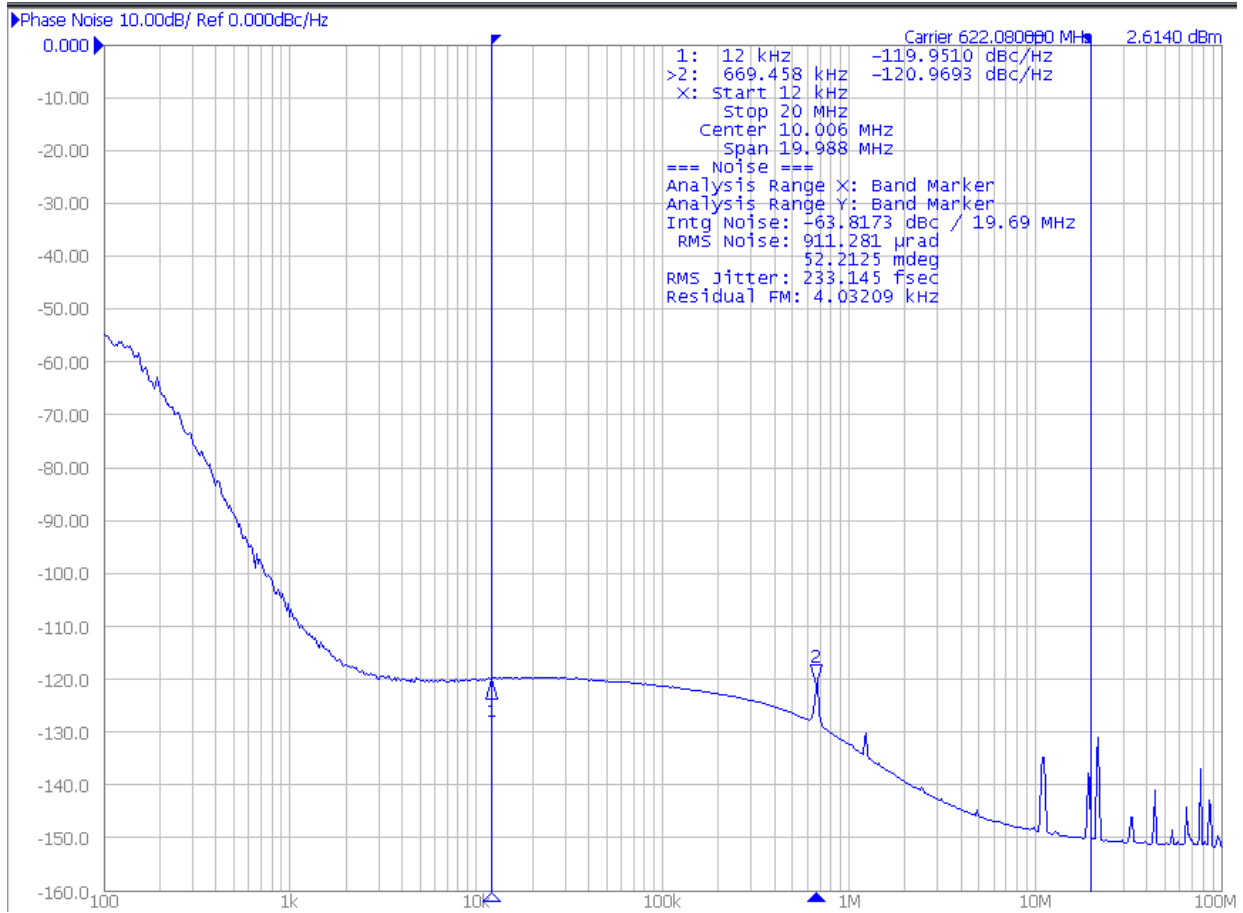


Figure 3. Typical Phase Noise Plot

Jitter Band	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	249 fs
SONET_OC192_A, 20 kHz to 80 MHz	274 fs
SONET_OC192_B, 4 MHz to 80 MHz	166 fs
SONET_OC192_C, 50 kHz to 80 MHz	267 fs
Brick Wall_800 Hz to 80 MHz	274 fs
<p>*Note: Jitter integration bands include low-pass (-20 dB/Dec) and hi-pass (-60 dB/Dec) roll-offs per Telecordia GR-253-CORE.</p>	

3. Typical Application Circuit

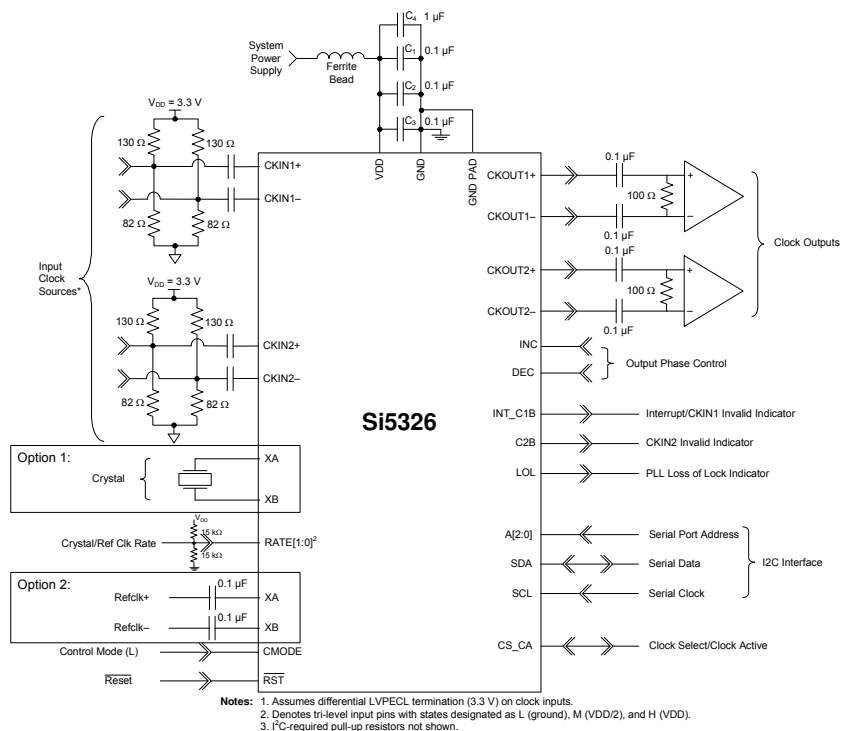


Figure 4. Si5326 Typical Application Circuit (I²C Control Mode)

Note: For an example schematic and layout, refer to the Si5325/26-EVB User's Guide.

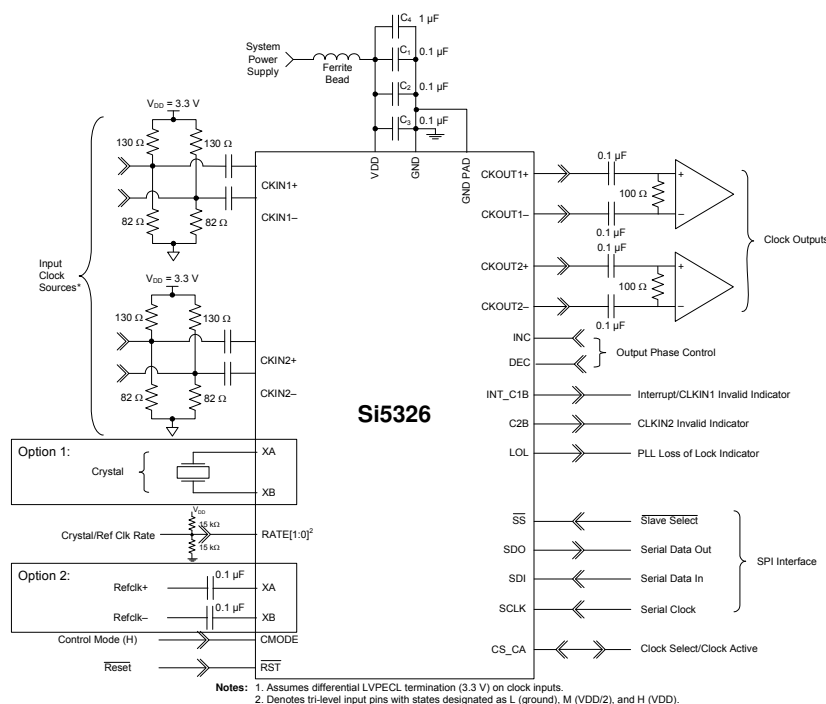


Figure 5. Si5326 Typical Application Circuit (SPI Control Mode)

Note: For an example schematic and layout, refer to the Si5325/26-EVB User's Guide.

4. Functional Description

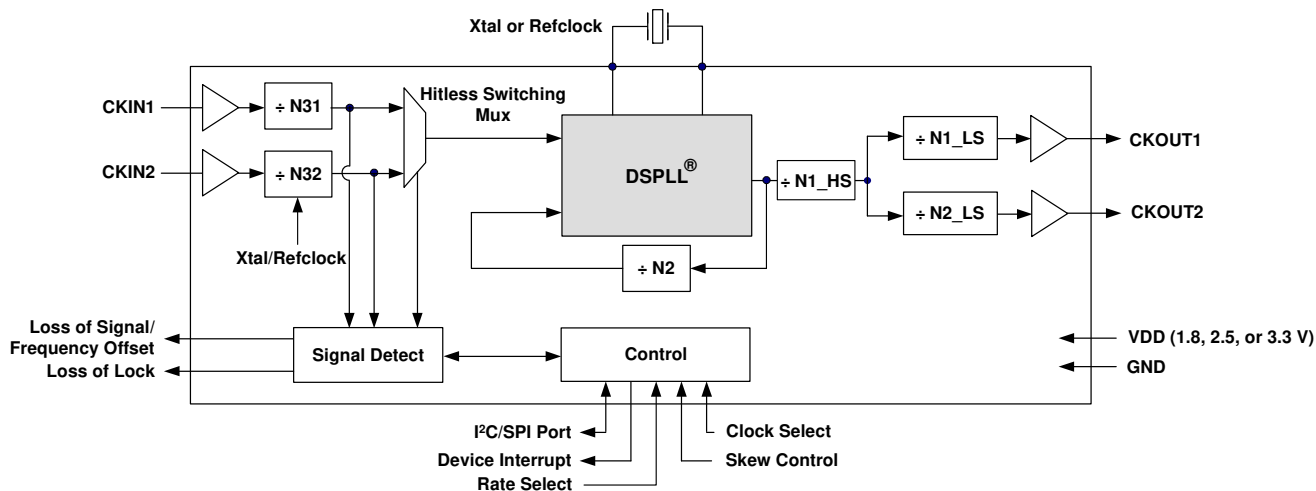


Figure 6. Functional Block Diagram

The Si5326 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5326 accepts two input clocks ranging from 2 kHz to 710 MHz and generates two output clocks ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The Si5326 can also use its crystal oscillator as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for each input clock and output clock, so the Si5326 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5326 input clock frequency and clock multiplication ratio are programmable through an I²C or SPI interface. Silicon Laboratories offers a PC-based software utility, *DSPLLsim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from <http://www.silabs.com/timing>.

The Si5326 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5326 PLL loop bandwidth is digitally programmable and supports a range from 60 Hz to 8.4 kHz. The *DSPLLsim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5326 supports hitless switching between the two synchronous input clocks in compliance with GR-253-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (maximum 200 ps phase change). Manual and automatic revertive and non-revertive input clock switching options are available. The Si5326 monitors both input clocks for loss-of-signal (LOS) and provides a LOS alarm (INT_C1B and C2B) when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. The Si5326 also monitors frequency offset alarms (FOS), which indicate if an input clock is within a specified frequency band relative to the frequency of a reference clock. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported. The Si5326 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average frequency that existed for a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5326 has two differential clock outputs. The electrical format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control using the *CLAT*[7:0] register. Fine phase adjustment is available and is set using the *FLAT* register bits. The nominal range and resolution of the *FLAT*[14:0] skew adjustment word are: ± 110 ps and 3 ps, respectively. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. See Table 8 for instructions on ensuring output-to-output alignment. The input to output skew is not specified. The *DSPLLsim* software utility determines the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

4.1. External Reference

An external, high quality clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high quality crystal. Specific recommendations may be found in the Family Reference Manual.

In digital hold, the DSPLL remains locked and tracks the external reference. Note that crystals can have temperature sensitivities.

4.2. Further Documentation

Consult the Silicon Laboratories Si53xx Any Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5326 functions. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called *DSPLLsim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from <http://www.silabs.com/timing>.

Table 8. CKOUT_ALWAYS_ON and SQ_ICAL Truth Table

CKOUT_ALWAYS_ON	SQ_ICAL	Results
0	0	CKOUT OFF until after the first ICAL
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)
1	0	CKOUT always ON, including during an ICAL
1	1	CKOUT always ON, including during an ICAL. Use these settings to preserve output-to-output skew

5. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

Register	D7	D6	D5	D4	D3	D2	D1	D0
0		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS_REG	
1					CK_PRIOR2[1:0]		CK_PRIOR[1:0]	
2	BWSEL_REG[3:0]							
3	CKSEL_REG[1:0]		DHOLD	SQ_ICAL				
4	AUTOSEL_REG[1:0]		HST_DEL[4:0]					
5	ICMOS[1:0]							
6		SLEEP	SFOUT2_REG[2:0]			SFOUT1_REG[2:0]		
7						FOSREFSEL[2:0]		
8	HLOG_2[1:0]		HLOG_1[1:0]					
9	HIST_AVG[4:0]							
10					DSBL2_REG	DSBL1_REG		
11							PD_CK2	PD_CK1
16	CLAT[7:0]							
17	FLAT_VALID	FLAT[14:8]						
18	FLAT[7:0]							
19	FOS_EN	FOS_THR[1:0]		VALTIME[1:0]		LOCK[T2:0]		
20					CK2_BAD_PIN	CK1_BAD_PIN	LOL_PIN	INT_PIN
21	INCDEC_PIN						CK1_ACTV_PIN	CKSEL_PIN
22					CK_ACTV_POL	CK_BAD_POL	LOL_POL	INT_POL
23						LOS2_MSK	LOS1_MSK	LOSX_MSK
24						FOS2_MSK	FOS1_MSK	LOL_MSK
25	N1_HS[2:0]							
31					NC1_LS[19:16]			
32	NC1_LS[15:8]							

Register	D7	D6	D5	D4	D3	D2	D1	D0	
33	NC1_LS[7:0]								
34	NC2_LS[19:16]								
35	NC2_LS[15:8]								
36	NC2_LS[7:0]								
40	N2_HS[2:0]			N2_LS[19:16]					
41	N2_LS[15:8]								
42	N2_LS[7:0]								
43	N31[18:16]								
44	N31[15:8]								
45	N31[7:0]								
46	N32[18:16]								
47	N32[15:8]								
48	N32[7:0]								
55	CLKIN2RATE[2:0]				CLKIN1RATE[2:0]				
128							CK2_ACT-V_REG	CK1_ACT-V_REG	
129							LOS2_INT	LOS1_INT	LOSX_INT
130	CLATPROG-RESS	DIGHOLD-VALID					FOS2_INT	FOS1_INT	LOL_INT
131							LOS2_FLG	LOS1_FLG	LOSX_FLG
132							FOS2_FLG	FOS1_FLG	LOL_FLG
134	PARTNUM_RO[11:4]								
135	PARTNUM_RO[3:0]				REVID_RO[3:0]				
136	RST_REG	ICAL							GRADE_RO[1:0]
138							LOS2_EN [1:1]	LOS1_EN [1:1]	
139			LOS2_EN [0:0]	LOS1_EN [0:0]				FOS2_EN	FOS1_EN
142	INDEPENDENTSKEW1[7:0]								
143	INDEPENDENTSKEW2[7:0]								

6. Register Descriptions

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS_REG	
Type	R	R/W	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7	Reserved	Reserved.
6	FREE_RUN	Free Run. Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its XA-XB reference. 0: Disable 1: Enable
5	CKOUT_ALWAYS_ON	CKOUT Always On. This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 8 on page 19. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Note: The frequency may be significantly off and variable until the part is calibrated.
4:2	Reserved	Reserved.
1	BYPASS_REG	Bypass Register. This bit enables or disables the PLL bypass mode. Use only when the device is in digital hold or before the first ICAL. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing the PLL. Bypass mode does not support CMOS clock outputs.
0	Reserved	Reserved.

Register 1.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
Type	R				R/W		R/W	

Reset value = 1110 0100

Bit	Name	Function
7:4	Reserved	Reserved.
3:2	CK_PRIOR2 [1:0]	CK_PRIOR 2. Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority. 01: CKIN2 is 2nd priority. 10: Reserved 11: Reserved
1:0	CK_PRIOR1 [1:0]	CK_PRIOR 1. Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN1 is 1st priority. 01: CKIN2 is 1st priority. 10: Reserved 11: Reserved

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]				Reserved			
Type	R/W				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	BWSEL_REG. Selects nominal f3dB bandwidth for PLL. See DSPLL <i>sim</i> for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	Reserved.

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CKSEL_REG [1:0]		DHOLD	SQ_ICAL	Reserved			
Type	R/W		R/W	R/W	R			

Reset value = 0000 0101

Bit	Name	Function
7:6	CKSEL_REG [1:0]	<p>CKSEL_REG.</p> <p>If the device is operating in register-based manual clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1 and AUTOSEL_REG = 00, the CS_CA input pin continues to control clock selection and CKSEL_REG is of no consequence.</p> <p>00: CKIN_1 selected. 01: CKIN_2 selected. 10: Reserved 11: Reserved</p>
5	DHOLD	<p>DHOLD.</p> <p>Forces the part into digital hold. This bit overrides all other manual and automatic clock selection controls.</p> <p>0: Normal operation. 1: Force digital hold mode. Overrides all other settings and ignores the quality of all of the input clocks.</p>
4	SQ_ICAL	<p>SQ_ICAL.</p> <p>This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 8 on page 19.</p> <p>0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.</p>
3:0	Reserved	Reserved.

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTOSEL_REG [1:0]		Reserved	HIST_DEL [4:0]				
Type	R/W		R	R/W				

Reset value = 0001 0010

Bit	Name	Function
7:6	AUTOSEL_REG [1:0]	AUTOSEL_REG [1:0]. Selects method of input clock selection to be used. 00: Manual (either register or pin controlled, see CKSEL_PIN) 01: Automatic Non-Revertive 10: Automatic Revertive 11: Reserved See the Si53xx Family Reference Manual for a detailed description.
5	Reserved	Reserved.
4:0	HIST_DEL [4:0]	HIST_DEL [4:0]. Selects amount of delay to be used in generating the history information used for Digital Hold. See the Si53xx Family Reference Manual for a detailed description.

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMOS [1:0]		Reserved					
Type	R/W		R					

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	ICMOS [1:0]. When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 8mA/2mA 01: 16mA/4mA 10: 24mA/6mA 11: 32mA/8mA
5:0	Reserved	Reserved.