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Si53301/4-EVB

Si53301/4 Evaluation Board User's Guide

Description

The Si53301/4-EVB is used for evaluation of the Si533xx family of low-jitter clock buffers/level translators. As shipped from the factory, this evaluation board has the Si53301 device installed. The entire Si533xx family of buffers use the same input circuits and output drivers, and all have the same jitter specifications. Thus, this evaluation board can be used to evaluate any Si533xx device. The Si53301 provides pin-selectable clock output signal format, drive strength control, optional clock division, and per-bank output enable. The Si53304 provides pin-selectable clock output signal format, drive strength control, and individual output enable pins for each clock output.

EVB Features

Features of this evaluation board include:

- Power supply connections for VDD, VDDOA and VDDOB, GND
- Jumpers for selection of output signal format, output enable, input clock select and output divider
- Jumpers to allow self biasing of CMOS single-ended inputs
- SMA connectors for easy access to test and evaluate the Si53301

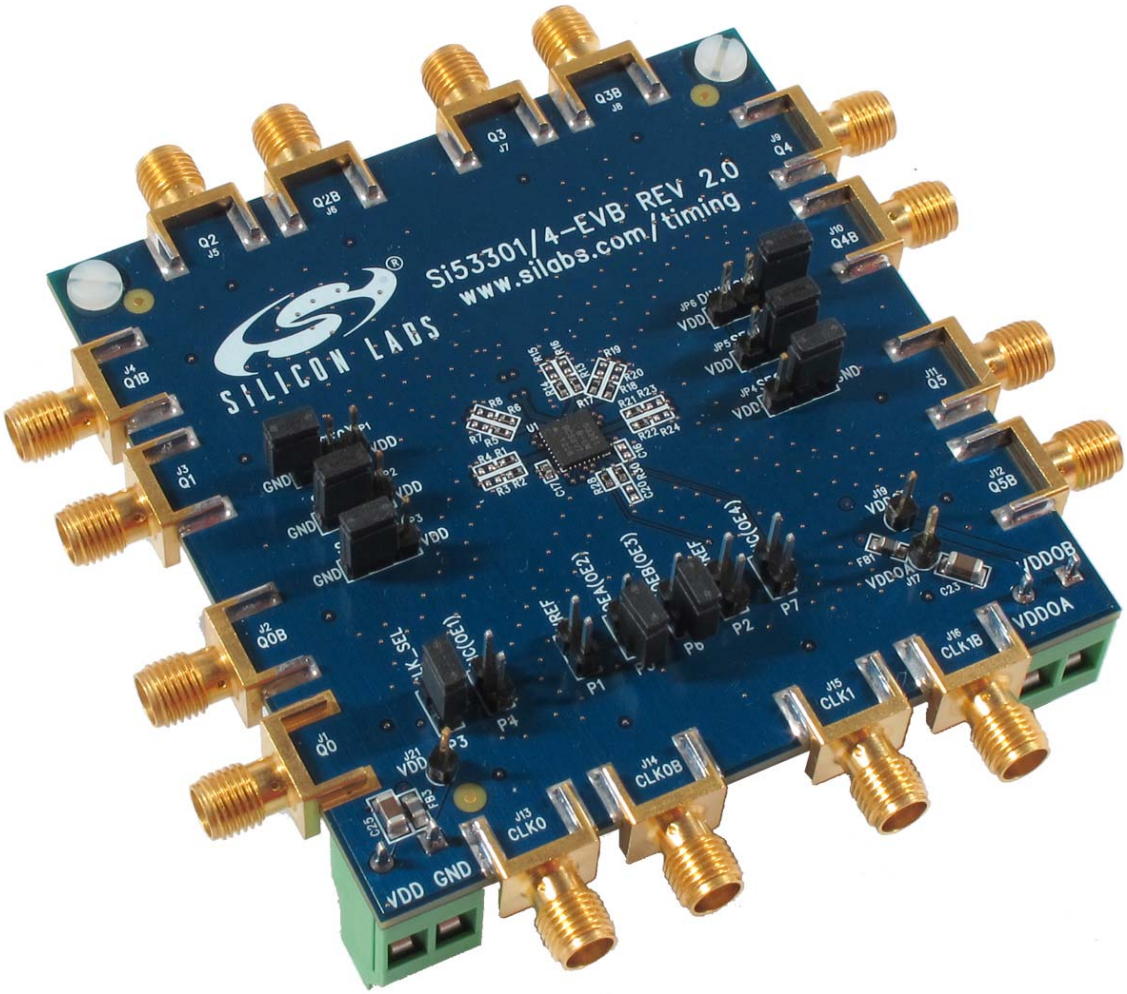

Figure 1. Si53301/4 Evaluation Board

1. Supply Voltage

Three supply voltages are required: VDD, VDDOA, and VDDOB. These supply voltages are applied at the two bottom corners of the evaluation board via J18 and J20, which are located on the bottom side of the evaluation board and function as standoffs as well as inputs for the supply voltages. Note that the J18 and J20 have silkscreen on the top side of the evaluation board that identifies the J18 and J20 inputs. VDD powers the input buffers, mux, and dividers. VDDOA and VDDOB provide power for the output drivers on CLK0,1,2 and CLK3,4,5, respectively. The three input power supply voltages should all have a common external ground. A separate ground wire should be run from the common power ground to the ground on both J18 and J20. VDD, VDDOA, and VDDOB can be 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±10%. VDDOA,B need to be set according to the output driver format as shown in Table 1.

2. Clock Inputs

This evaluation board accepts differential clock inputs on SMA connectors labeled CLK0,CLK0B as well as CLK1,CLK1B. A single-ended CMOS input with the same voltage swing as the VDD voltage may also be applied to either CLK0 and/or CLK1. See “4.4. Jumpers P1 and P2” for more information. The clock input that is active is selected by JP1, which controls the CLK_SEL input pin 8.

3. Clock Outputs

Six clock outputs are present at the SMA connectors labeled Q0, 1, 2, 3, 4, 5. As built and delivered, the evaluation board will support differential outputs that are LVDS, CML, or low-power LVPECL without any component changes. Standard LVPECL and HCSL outputs require output resistor and/or capacitor changes. See the table in Figure 3 for these changes.

4. Jumpers

This evaluation board can be used to evaluate a Si53301 or Si53304; however, the Si53301 is installed on the evaluation board. Refer to Figures 1, 2, and 3 and Tables 1 and 2 as needed for the following discussion about the jumpers. Many of the inputs are shown on the evaluation board silkscreen and schematic with dual names, such as name1(name2), where name1 is the input pin name for the Si53301 and name2 is the input pin name for the Si53304. In two cases, the input pin of the Si53301 is a no-connect (NC) when the Si53304 is a functional input.

4.1. Jumpers JP2 and JP3

Jumpers JP2 and JP3 set the level to SFOUTA1 and SFOUTA0 on input pins 2 and 3, respectively. Jumpers JP4 and JP5 set the level to SFOUTB1 and SFOUTB0 on input pins 22 and 23, respectively. These inputs have three valid input levels: Ground, VDD, and Open. See Table 1.

4.2. Jumpers JP1 and JP6

For the Si53301 device, Jumpers JP1 and JP6 control the output dividers for bank A (Q0,1,2) and bank B (Q3,4,5), respectively. For the Si53304 device, Jumpers JP1 and JP6 control the enabling of output clocks Q1 and Q5, respectively. See Table 2 for the settings of these jumpers.

4.3. Jumpers P3, P4, P5, P6, and P7

For the Si53301, these jumpers control CLK_SEL, OEA, and OEB. OEA is the enable for output clocks Q0,1,2, and OEB is the enable for output clocks Q3,4,5. For the Si53304, these jumpers control CLK_SEL, OE1, OE2, OE3, and OE4. See Table 3 for more information.

4.4. Jumpers P1 and P2

Jumpers P1 and P2 should be left open unless a single-ended input is applied to the CLK0 or CLK1 input. When a jumper is placed across P1 (P2), the voltage from the VREF pin 17 is applied to the CLK0B (CLK1B) input pin so that a CMOS input with a voltage swing of VDD (pin7) volts can be applied to the CLK0 (CLK1) pin. In addition, some resistor and capacitor changes (described in the Figure 3 schematic near P1 and P2) must be made to the evaluation board.

Table 1. JP2, JP3, JP4, and JP5 Output Signal Format

SFOUTX1[1]	SFOUTX0[1]	VDDOX = 3.3 V	VDDOX = 2.5 V	VDDOX = 1.8 V
Open[2]	Open[2]	LVPECL	LVPECL	N/A
Ground	Ground	LVDS	LVDS	LVDS
Ground	VDD	LVCMOS, 24 mA drive	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive
VDD	Ground	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive
VDD	VDD	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive	LVCMOS, 6 mA drive
Open[2]	Ground	LVCMOS, 6 mA drive	LVCMOS, 4 mA drive	LVCMOS, 2 mA drive
Open[2]	VDD	LVPECL Low power	LVPECL Low power	N/A
Ground	Open[2]	CML	CML	CML
VDD	Open[2]	HCSL	HCSL	HCSL

Notes:
1. Ground means short center pin to ground pin. VDD means short center pin to VDD pin. Open means leave center pin open.
2. SFOUTX are three-level input pins.

Table 2. Jumper Selections for JP1,6

		Si53301			Si53304		
Signal*	Jumper	Jumper Position			Jumper Position		
		Ground	Open	VDD	Ground	Open	VDD
DIVA(OE1)	JP1	/2	/1	/4	Q1 Disabled	Q1 Enabled	Q1 Enabled
DIVB(OE5)	JP6	/2	/1	/4	Q5 Disabled	Q5 Enabled	Q5 Enabled

***Note:** The signal name in parentheses applies to the Si53304 device, which is not installed from the factory.

Table 3. Jumper Selections for P3,4,5,6,7

		Si53301		Si53304	
Signal*	Jumper	Jumper Position		Jumper Position	
		Shorted	Open	Shorted	Open
CLK_SEL	P3	CLK0 Selected	CLK1 Selected	CLK0 Selected	CLK1 Selected
NC(OE1)	P4	NA	NA	Q1 Disabled	Q1 Enabled
OEA(OE2)	P5	Q0,1,2 Disabled	Q0,1,2 Enabled	Q2 Disabled	Q2 Enabled
OEB(OE3)	P6	Q3,4,5 Disabled	Q3,4,5 Enabled	Q3 Disabled	Q3 Enabled
NC(OE4)	P7	NA	NA	Q4 Disabled	Q4 Enabled

***Note:** The signal name in parentheses applies to the Si53304 device, which is not installed from the factory.

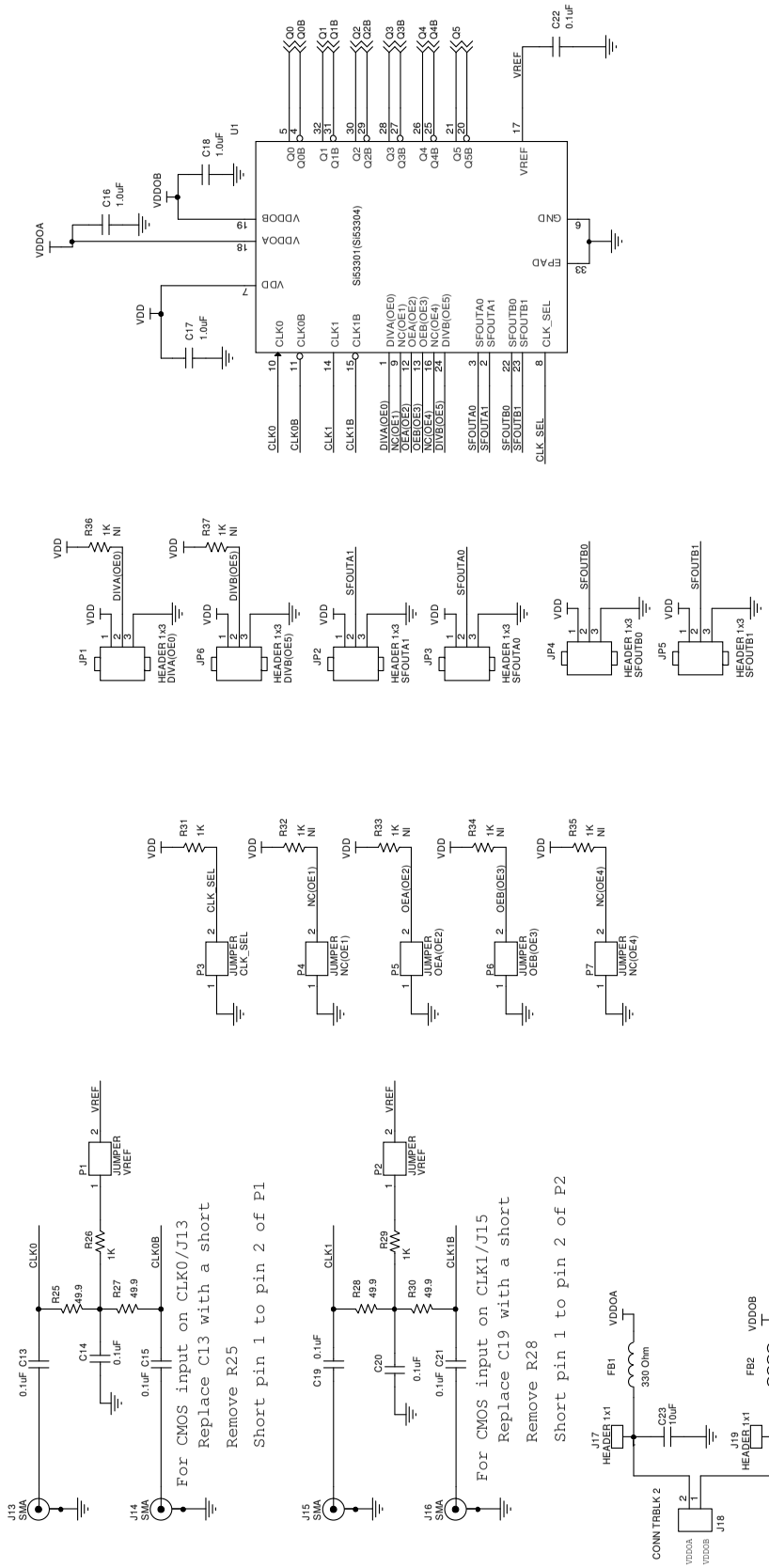

Figure 2. Schematic Main

All resistors on this page are located very close to the Si533xx device, caps are located very close to the SMA's

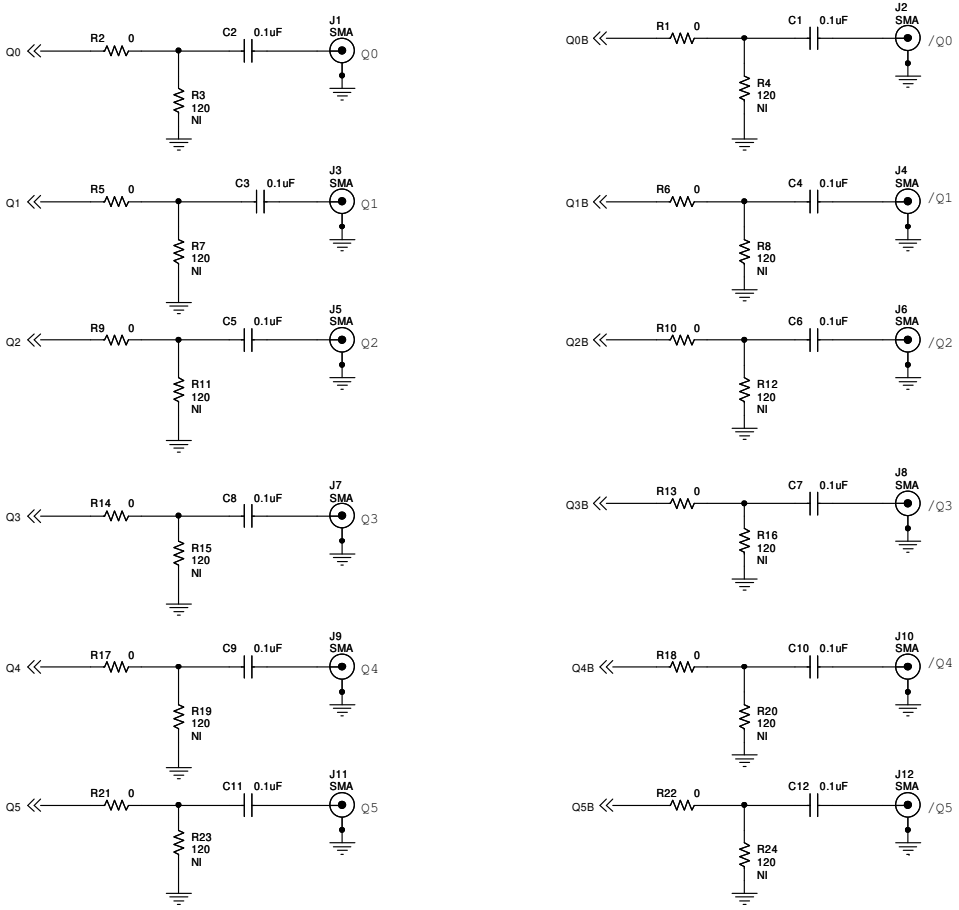

Figure 3. Schematic Outputs

Component Configurations For Various Output Formats

Output Format	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10,C11,C12	R1, R2, R5, R6, R9, R10, R13,R14, R17, R18,R21, R22	R3, R4, R7, R8, R11,R12, R15,R16,R19, R20,R23,R24
HCSL SAME BD	0 OHMS	0	NP
HCSL ADD-IN	0 OHMS	42.2	86.6
LOW POWER LVPECL	0.1 uF	0	NP
STANDARD LVPECL	0.1 uF	0	See note
LVDS AC/DC	0.1 uF/0 ohms	0	NP
CML	0.1 uF	0	NP
CMOS	0 OHMS	0	NP

Note : 90 for VDD = 2.5V; 120 for VDD = 3.3V

5. Bill of Materials

Table 4. Si53301/4-EVB Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part #	Mfr
19	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C19, C20, C21, C22	0.1 µF		10 V	±10%	X7R	C0402	C0402X7R100-104K	Venkel
3	C16, C17, C18	1.0 µF		6.3 V	±10%	X5R	C0402	C0402X5R6R3-105K	Venkel
3	C23, C24, C25	10 µF		10 V	±20%	X7R	C1206	C1206X7R100-106M	Venkel
3	FB1, FB2, FB3	330 Ω	1500 mA			SMT	L0805	BLM21PG331SN1	MuRata
16	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16	SMA				SMA	SMA-EDGE-3	142-0701-801	Johnson Components
3	J17, J19, J21	Header 1x1				Header	CONN-1X1	TSW-101-14-T-S	Samtec
2	J18, J20	CONN TRBLK 2	24 A			Term Blk	CONN-TB-1711026	1711026	Phoenix Contact
6	JP1, JP2, JP3, JP4, JP5, JP6	Header 1x3				Header	CONN-1X3	TSW-103-07-T-S	Samtec
9	JS1, JS2, JS3, JS4, JS5, JS6, JS7, JS8, JS9	Jumper Shunt				Shunt	N/A	SNT-100-BK-T	Samtec
2	MH1, MH2	Screw/ Standoff				HDW	MH-125NP	NSS-4-4-01/2399	Various
7	P1, P2, P3, P4, P5, P6, P7	Jumper				Header	CONN1X2	TSW-102-07-L-S	Samtec
12	R1, R2, R5, R6, R9, R10, R13, R14, R17, R18, R21, R22	0	1 A			Thick-Film	R0402	CR0402-16W-000	Venkel
4	R25, R27, R28, R30	49.9 Ω	1/16 W		±1%	Thick-Film	R0402	CR0402-16W-49R9F	Venkel
3	R26, R29, R31	1 kΩ	1/16 W		±5%	Thick-Film	R0402	CR0402-16W-102J	Venkel
1	U1	Si53301				Timing	QFN32M5X5 P0.5	Si53301-A-GM	SiLabs

Table 4. Si53301/4-EVB Bill of Materials (Continued)

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part #	Mfr
Not-Installed Components									
12	R3, R4, R7, R8, R11, R12, R15, R16, R19, R20, R23, R24	120 Ω	1/16 W		±1%	Thick-Film	R0402	CR0402-16W-1200F	Venkel
6	R32, R33, R34, R35, R36, R37	1 kΩ	1/16 W		±5%	Thick-Film	R0402	CR0402-16W-102J	Venkel

Document Change List

Revision 0.1 to Revision 0.3

- Comprehensive rewrite of previous revision.

NOTES:

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