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Si53303

DUAL 1:5 LOW JITTER BUFFER/LEVEL TRANSLATOR

Features

- 10 differential or 20 LVCMOS outputs
- Ultra-low additive jitter: 100 fs rms
- Wide frequency range: 1 to 725 MHz
- Any-format input with pin selectable output formats: LVPECL, Low Power LVPECL, LVDS, CML, HCSL, LVCMOS
- Synchronous output enable
- Output clock division: /1, /2, /4
- Low output-output skew: <50 ps
- Low propagation delay variation: <400 ps
- Independent V_{DD} and V_{DDO} : 1.8/2.5/3.3 V
- Excellent power supply noise rejection (PSRR)
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 44-QFN (7 mm x 7 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C

Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Description

The Si53303 is an ultra low jitter dual 1:5 differential output buffer with pin-selectable output clock signal format and divider selection. The Si53303 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53303 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

Functional Block Diagram

Ordering Information:
See page 25.

Pin Assignments

Si53303
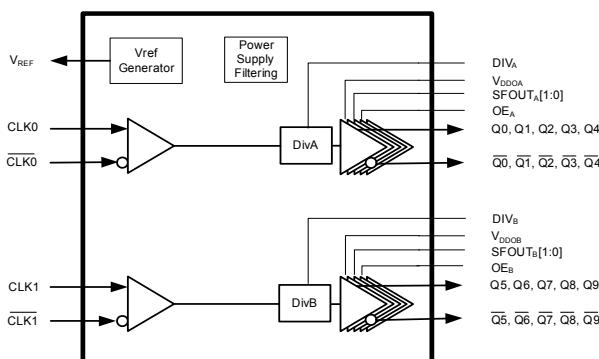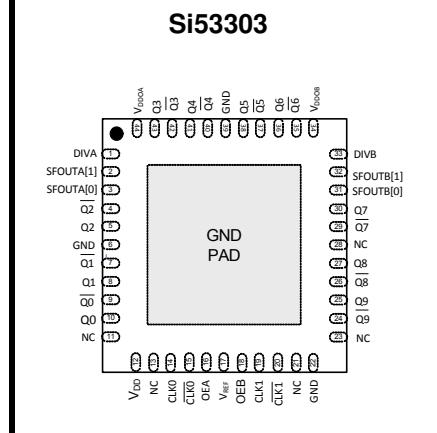
Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range*	V_{DD}	LVDS, CML, HCSL, LVCMOS	1.71	1.8	1.89	V
		LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
Output Buffer Supply Voltage*	V_{DDO}	LVDS, CML, HCSL, LVCMOS	1.71	—	1.89	V
		LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS	2.38	—	2.63	V
			2.97	—	3.63	V
*Note: Core supply VDD and output buffer supplies V_{DDO} are independent.						

Table 2. Input Clock Specifications
(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}	VDD=2.5V$\pm$5%, 3.3V$\pm$10%	0.05	—	—	V
Input Swing (single-ended, peak-to-peak)	V_{IN}		0.1	—	1.1	V
Input Voltage High	V_{IH}		VDD x 0.7	—	—	V
Input Voltage Low	V_{IL}		—	—	VDD x 0.3	V
Input Capacitance	C_{IN}		—	5	—	pF

Table 3. DC Common Characteristics

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^{\circ}$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	TBD	100	mA
Output Buffer Supply Current (Per Clock Output) @100 MHz	I_{DDOX}	LVPECL (3.3 V)	—	35	—	mA
		Low Power LVPECL (3.3 V)	—	30	—	mA
		LVDS (3.3 V)	—	20	—	mA
		CML (3.3 V)	—	30	—	mA
		HCSL, 100 MHz, 2 pF load (3.3 V)	—	35	—	mA
		CMOS (1.8 V, SFOUT = Open/0), per output, C_L = 5 pF, 200 MHz	—	5	—	mA
		CMOS (2.5 V, SFOUT=Open/0), per output, C_L=5pF, 200 MHz	—	8	—	mA
		CMOS (3.3 V, SFOUT = 0/1), per output, C_L = 5 pF, 200 MHz	—	15	—	mA
Leakage Current	I_L	Input leakage at all inputs except CLKIN, V_{IN} = 0 V	—	—	TBD	µA
		Input leakage at CLKIN V_{IN} = 0 V	—	—	TBD	µA
Voltage Reference	V_{REF}	V_{REF} pin	—	VDD/2	—	V
Input High Voltage	V_{IH}	SFOUTX, DIVX 3-level input pins	0.85 x VDD	—	—	V
Input Mid Voltage	V_{IM}	SFOUTX, DIVX 3-level input pins	0.45 x VDD	0.5 x VDD	0.55 x VDD	V
Input Low Voltage	V_{IL}	SFOUTX, DIVXpin 3-level input pins	—	—	0.15 x VDD	V
Internal Pull-down Resistor	R_{DOWN}	CLK_SEL, DIVA, DIVB, SFOUTA[1], SFOUTB[1]	—	25	—	kΩ
Internal Pull-up Resistor	R_{UP}	SFOUTA[1], SFOUTB[1], DIVA, DIVB, OEA, OEB	—	25	—	kΩ

Table 4. DC Characteristics—LVPECL and Low Power LVPECL

(V_{DD} = 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^\circ$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	V_{OH}	R_L = 50 Ω to V_{DDOX} – 2 V	V_{DDOX} – 1.145	—	V_{DDOX} – 0.895	V
Output Voltage Low	V_{OL}	R_L = 50 Ω to V_{DDOX} – 2 V	V_{DDOX} – 1.945	—	V_{DDOX} – 1.695	V
Output DC Common Mode Voltage	V_{COM}		V_{DDOX} – 1.895	—	V_{DDOX} – 1.425	V
Single-Ended Output Swing	V_{SE}	Terminate unused outputs to R_L = 50 Ω to V_{DDOX} – 2 V	0.25	0.60	0.85	V

Table 5. DC Characteristics—CML

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^\circ$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	V_{SE}	Terminated as shown in Figure 7 (CML termination).	300	400	500	mV

Table 6. DC Characteristics—LVDS

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^\circ$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	V_{SE}	R_L = 100 Ω across Q_N and $\overline{Q}_N$	247	—	454	mV
Output Common Mode Voltage (V_{DDO} = 2.5 V or 3.3 V)	V_{COM1}	V_{DDOX} = 2.38 to 2.63 V, 2.97 to 3.63 V, R_L = 100 Ω across Q_N and $\overline{Q}_N$	1.10	1.25	1.35	V
Output Common Mode Voltage (V_{DDO} = 1.8 V)	V_{COM2}	V_{DDOX} = 1.71 to 1.89 V, R_L = 100 Ω across Q_N and $\overline{Q}_N$	0.85	0.97	1.10	V

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Table 7. DC Characteristics—LVCMOS

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^{\circ}$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High[*]	V_{OH}		0.8 x V_{DDOX}	—	—	V
Output Voltage Low[*]	V_{OL}		—	—	0.2 x V_{DDOX}	V
*Note: I_{OH} and I_{OL} per the Output Signal Format Table for specific V_{DDOX} and SFOUTX settings.						

Table 8. DC Characteristics—HCSL

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^{\circ}$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	V_{OH}	R_L = 50 Ω to GND	550	700	850	mV
Output Voltage Low	V_{OL}	R_L = 50 Ω to GND	–150	0	150	mV
Single-Ended Output Swing	V_{SE}	R_L = 50 Ω to GND	—	700	—	mV
Crossing Voltage	V_C	R_L = 50 Ω to GND	250	350	550	mV

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Table 9. AC Characteristics

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%,T_A = –40 to 85 $^{\circ}$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL, low power LVPECL, LVDS, CML, HCSL	1	—	725	MHz
		LVCMOS	1	—	200	MHz
Duty Cycle **Note:** 50% input duty cycle.	D_C	200 MHz, 50 Ω to V_{DD}/2, 20/80% T_R/T_F<10% of period (LVCMOS)	TBD	TBD	TBD	%
		20/80% T_R/T_F<10% of period (Differential)	48	50	52	%
Minimum Input Clock Slew Rate[1]	SR	Required to meet prop delay and additive jitter specifications (20-80%)	0.75	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	LVPECL, LVDS, CML, HCSL, 20/80%			350	ps
		200 MHz, 50 Ω, 20/80%, 2 pF load (LVCMOS)	TBD	TBD	750	ps
Minimum Input Pulse Width	T_W		500	—	—	ps
Additive Jitter (Differential Clock Input)	J	V_{DD} = 2.5/3.3 V, LVPECL/LVDS, F = 725 MHz, 0.75 V/ns input slew rate	—	60	80	fs
Propagation Delay	T_{PLH}, T_{PHL}	Low to high, high to low Single-ended	TBD	—	TBD	ns
		Low to high, high to low Differential	TBD	—	TBD	ns
Output Enable Time[2]	T_{EN}	F = 1 MHz	—	2	—	μs
		F = 100 MHz	—	60	—	ns
		F = 725 MHz	—	50	—	ns
Output Disable Time[2]	T_{DIS}	F = 1 MHz	—	2	—	μs
		F = 100 MHz	—	25	—	ns
		F = 725 MHz	—	15	—	ns

Notes:
1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (1.8V=50mV$_{PP}$, 2.5/3.3V=100mV$_{PP}$) and noise spur amplitude measured. See AN491 for further details.

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Table 9. AC Characteristics (Continued)

(V_{DD} = 1.8 V $\pm$ 5%, 2.5 V $\pm$ 5%, or 3.3 V $\pm$ 10%, T_A = –40 to 85 $^\circ$C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output to Output Skew	T_{SK}	Identical Configuration, Single-ended (Q_N to Q_M)	—	—	100	ps
		Identical Configuration, Differential (Q_N to Q_M)	—	—	50	ps
Part to Part Skew[3]	T_{PS}	Identical configuration	—	50	—	ps
Power Supply Noise Rejection[4]	PSRR	10 kHz sinusoidal noise	—	–90	—	dBc
		100 kHz sinusoidal noise	—	–90	—	dBc
		500 kHz sinusoidal noise	—	–80	—	dBc
		1 MHz sinusoidal noise	—	–70	—	dBc

Notes:
1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (1.8V=50mV$_{PP}$, 2.5/3.3V=100mV$_{PP}$) and noise spur amplitude measured. See AN491 for further details.

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Table 10. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	46.2	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	Still air	27.1	°C/W

Table 11. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	VDD		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	VDD+ 0.3	V
Output Voltage	V_{OUT}		—	—	VDD+ 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	2000	—	—	V
ESD Sensitivity	CDM		500	—	—	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C
Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.						

2. Functional Description

The Si53303 is a low jitter, low skew dual 1:5 differential output buffer. The device has a universal input that accepts most common differential or LVCMOS input signals. Each output bank features control pins to select signal format, output enable, output divider setting and LVCMOS drive strength.

2.1. Universal, Any-Format Input

The Si53303 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 12 and 13 summarize the various input ac- and dc-coupling options supported by the device. Figures 3 and 4 show the recommended input clock termination options.

Table 12. LVPECL, LVCMOS, and LVDS

	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	Yes	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

Table 13. HCSL and CML

	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	No	Yes (3.3 V)	Yes	No
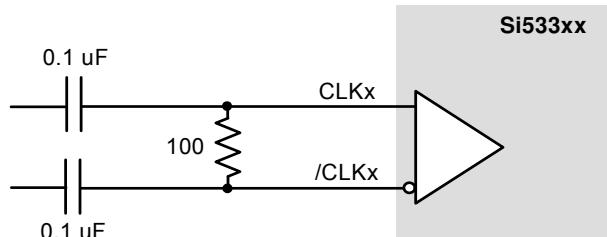
Figure 1. Differential LVPECL, LVDS, CML AC-Coupled Input Termination

Note: V_{DDO} and V_{DD} must be at the same voltage level.
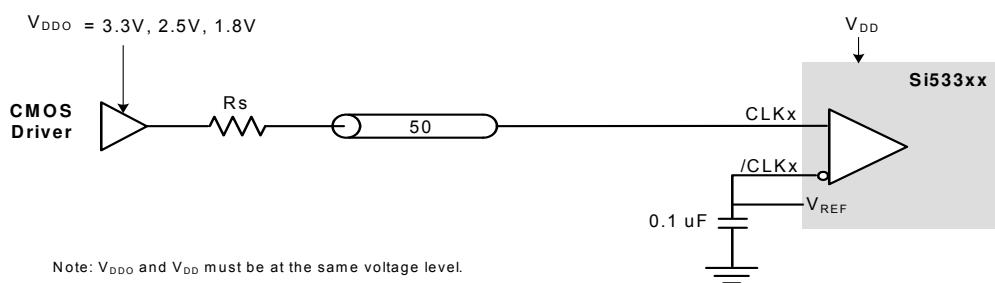
Figure 2. LVCMOS DC-Coupled Input Termination

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DC Coupled LVPECL Termination Scheme 1

V_{DDO} = 3.3V or 2.5V

"Standard" LVPECL Driver

50

50

V_{DDO}

R_1 R_1

V_{DD}

Si533xx

CLKx

/CLKx

R_2 R_2

$V_{TERM} = V_{DDO} - 2V$
$R_1 // R_2 = 50$ Ohm

3.3V LVPECL: R_1 = 127 Ohm, R_2 = 82.5 Ohm
2.5V LVPECL: R_1 = 250 Ohm, R_2 = 62.5 Ohm

DC Coupled LVPECL Termination Scheme 2

V_{DDO} = 3.3V or 2.5V

"Standard" LVPECL Driver

50

50

V_{DD}

Si533xx

CLKx

/CLKx

50   50

$V_{TERM} = V_{DDO} - 2V$

DC Coupled LVDS Termination

V_{DDO} = 3.3V or 2.5V

Standard LVDS Driver

50

50

V_{DD}

Si533xx

CLKx

/CLKx

100
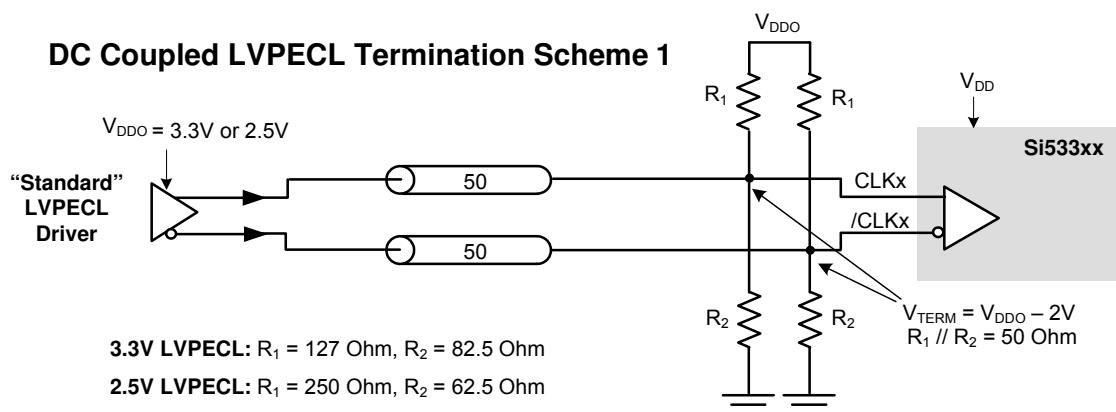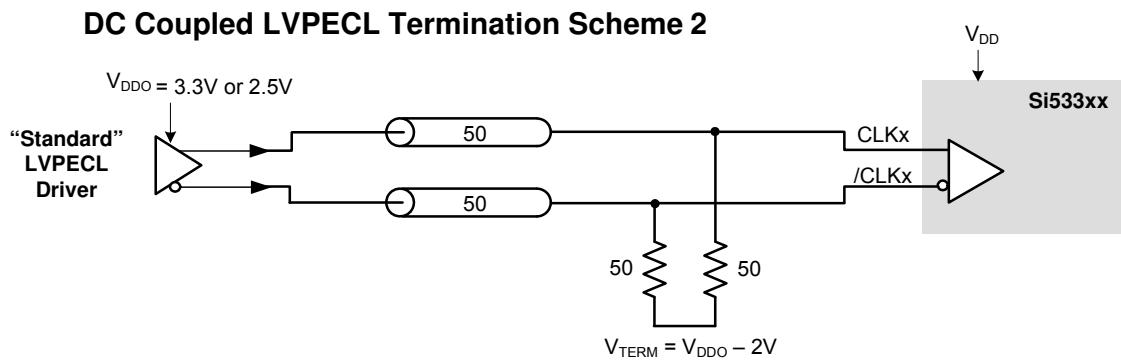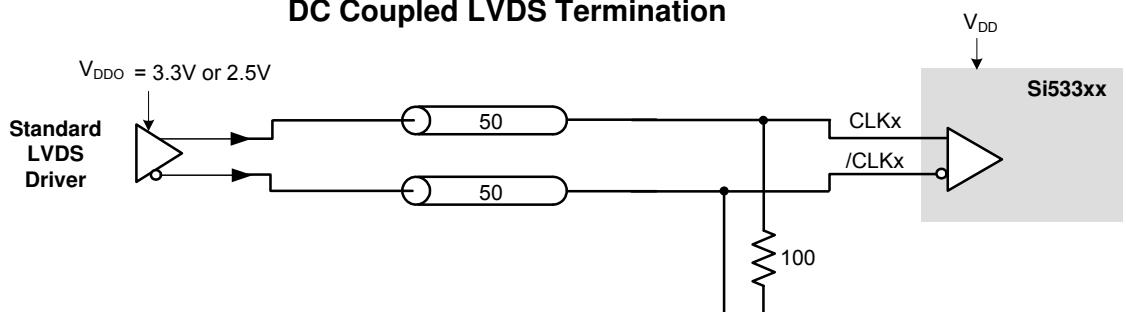
DC Coupled HCSL Termination Scheme

V_{DDO} = 3.3V

Standard HCSL Driver

33

33

50

50

V_{DD}

Si533xx

CLKx

/CLKx

50   50
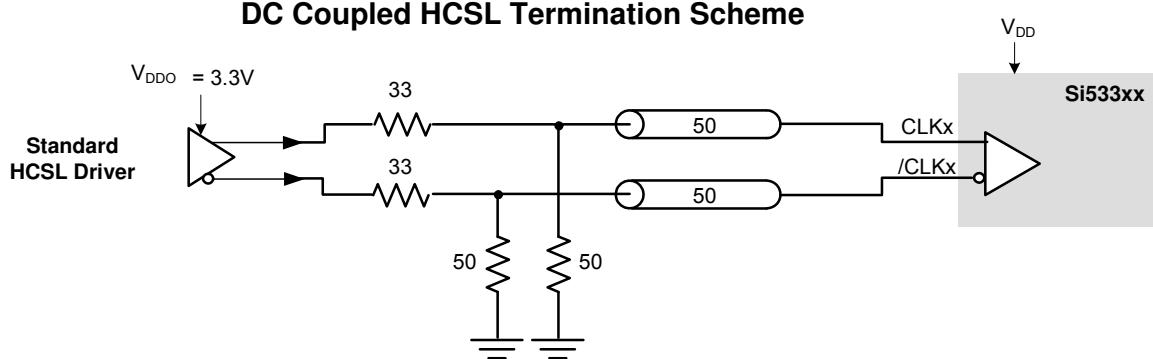
Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 3. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V_{DD}. The inverting input is biased with a 75 kΩ pullup to V_{DD}.

R_{PU} = 75 kohm

R_{PD} = 18.75 kohm
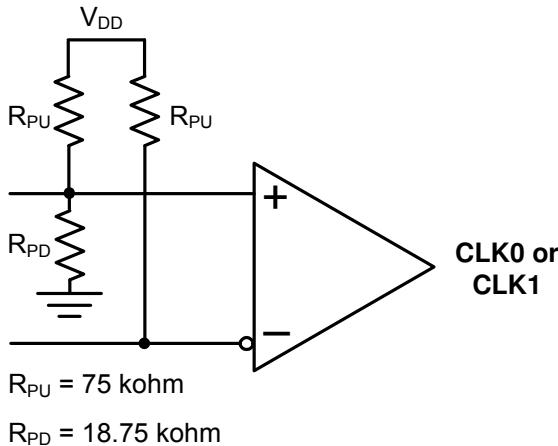
Figure 4. Input Bias Resistors

2.3. Universal, Any-Format Output Buffer

The Si53303 has highly flexible output drivers that support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTA[1] and SFOUTB[1] are 3-level inputs that can be pin-strapped to select the Bank A and Bank B clock signal formats, respectively. This feature enables the device to be used for level translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each V_{DDO} setting.

Table 14. Output Signal Format Selection

SFOUTX[1]	SFOUTX[0]	V_{DDOX} = 3.3 V	V_{DDOX} = 2.5 V	V_{DDOX} = 1.8 V
Open*	Open*	LVPECL	LVPECL	N/A
0	0	LVDS	LVDS	LVDS
0	1	LVCMOS, 24mA drive	LVCMOS, 18mA drive	LVCMOS, 12mA drive
1	0	LVCMOS, 18mA drive	LVCMOS, 12mA drive	LVCMOS, 9mA drive
1	1	LVCMOS, 12mA drive	LVCMOS, 9mA drive	LVCMOS, 6mA drive
Open*	0	LVCMOS, 6mA drive	LVCMOS, 4mA drive	LVCMOS, 2mA drive
Open*	1	LVPECL Low power	LVPECL Low power	N/A
0	Open*	CML	CML	CML
1	Open*	HCSL	HCSL	HCSL
*Note: SFOUTX[1:0] are 3-level input pins. Tie low for "0" setting. Tie high for "1" setting. When left open, the pin floats to V_{DD}/2.				

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2.4. Synchronous Output Enable

The Si53303 features a synchronous output enable (disable) feature. Output enable is sampled and synchronized on the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.
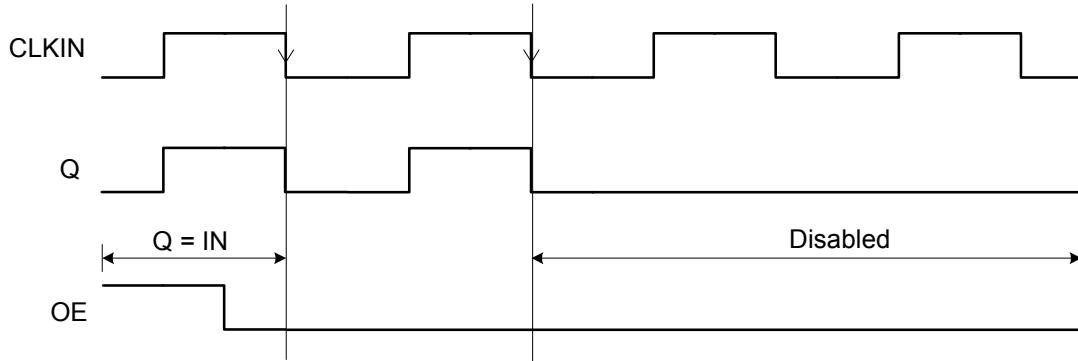
Note 1. Outputs are disabled after 1 to 2 negative edges of the input clock.

Figure 5. Synchronous Output Enable

When OE is low, Q is held low and $\overline{Q}$ is held high for differential output formats. For LVCMOS output format options, both Q and $\overline{Q}$ are held low when OE is set low. The device outputs are enabled when the output enable pin is unconnected.

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2.5. Flexible Output Divider

The Si53303 provides optional clock division in addition to clock distribution. The divider setting for each bank of output clocks is selected via 3-level control pins as shown in the table below. Leaving the DIVX pins open will force a divider value of 1 which is the default mode of operation.

Table 15. Divider Selection

DIVX	Divider Value
Open*	÷1 (default)
0	÷2
1	÷4

*Note: DIVX are 3-level input pins. Tie low for "0" setting. Tie high for "1" setting. When left open, the pin floats to V_{DD}/2.

2.6. Output Enable Logic

Each 1:5 output has an independent clock input (CLK0/CLK1) and an output enable pin. The table below summarizes the input and output clock based upon the state of the input clock and the OE pin.

Table 16. Input Clock and Output Enable Logic

| CLK	OE[1]	Q[2]
L	H	L
H	H	H
X	L	L[3]

Notes:
1. Output enable active high
2. On the next negative transition of CLK0 or CLK1.
3. Single-end: Q=low, $\overline{Q}$=high
   Differential: Q=low, $\overline{Q}$=high

2.7. Power Supply (V$_{DD}$ and V$_{DDO}$X)

The device includes separate core (V$_{DD}$) and output driver supplies (V$_{DDOX}$). This feature allows the core to operate at a lower voltage than V$_{DDO}$, reducing current consumption in mixed supply applications. The core V$_{DD}$ supports 3.3V, 2.5V, or 1.8V. Each output bank has its own V$_{DDOX}$ supply, supporting 3.3V, 2.5V, or 1.8V.

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2.8. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused output clocks should be left floating.
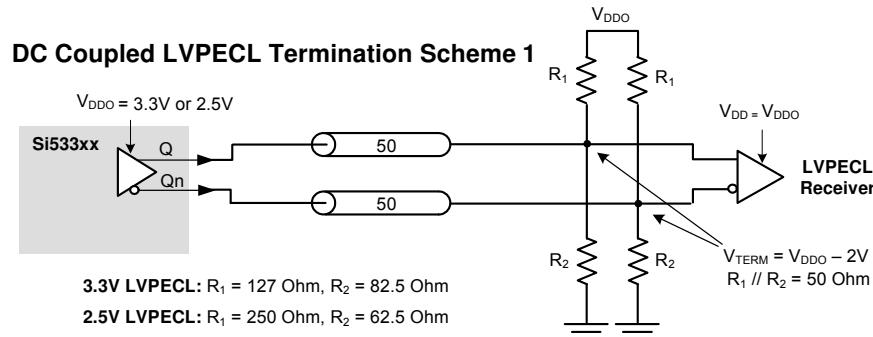
DC Coupled LVPECL Termination Scheme 1

3.3V LVPECL: R_1 = 127 Ohm, R_2 = 82.5 Ohm
2.5V LVPECL: R_1 = 250 Ohm, R_2 = 62.5 Ohm

V_{DDO} = 3.3V or 2.5V

$V_{DD} = V_{DDO}$

$V_{TERM} = V_{DDO} - 2V$
$R_1 // R_2$ = 50 Ohm

DC Coupled LVPECL Termination Scheme 2

V_{DDO} = 3.3V or 2.5V

$V_{DD} = V_{DDO}$

$V_{TERM} = V_{DDO} - 2V$

AC Coupled LVPECL Termination Scheme 1

3.3V LVPECL: R_1 = 82.5 Ohm, R_2 = 127 Ohm, Rb = 120 Ohm
2.5V LVPECL: R_1 = 62.5 Ohm, R_2 = 250 Ohm, Rb = 90 Ohm

V_{DDO} = 3.3V or 2.5V

V_{DD} = 3.3V or 2.5V

$V_{BIAS} = V_{DD} - 1.3V$
$R_1 // R_2$ = 50 Ohm
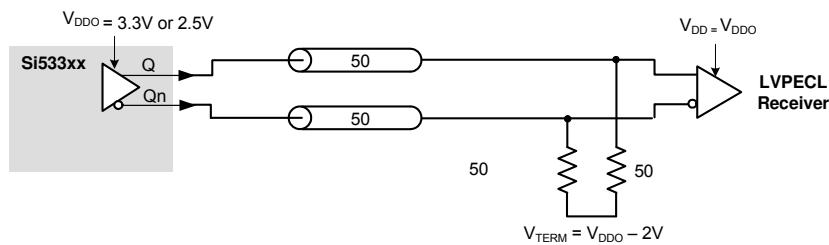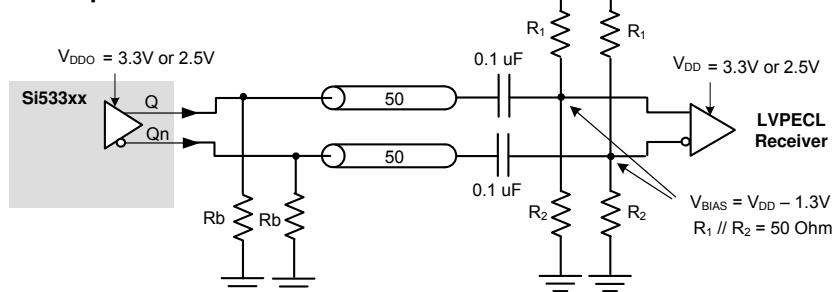
AC Coupled LVPECL Termination Scheme 2
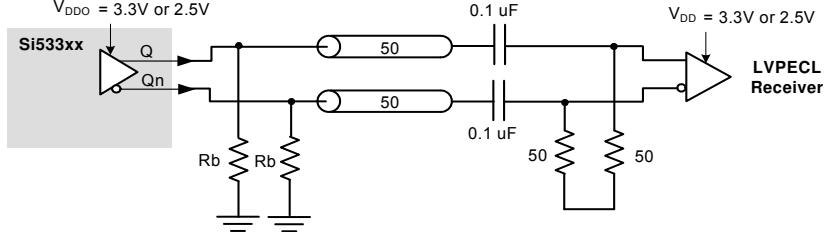
3.3V LVPECL: Rb = 120 Ohm
2.5V LVPECL: Rb = 90 Ohm

V_{DDO} = 3.3V or 2.5V

V_{DD} = 3.3V or 2.5V

Figure 6. LVPECL Output Termination

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DC Coupled LVDS and Low-Power LVPECL Termination

V_{DDO}= 3.3 or 2.5V or 1.8V

V_{DD}

Si533xx

Q
Qn

50

50

100

LVDS
Receiver

AC Coupled LVDS Termination

V_{DDO} = 3.3V or 2.5V or 1.8V

V_{DD}

Si533xx

Q
Qn

50

50

0.1 uF

0.1 uF

50

50
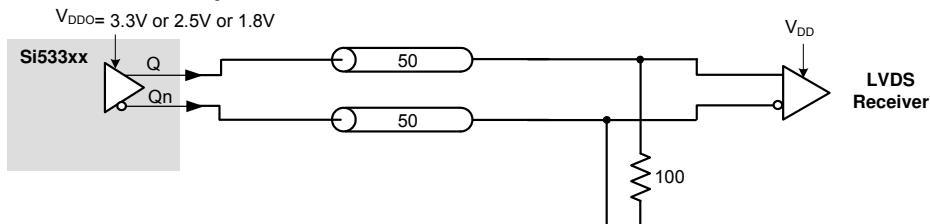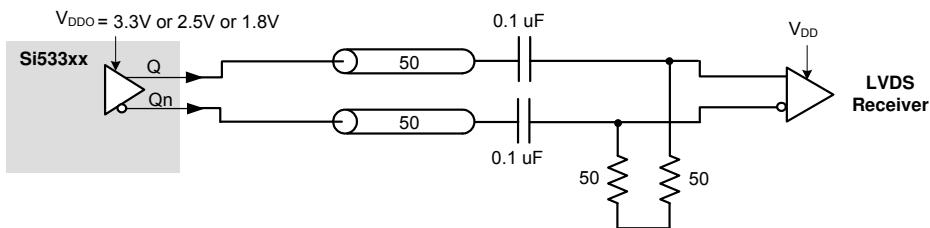
LVDS
Receiver

AC Coupled CML Termination

V_{DDO} = 3.3V or 2.5V or 1.8V

V_{DD}

Si533xx

Q
Qn

50

50

0.1 uF

0.1 uF

100

CML
Receiver
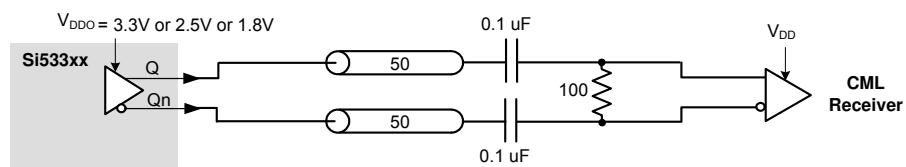
DC Coupled HCSL Receiver Termination

V_{DDO} = 3.3V

V_{DD}

Si533xx

Q
Qn

50

50

50

50

Standard
HCSL
Receiver
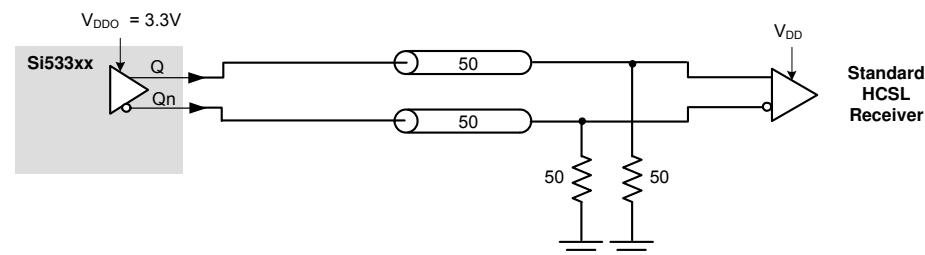
DC Coupled HCSL Source Termination

V_{DDO} = 3.3V

V_{DD}

Si533xx

Q
Qn

42.2

42.2

50

50

86.6

86.6

Standard
HCSL
Receiver
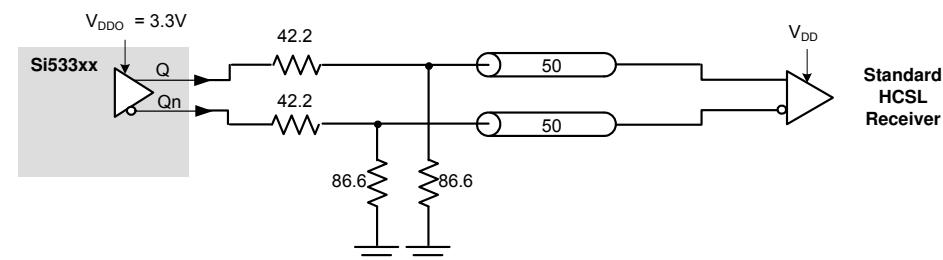
**Figure 7. LVDS, CML, and HCSL Output Termination**

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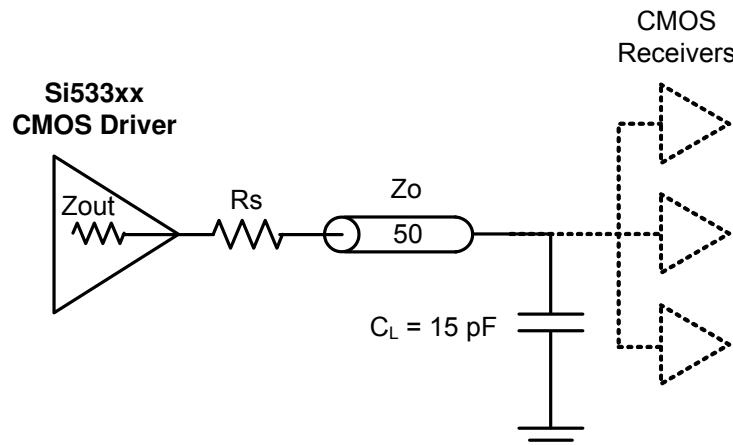
Figure 8. LVCMOS Output Termination

Table 17. Recommended LVCMOS R$_S$ Series Termination

SFOUTX[1]	SFOUTX[0]	R$_S$ (ohms)		
		3.3V	2.5V	1.8V
0	1	33	33	33
1	0	33	33	33
1	1	0	0	0
Open	0	0	0	0

2.9. AC Timing Waveforms
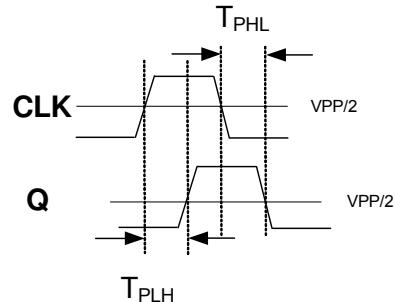

Propagation Delay
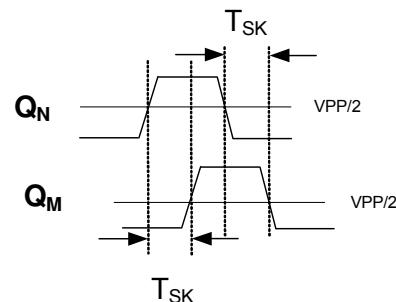
Output-Output Skew
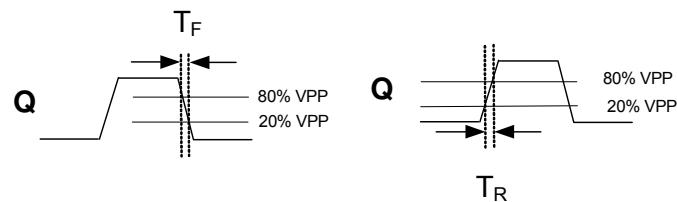
Rise/Fall Time

Figure 9. AC Waveforms

2.10. Typical Phase Noise Performance
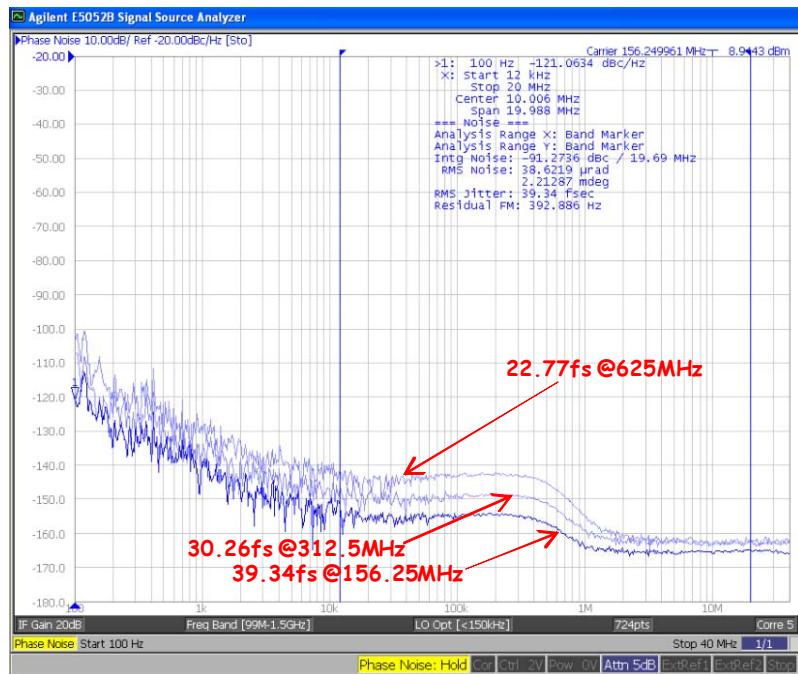
Source Jitter
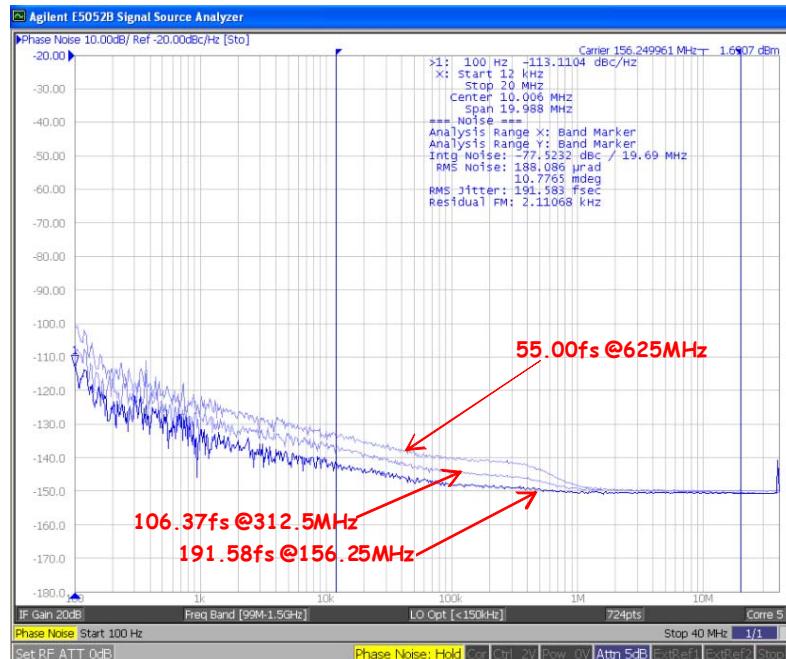

Total Jitter

Figure 10. Si53303 Phase Noise

Note: Measured single-endedly.

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Table 18. Si53303 Additive Jitter

Frequency (MHz)	Source Jitter (fs)	Total Jitter (fs)	Additive Jitter (fs)
156.25	39.34	191.58	187.50
312.5	30.26	106.37	101.98
625	22.77	55.00	50.07

2.11. Input Noise Isolation
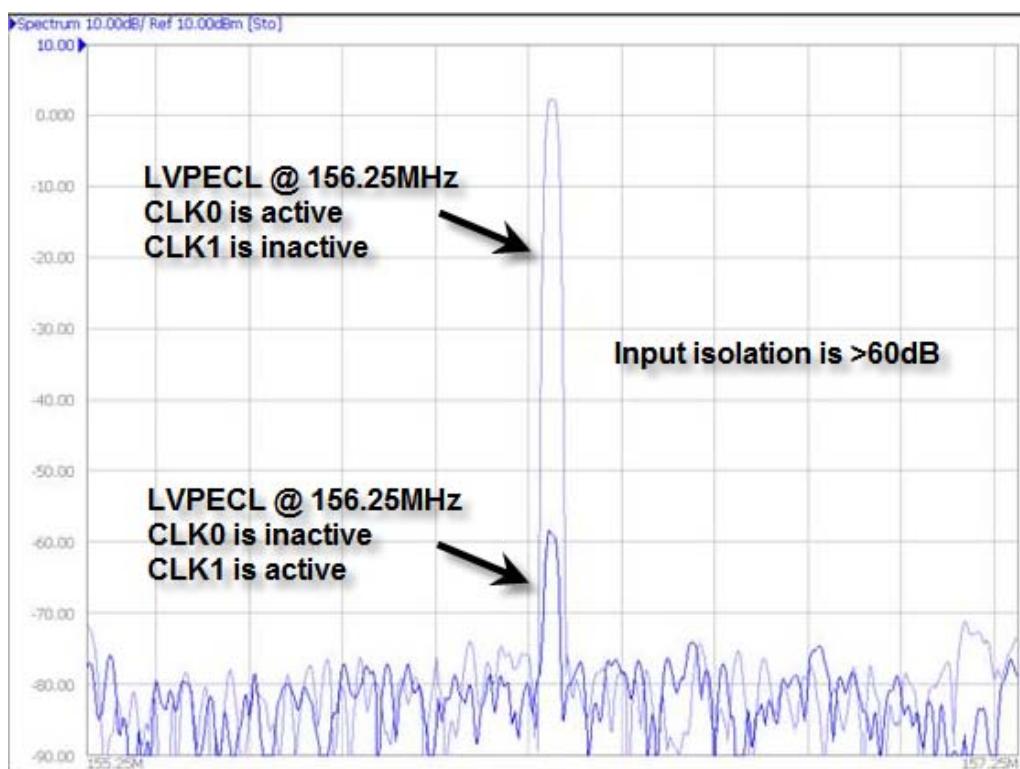
Figure 11. Input Noise Isolation

2.12. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see AN491: Power Supply Rejection for Low Jitter Clocks.
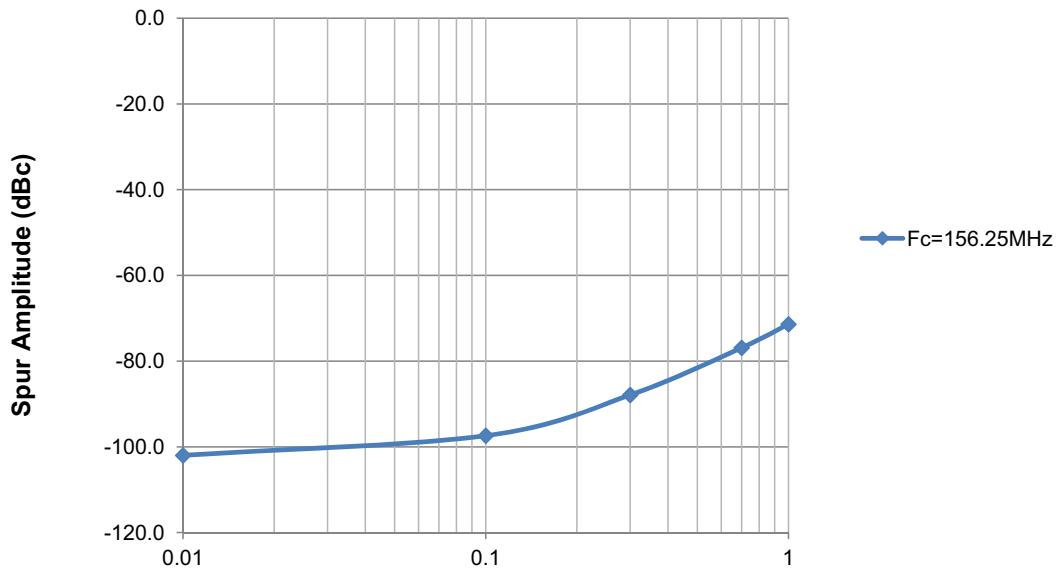

Figure 12. Power Supply Noise Rejection (100 mVpp Sinusoidal Power Supply Noise Applied)

3. Pin Description: 44-Pin QFN
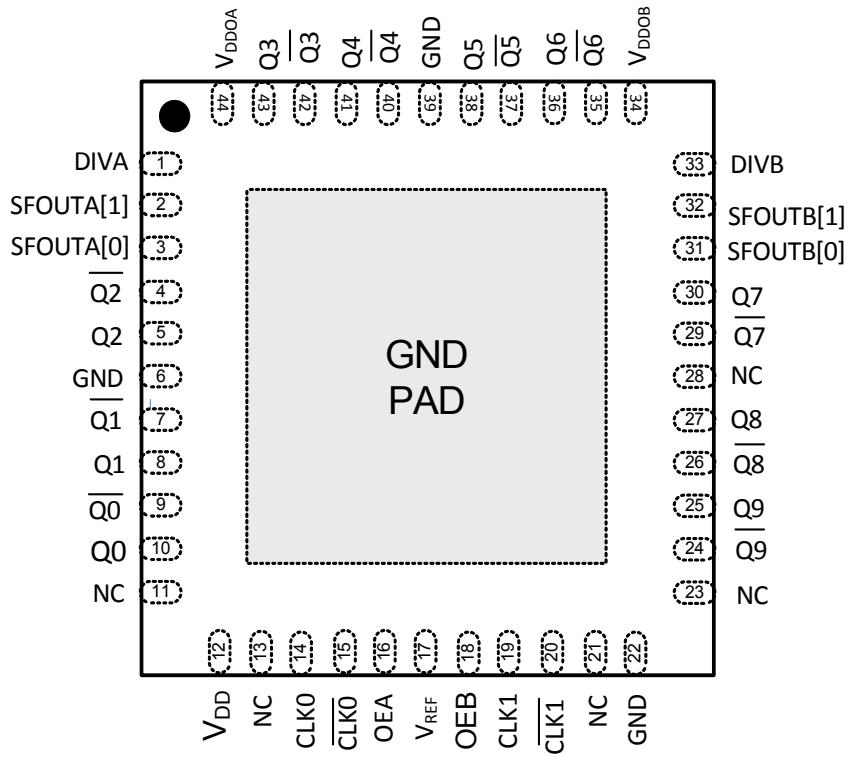
Table 19. Pin Description

Pin #	Name	Description
1	DIVA	Output divider control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V_{DD}.
2	SFOUTA[1]	Output signal format control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V_{DD}.
3	SFOUTA[0]	Output signal format control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V_{DD}.
4	$\overline{Q2}$	Output clock 2 (complement)
5	Q2	Output clock 2
6	GND	Ground
7	$\overline{Q1}$	Output clock 1 (complement)
8	Q1	Output clock 1

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Table 19. Pin Description (Continued)

Pin #	Name	Description
9	$\overline{Q0}$	Output clock 0 (complement)
10	Q0	Output clock 0
11	NC	No connect
12	VDD	Core voltage supply Bypass with 1.0 µF capacitor and place close to the VDD pin as possible
13	NC	No connect
14	CLK0	Input clock 0
15	$\overline{CLK0}$	Input clock 0 (complement) When CLK0 is driven by a single-end input, connect V_{REF} to $\overline{CLK0}$ $\overline{CLK0}$ contains an internal pull-up resistor
16	OEA	Output enable—Bank A When OE = high, the Bank A outputs are enabled When OE = low, Q is held low and $\overline{Q}$ is held high for differential formats For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low OEA contains an internal pull-up resistor
17	V_{REF}	Input reference voltage When driven by a LVCMOS clock input, connect the unused clock input to V_{REF} and a 0.1µF cap to ground. When driven by a differential clock, do not connect the V_{REF} pin.
18	OEB	Output enable—Bank B When OE = high, the Bank B outputs are enabled When OE = low, Q is held low and $\overline{Q}$ is held high for differential formats For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low OEB contains an internal pull-up resistor.
19	CLK1	Input clock 1
20	$\overline{CLK1}$	Input clock 1 (complement) When CLK1 is driven by a single-end input, connect V_{REF} to $\overline{CLK1}$ $\overline{CLK1}$ contains an internal pull-up resistor
21	NC	No connect
22	GND	Ground
23	NC	No connect
24	$\overline{Q9}$	Output clock 9 (complement)
25	Q9	Output clock 9
26	$\overline{Q8}$	Output clock 8 (complement)
27	Q8	Output clock 8
28	NC	No connect

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Table 19. Pin Description (Continued)

Pin #	Name	Description
29	$\overline{Q7}$	Output clock 7 (complement)
30	Q7	Output clock 7
31	SFOUTB[0]	Output signal format control pin for Bank B Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V_{DD}.
32	SFOUTB[1]	Output signal format control pin for Bank B Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V_{DD}.
33	DIVB	Output divider configuration bit for Bank B Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V_{DD}.
34	V_{DDOB}	Output Clock Voltage Supply—Bank B (Outputs: Q5 to Q9) Bypass with 1.0 µF capacitor and place close to the V_{DDOB} pin as possible
35	$\overline{Q6}$	Output clock 6 (complement)
36	Q6	Output clock 6
37	$\overline{Q5}$	Output clock 5 (complement)
38	Q5	Output clock 5.
39	GND	Ground.
40	$\overline{Q4}$	Output clock 4 (complement)
41	Q4	Output clock 4.
42	$\overline{Q3}$	Output clock 3 (complement)
43	Q3	Output clock 3
44	V_{DDOA}	Output Voltage Supply—Bank A (Outputs: Q0 to Q4) Bypass with 1.0 µF capacitor and place close to the V_{DDOA} pin as possible
GND Pad	GND	Ground Pad Power supply ground and thermal relief

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4. Ordering Guide

Part Number	Package	PB-Free, ROHS-6	Temperature
Si53303-B-GM	44-QFN	Yes	–40 to 85 °C

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