Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

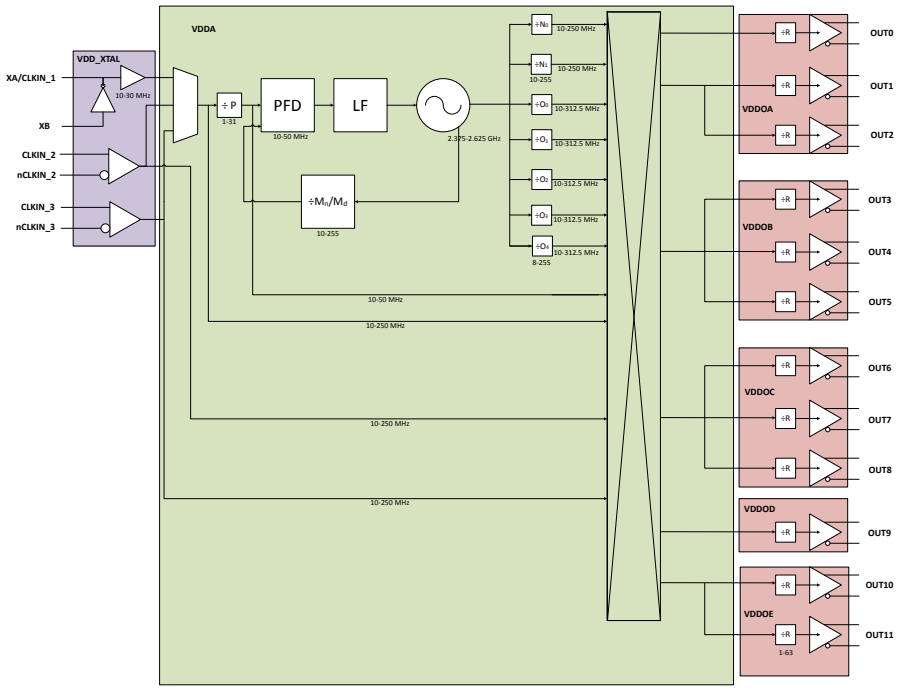
We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Si5332 Reference Manual

The Si5332 is a high-performance, low-jitter clock generator capable of synthesizing five independent banks of user-programmable clock frequencies up to 333.33 MHz, while providing up to 12 differential or 24 single-ended output clocks. The Si5332 supports free run operation using an external crystal, or optional internal crystal, as well as lock to an external clock signal. The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, and LVCMOS. Separate output supply pins allow supply voltages of 3.3, 2.5, 1.8 V and 1.5V (CMOS only) to power the multi-format output drivers. The core voltage supply (VDD) accepts 3.3, 2.5, or 1.8 V and is independent from the output supplies (VDDOs). Using its two-stage synthesis architecture and patented high-resolution Multisynth technology, the Si5332 can generate three fully independent / non-harmonically-related bank frequencies from a single input frequency.



KEY FEATURES

- Any-Frequency 6/8/12-output programmable clock generators
- Offered in three different package sizes, supporting different combinations of output clocks and user configurable hardware input pins
  - 32-pin QFN, up to 6 outputs
  - 40-pin QFN, up to 8 outputs
  - 48-pin QFN, up to 12 outputs
- Multisynth technology enables any frequency synthesis on any output up to 250 MHz
- Highly configurable output path featuring a cross point mux
- Up to three independent fractional synthesis output paths
- Up to five independent integer dividers
- Down and center spread spectrum
- Embedded 50 MHz crystal option
- Input frequency range:
  - External crystal: 16 to 50 MHz
  - Embedded crystal: 50 MHz
  - Differential clock: 10 to 250 MHz
  - LVCMOS clock: 10 to 170 MHz
- Output frequency range:
  - Differential: 5 to 312.5 MHz
  - LVCMOS: 5 to 170 MHz
- User-configurable clock output signal format per output: LVDS, LVPECL, HCSL, LVCMOS
- Easy device configuration using our ClockBuilder Pro™ (CBPro) software tool available for download from our web site
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant
- For more information, refer to the Si5332 data sheet

Table of Contents

1. Overview

In addition to clock generation, the input clocks can bypass the synthesis stage enabling the Si5332 to be used as a high-performance clock buffer or a combination of a buffer and generator. The Multisynth dividers have two sets of divide ratio registers, an A set and a B set. The active in-use divide ratio can be switched between the A set or B set via external input pin or register control. This feature allows for dynamic frequency shifting at ppb accuracy for applications such as frequency margining. Similar A set and B set divider ratios are available for the integer dividers, but the ratios must be integer related. CBPro supports use of A and B divider sets. Spread spectrum is available for any clock output from two Multisynth dividers for use in EMI-sensitive applications, such as PCI Express. Configurations and controls of the Si5332 are mainly handled through I2C. Any GPI pin can be programmed to be clock input select, frequency A/B select, spread enable, output enable, or I2C address select.

2. Power Supply Sequencing

The Si5332 VDD_core voltages are VDD_DIG, VDD_XTAL and VDDA. These 3 VDD_core pins must all use the *same* voltage. Power supply sequencing between VDD_core and any VDDOx pin is allowed in any order. However, to minimize the “bring up” time, it is recommended that VDD_core is powered up first, this ensures that the NVM download is completed first. It is estimated that the total device “bring up” time will be ~50 ms. When VDD_core is powered up, the I2C master can communicate with the Si5332 slave. The register bit field “VDD_XTAL_OK” is set to indicate input buffer(s) and crystal oscillator are powered up. Once the appropriate VDDOx supplies are powered-up, the VDDO_OK register field will indicate output driver bank supply voltage status. These status registers are available to provide an indication of general device status and presence of output driver voltages. The figure below shows the Si5332 device power-up sequencing and expected device behavior. Note that a blank (unconfigured) part will stop and wait to be configured with outputs disabled.

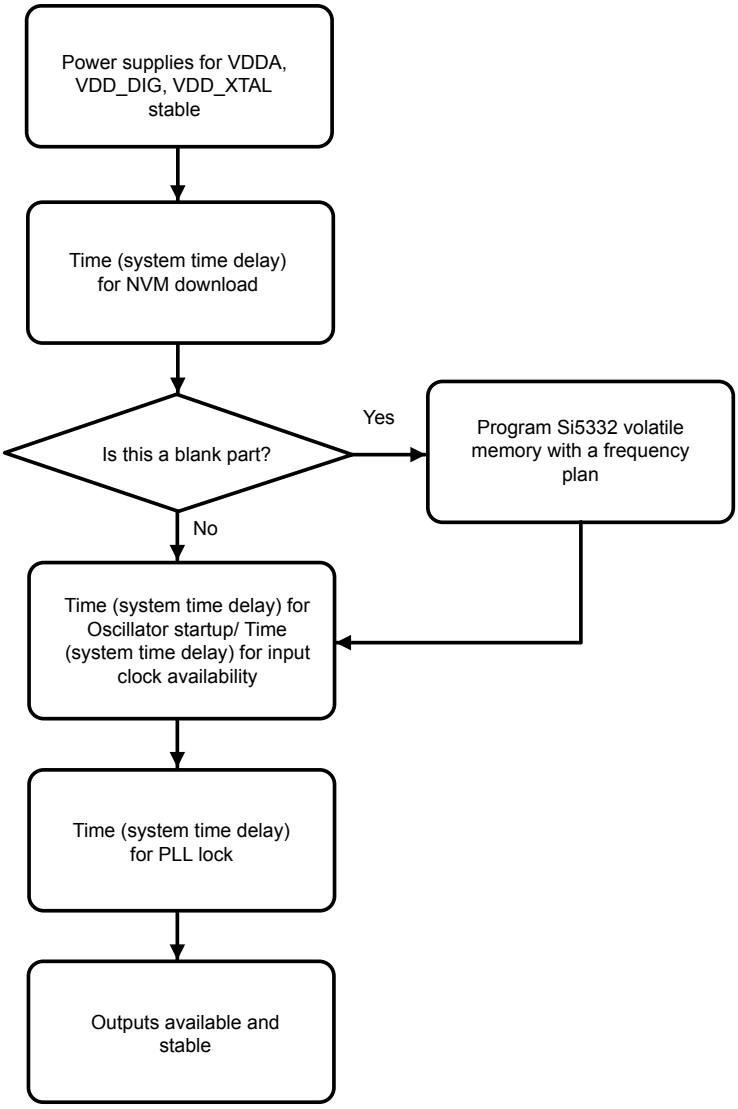


Figure 2.1. Power Supply Sequencing for Si5332

3. Input Clocks

The Si5332 has three input clock nodes, the XA/XB pair, the CLKIN_2/CLKIN_2# pair and the CLKIN_3/CLKIN_3# pair.

XA/XB supports a crystal input or an external clock input whereas the CLKIN_x/CLKIN_x# pairs support ONLY external clock inputs. The GPI pins can be set to select the active input clock for the PLL (or the user can set the active input via register writes).

3.1 Input Clock Terminations

Supported input clock sources for the Si5332 are:

1. External crystal attached to the Si5332 XA/XB inputs (Si5332A/B/C/D only).
2. Internal crystal (Si5332E/F/G/H only).
3. External single-ended clock attached to XA (Si5332A/B/C/D only).
4. Externally supplied clock attached to available CLKIN_x/CLKINx# inputs.

3.1.1 External Crystal (Si5332A/B/C/D)

An external crystal can be connected to a Si5332A/B/C/D device's XA/XB inputs as shown below. See section 3.2 for a list of recommended crystals, or see Table 5.4 in the Si5332 datasheet for crystal specifications when selecting a different crystal. Note the external crystal specifications in Si5332 datasheet Table 5.4 must be met.

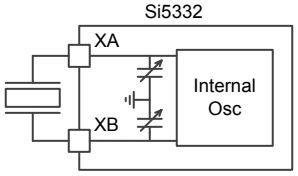


Figure 3.1. External Crystal Connection

3.1.2 Internal Crystal (Si5332E/F/G/H)

An internal crystal option is available by selecting the E, F, G, or H variant of the Si5332. The internal crystal is a fixed 50 MHz crystal. No external crystal or other components should be connected to the XA/XB pins and the pins should not have signals routed next to or underneath. For layout purposes, the XA/XB pins should be treated as if the crystal is attached.

3.1.3 External Input Clock on XA Input (Si5332A/B/C/D)

The XA input can accept an externally supplied, AC coupled clock with maximum voltage swing of 1Vpp. See figure below for connection details. The XB pin must be left open with nothing connected. If using this input clock mode, it is suggested to zero-out the internal crystal loading capacitance (CL) for best operation.

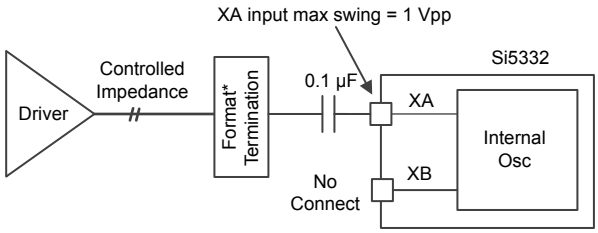


Figure 3.2. External Input Clock on XA Input

3.1.4 External Input Clock on CLKIN_x/CLKIN_x#

When supplying clocks into the CLKINx inputs, AC coupling is the preferred method for both differential and single-ended clocks with DC coupling an option in certain configurations.

The figures below show how to connect either a differential or single-ended input clock to the Si5332 clock inputs.

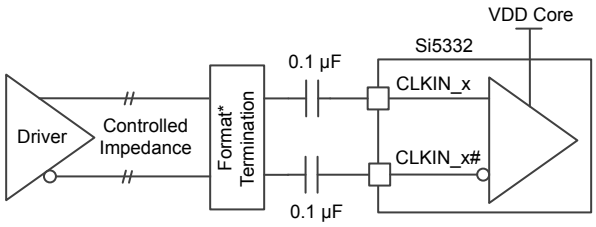


Figure 3.3. AC-coupled Differential Input Clock (LVDS, LVPECL, HCSL, CML, etc.)

For AC-coupled differential input clocks the Vswing of the clock must be limited to the maximum VDD_Core voltage. VDD_Core is defined as the following group of VDD supply pins: VDD_DIG, VDDA, and VDD_XTAL. (Format Termination: Input clock format termination is dependent on the driver format used and is usually specified by the driving device and/or industry standard clock format specification. The CLKIN inputs of Si5332 are high impedance inputs.)

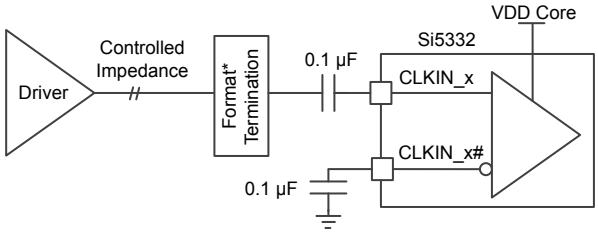


Figure 3.4. AC-coupled Single-ended Input Clock (LVCMOS)

For AC-coupled single-ended input clocks the Vswing of the clock must be limited to the maximum VDD_Core voltage. VDD_Core is defined as the following group of VDD supply pins: VDD_DIG, VDDA, and VDD_XTAL. (Format Termination: Input clock format termination is dependent on the driver format used and is usually specified by the driving device and/or industry standard clock format specification. The CLKIN inputs of Si5332 are high impedance inputs.)

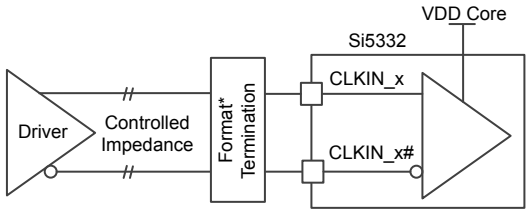


Figure 3.5. DC-coupled Differential Input Clock

For DC-coupled differential input clocks, refer to Table 3.1 Input Clock Coupling Restrictions on page 7 to determine if DC coupling is supported. (Format Termination: Input clock format termination is dependent on the driver format used and is usually specified by the driving device and/or industry standard clock format specification. The CLKIN inputs of Si5332 are high impedance inputs.)

Table 3.1. Si5332 Input Clock Coupling Restrictions (AC or DC)

Format	VDD_Core		
	3.3 V	2.5 V	1.8 V
LVDS 3.3 V/2.5 V	AC or DC	AC only	AC only
LVDS 1.8 V	AC or DC	AC only	AC only
LVPECL 3.3 V/2.5 V	AC or DC	AC only	AC only
HCSL	AC or DC	AC or DC	AC only
CML	AC only	AC only	AC only
LVCMOS	AC only	AC only	AC only

Note:

1. For DC-coupled, input clock peak voltage must not exceed VDD_Core and minimum voltage must not be below GND.
2. For AC-coupled, peak swing must not exceed VDD_Core.

3.2 Crystal Recommendations

The crystals in the table below are recommended for use with Si5332. The crystals listed are 25 and 27 MHz frequencies. However, when choosing any crystal frequency between 16-30 MHz, a crystal with with ESR less than (or equal to) 50 Ω and CL less than (or equal to) 20 pF can be used with Si5332. When choosing crystals of 31-50 MHz frequencies, C0 should not exceed 2 pF, CL should not exceed 10 pF and the ESR should not exceed 50 Ω.

Table 3.2. Recommended Crystals

Crystal Part Number	Make	Stability	CL	ESR
ECS-25-18-30B-AKN	ECS	30ppm	18pf	30 Ω
ECS-27-18-30B-AKN		30ppm	18pf	30 Ω
FOXSDLF/250FR-20	Fox	30ppm	20pf	30 Ω
FA-238V-25.000000MHz12.0+15.0-15.0	Epson	50ppm	12pf	50 Ω
ABM3B-25.000MHz-18-50-D1U	Abracon	20ppm	18pf	50 Ω
ABM3B-27.000MHz-18-50-D1U		20ppm	18pf	50 Ω
ABM3B-25.000MHz-18-60-D1U		30ppm	18pf	60 Ω
ABM3B-27.000MHz-18-60-D1U		30ppm	18pf	60 Ω
ABM3B-25.000MHz-12-50-D1U		10ppm	10pf	50 Ω
ABM3B-27.000MHz-12-50-D1U		10ppm	10pf	50 Ω
AA-25.000MALE-T	TXC	30ppm	12pf	50 Ω
AA-27.000MAGK-T		30ppm	20pf	50 Ω
FQ5032B-25.000	Fox	30ppm	20pf	50 Ω
FQ5032B-27.000				
NX5032GA-25.000M-STD-CSK-4	NDK	30ppm	8pf	50 Ω
NX5032GA-25.000000MHZ-LN-CD-1		30ppm	8pf	70 Ω
NX5032GA-27M-STD-CSK-4		30ppm	8pf	50 Ω
NX5032GA-27.000000MHZ-LN-CD-1		30ppm	8pf	70 Ω
7A-25.000MAAE	TXC	30ppm	12pf	50 Ω
7A-25.000MAAJ		30ppm	18pf	50 Ω
7A-27.000MAAE		30ppm	12pf	50 Ω
7A-27.000MAAJ		30ppm	18pf	50 Ω

Crystals will resonate at their specified frequency (i.e., be “on-frequency”) if the capacitive loading across the crystal’s terminals is the same as specified by the crystal loading capacitance (CL) specification. The total loading capacitance presented to the crystal must factor in all capacitance sources such as parasitic “stray” capacitance as well as added loading capacitance. Stray capacitance comes from sources like PCB traces, capacitive coupling to nearby components, as well as any stray capacitance within the oscillator device itself. For “on-frequency” oscillator operation, all capacitance sources must be considered to determine the correct total capacitance presented to the crystal to match it’s required CL.

The Si5332 contains variable *internal* loading capacitors (CLVAR) to provide any necessary added crystal matching capacitance so external matching capacitors are not needed. The figure below shows the Si5332’s internal variable capacitance and the two sources of stray loading capacitance.

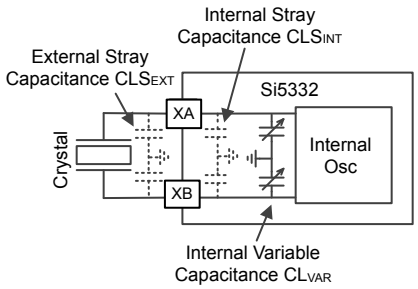


Figure 3.6. Sources of Crystal Loading Capacitance

Using the Si5332’s internal variable loading capacitors (CL_{VAR}), the crystal’s required CL can be matched by adding capacitance to the external stray and internal device capacitance. The total stray capacitance must be less than the required crystal loading capacitance CL. A value for CL_{VAR} must be selected such that:

$$Crystal\ \mathrm{CL} = CL_{VAR} + CLS_{INT} + CLS_{EXT}$$

Or rearranged:

$$CL_{VAR} = CrystalCL - CLS_{INT} - CLS_{EXT}$$

Equation 1.

The crystal CL value is specified by the choice of crystal. A list of Si5332 recommended crystals can be found in Table 3.2 on page 8 of this document. For the following example, a Crystal CL value of 10 pf will be used.

The internal stray capacitance (CLS_{INT}) of the Si5332 is 2.4 pf. External PCB stray capacitance (CLS_{EXT}) is usually in the order of 2-3 pf given a reasonably compact layout. The Si5332 EVB external stray capacitance is ~ 2.75 pf. Given these example values, the required CL_{VAR} can be calculated as shown below, using Equation 1.

$$CL_{VAR} = 10pF - 2.4pF - 2.75pF = 4.85pF$$

Equation 2.

Note the internal variable capacitor, CL_{VAR} , consists of two capacitors **in series**: one connected to the XA pin (CL_{XA}) and one to the XB pin (CL_{XB}) of the Si5332. For capacitors in series, if we keep CL_{XA} = CL_{XB}, we can simply double the value of CL_{VAR} to arrive at the correct CL_{XA} and CL_{XB} value.

$$CL_{XA} = CL_{XB} = \left(2 \times CL_{VAR}\right) = 2 \times 4.85pF = 9.7pF$$

Equation 3.

Combining Equation 1 and Equation 2 will solve for CL_{XA}/CL_{XB} in single equation form:

$$CL_{XA} = CL_{XB} = 2 \times \left(CrystalCL - CL_{int} - CL_{ext}\right)$$

Equation 4.

Note: Valid range for CL_{XA} and CL_{XB} in Si5332 is 0 to 38.395 pF

CL_{XA} and CL_{XB} may only be a positive value and in the range of 0 to 38.395 pF. Any values less than 0 cannot be implemented and any values greater than 38.395 pF cannot be implemented using internal capacitors alone. (Note that the above range is **NOT** simply the crystal CL spec because both external and internal stray capacitance play a role in determining valid CL_{XA}/CL_{XB}.)

Once CL_{XA} and CL_{XB} have been determined using Equation 4, use the following set of formulas to calculate the required register values to implement the desired CL_{XA}/CL_{XB}.

If ($CL_{XA/XB} \leq 30.555$ pF, then:

- xosc_cint_ena = 0
- xosc_ctrim_xin = Round to nearest integer (CL_{XA} / 0.485)
- xosc_ctrim_xout = Round to nearest integer (CL_{XB} / 0.485)

If (30.555 pF < $CL_{XA/XB} \leq 38.395$ pF, then:

- xosc_cint_ena = 1
- xosc_ctrim_xin = Round to nearest integer ((CL_{XA} - 7.84) / 0.485)
- xosc_ctrim_xout = Round to nearest integer (CL_{XB} - 7.84) / 0.485)

To summarize, use Equation 4 to calculate CL_{XA}/CL_{XB}, then use the above set of formulas to calculate register values to implement CL_{XA}/CL_{XB} in the Si5332.

Note: Your unique PCB assembly's stray capacitance value plays a role in determining correct internal capacitor settings and, consequently, the crystal's frequency of oscillation. Small differences in actual board stray capacitance values from the value used in the above calculations will result in the crystal oscillating slightly off-frequency. Significant capacitance differences can result in significant frequency error.

4. GPI

The General-purpose inputs (GPI pins) are pins whose input functions can be programmed (in NVM) to assume a pre-defined function. The Si5332 provides users the following options for each GPI pin available for programming.

A general-purpose input can be programed as one of the following pins:

Table 4.1. GPI Programming Guide

Function Name	Description
OE_0	Output enable input for OUT0
OE_1	Output enable input for OUT1
OE_2	Output enable input for OUT2
OE_3	Output enable input for OUT3
OE_4	Output enable input for OUT4
OE_5	Output enable input for OUT5
OE_6	Output enable input for OUT6
OE_7	Output enable input for OUT7
OE_8	Output enable input for OUT8
OE_9	Output enable input for OUT9
OE_10	Output enable input for OUT10
OE_11	Output enable input for OUT11
SSE_0	Spread spectrum control for outputs derived from N0
SSE_1	Spread spectrum control for outputs derived from N1
FS_N0	Frequency select for outputs derived from N0
FS_N1	Frequency select for outputs derived from N1
FS_O0	Frequency select for outputs derived from O0
FS_O1	Frequency select for outputs derived from O1
FS_O2	Frequency select for outputs derived from O2
FS_O3	Frequency select for outputs derived from O3
FS_O4	Frequency select for outputs derived from O4
CLKIN_SEL0	Input clock select (LSB)
CLKIN_SEL1	Input clock select (MSB)
I2C_ADDR	Selection control for i2c address

ClockBuilder Pro will allow a user to select similar functions to choose a single GPIO input. For instance, FS_x functions will be allowed to share a single GPIO pin but a FS_x function and OE_y function will not be allowed to share a single GPIO input.

The default I2C address for Si5332 is 6Ah. This I2C address can be customized and the user can select between “two” different I2C addresses using the I2C_ADDR function.

GPI pin functionality is only available when creating customized Si5332 configuration files and part numbers through ClockBuilder Pro. GPI function assignment and definition is not available through I^2C programming, meaning GPI pin use is not available in base parts.

5. Output Clock Terminations

The Si5332 output formats are programable and cover all popular output formats. The output drivers can be set by the programming the following bit fields:

Table 5.1. Output Format Related Register Fields

`outx_mode`: - Sets the mode of the driver.
`outx_cmos_inv`: - Sets an inverted copy for CMOS driver format.
`outx_cmos_slew`: - Sets the slew rate of the CMOS driver.
`outx_cmos_str`: - Sets the output impedance of the CMOS driver.

Table 5.2. OUTx_Mode vs Output Formats

OUTx_MODE	Driver Mode
0	off
1	CMOS on positive output only
2	CMOS on negative output only
3	dual CMOS outputs
4	2.5V/3.3V LVDS
5	1.8V LVDS
6	2.5V/3.3V LVDS fast
7	1.8V LVDS fast
8	HCSL 50 Ω (external termination)
9	HCSL 50 Ω (internal termination)
10	HCSL 42.5 Ω (external termination)
11	HCSL 42.5 Ω (internal termination)
12	LVPECL
13	Reserved
14	Reserved
15	Reserved

The recommended termination for each output format is shown in these figures: Figure 5.1 LVCMOS Termination, Option 1 on page 13 and Figure 5.2 LVCMOS Termination, Option 2 on page 13.

5.1 DC-Coupled Output Clock Terminations

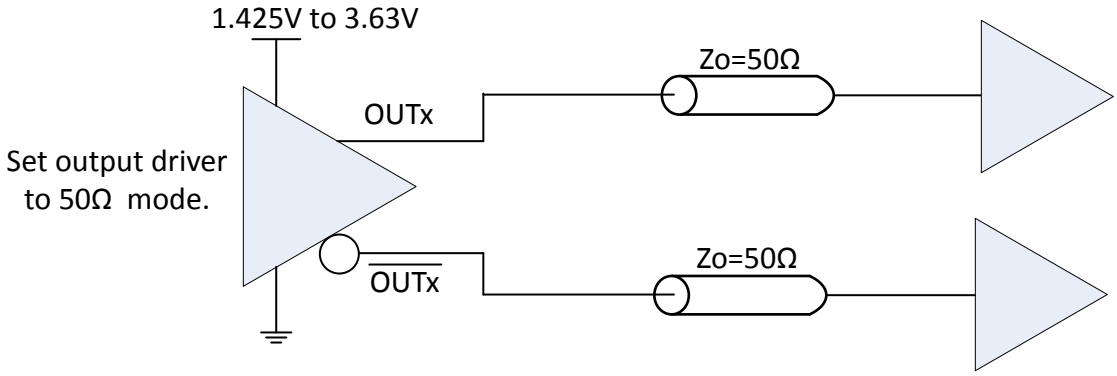


Figure 5.1. LVCMOS Termination, Option 1

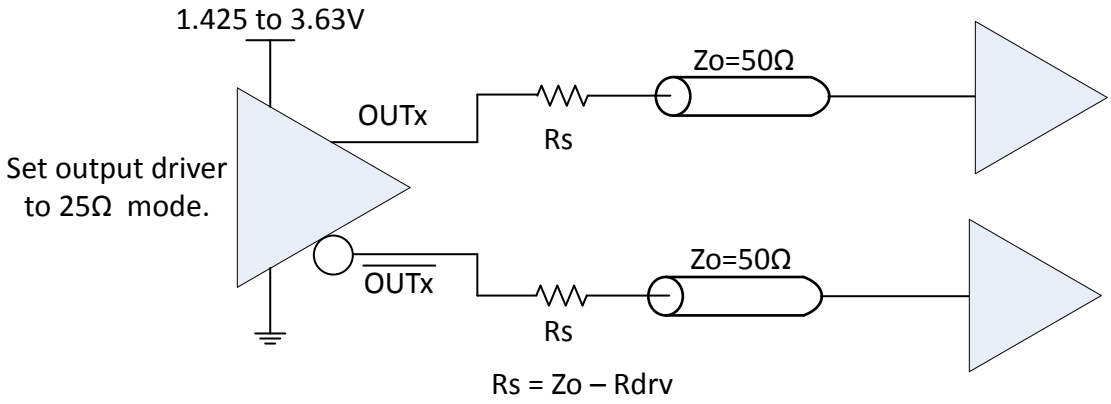


Figure 5.2. LVCMOS Termination, Option 2

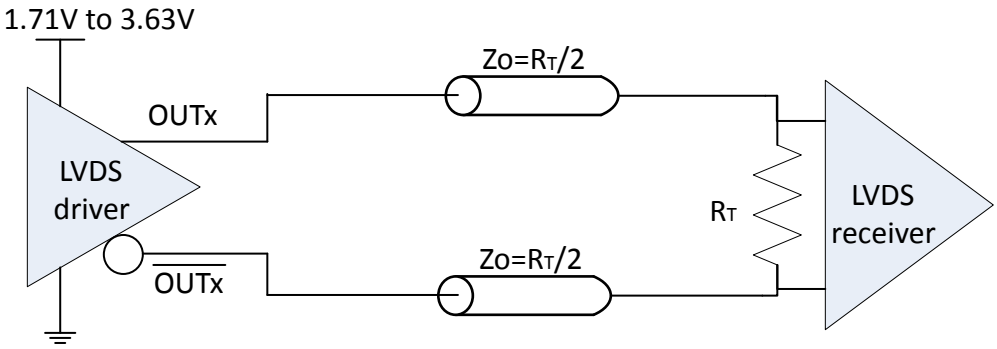


Figure 5.3. LVDS/LVDS Fast Termination, Option 1

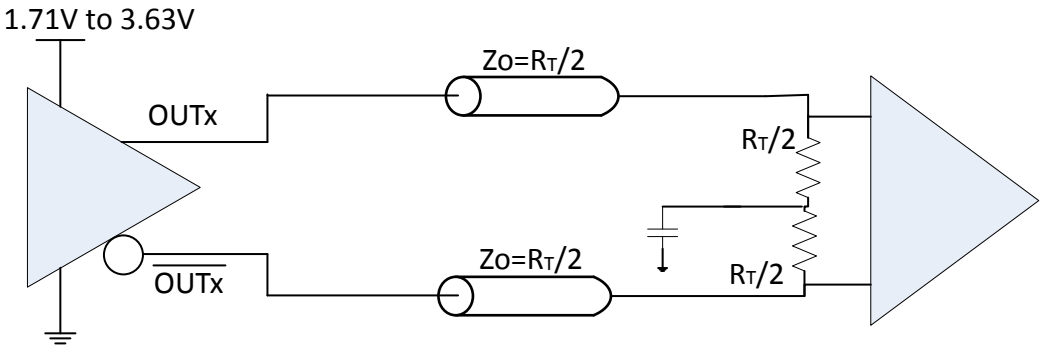


Figure 5.4. LVDS/LVDS Fast Termination, Option 2

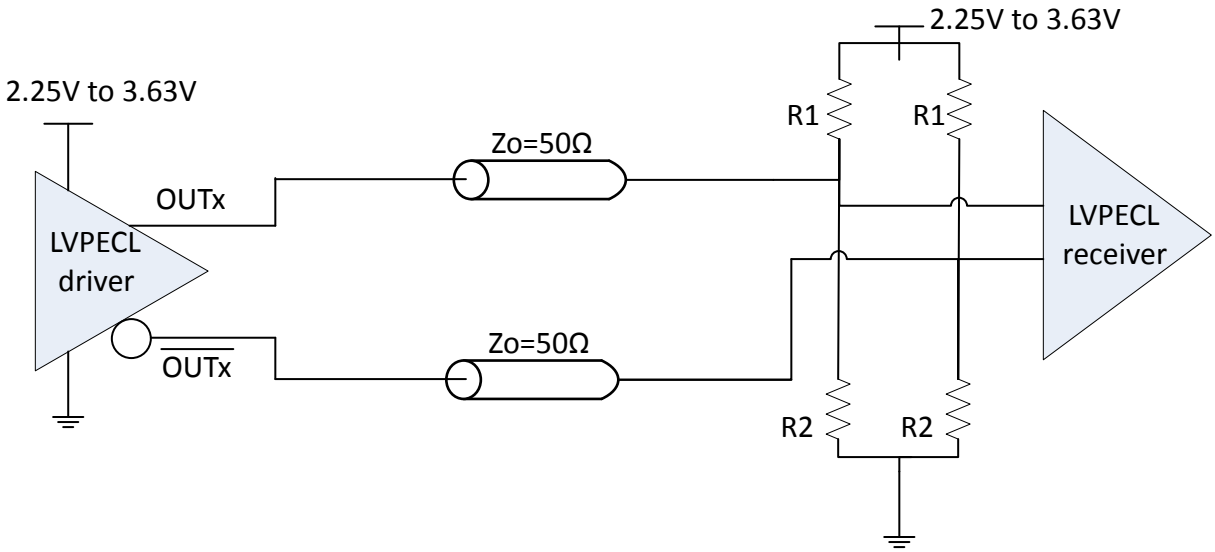


Figure 5.5. LVPECL Termination, Option 1

Table 5.3. LVPECL Termination, Option 1

VDD Standard	Resistance	Resistance Value
2.5	R1	250
	R2	62.5
3.3	R1	125
	R2	84

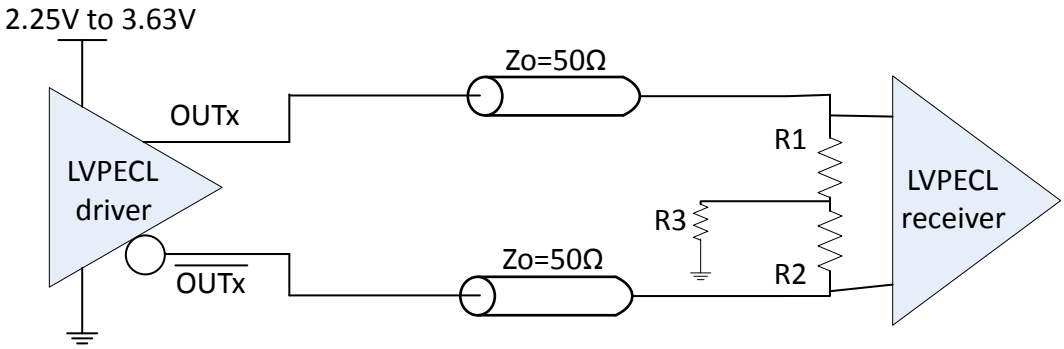


Figure 5.6. LVPECL Termination, Option 2

Table 5.4. LVPECL Termination, Option 2

VDD Standard	Resistance	Resistance Value
2.5	R1	50
	R2	50
	R3	29.5
3.3	R1	50
	R2	50
	R3	54 or 0

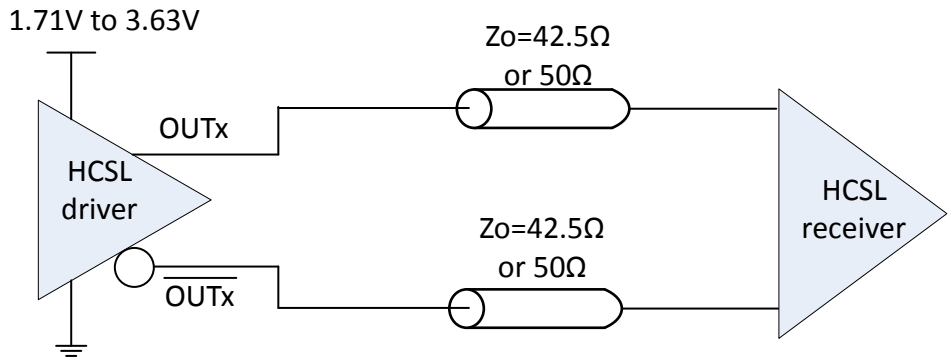


Figure 5.7. HCSL Internal Termination Mode

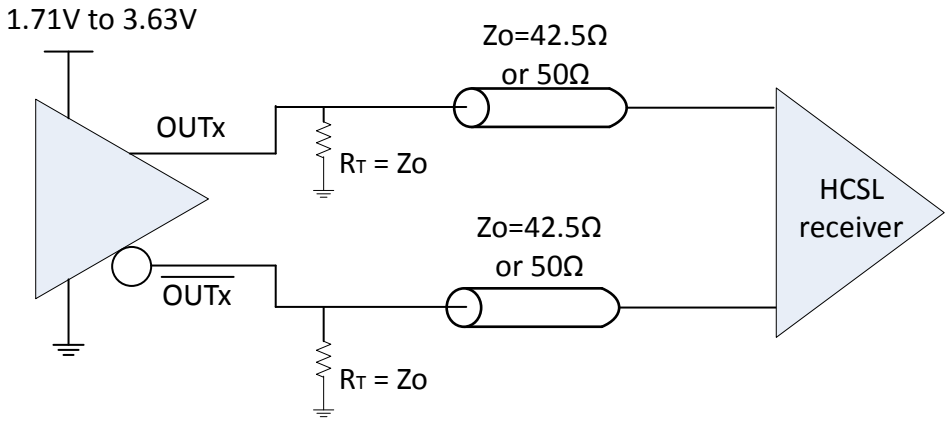


Figure 5.8. HCSL External Termination Mode

5.2 AC-Coupled Clock Terminations

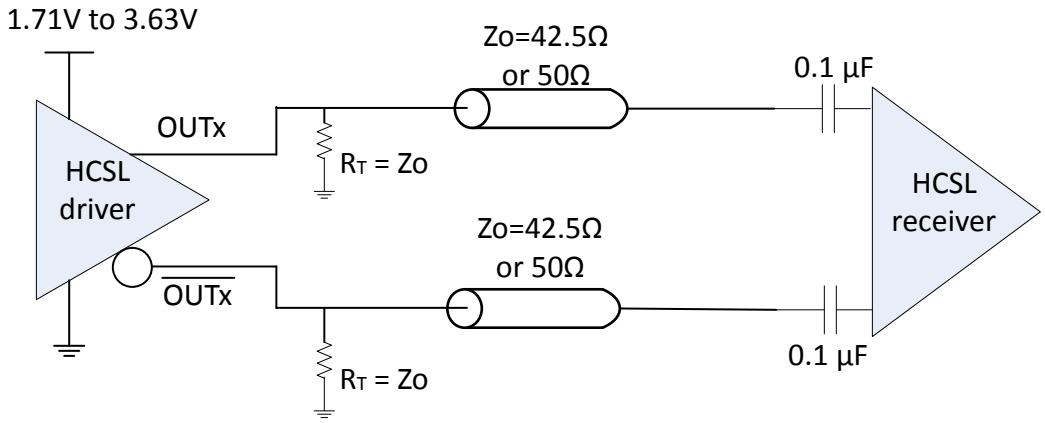


Figure 5.9. HCSL External Termination Mode

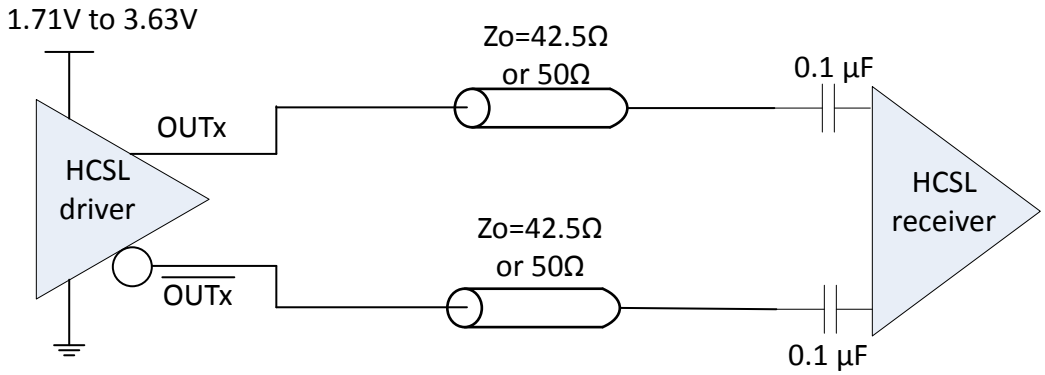


Figure 5.10. HCSL Internal Termination Mode

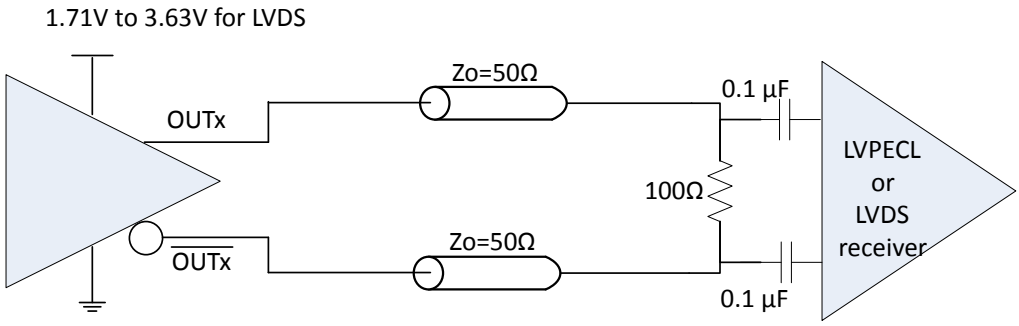


Figure 5.11. LVDS Termination

The terminations (shown in Figure 5.3 LVDS/LVDS Fast Termination, Option 1 on page 13 through Figure 5.6 LVPECL Termination, Option 2 on page 15) can also be converted by adding DC-blocking capacitances right before the receiver pins. However, the recommendation shown in Figure 5.11 LVDS Termination on page 16 is the simplest way to realize AC-coupling (i.e., the least number of components) and is, hence, the recommended circuit for AC-coupled termination circuits.

6. Programming the Volatile Memory

The volatile memory can be programmed to set up the various functions necessary to realize a PLL function, a clock output to clock input relationship and can be used to monitor input clock that controls the PLL. The front page block diagram is repeated here to refresh the various limits and possibilities that are necessary for the calculations below

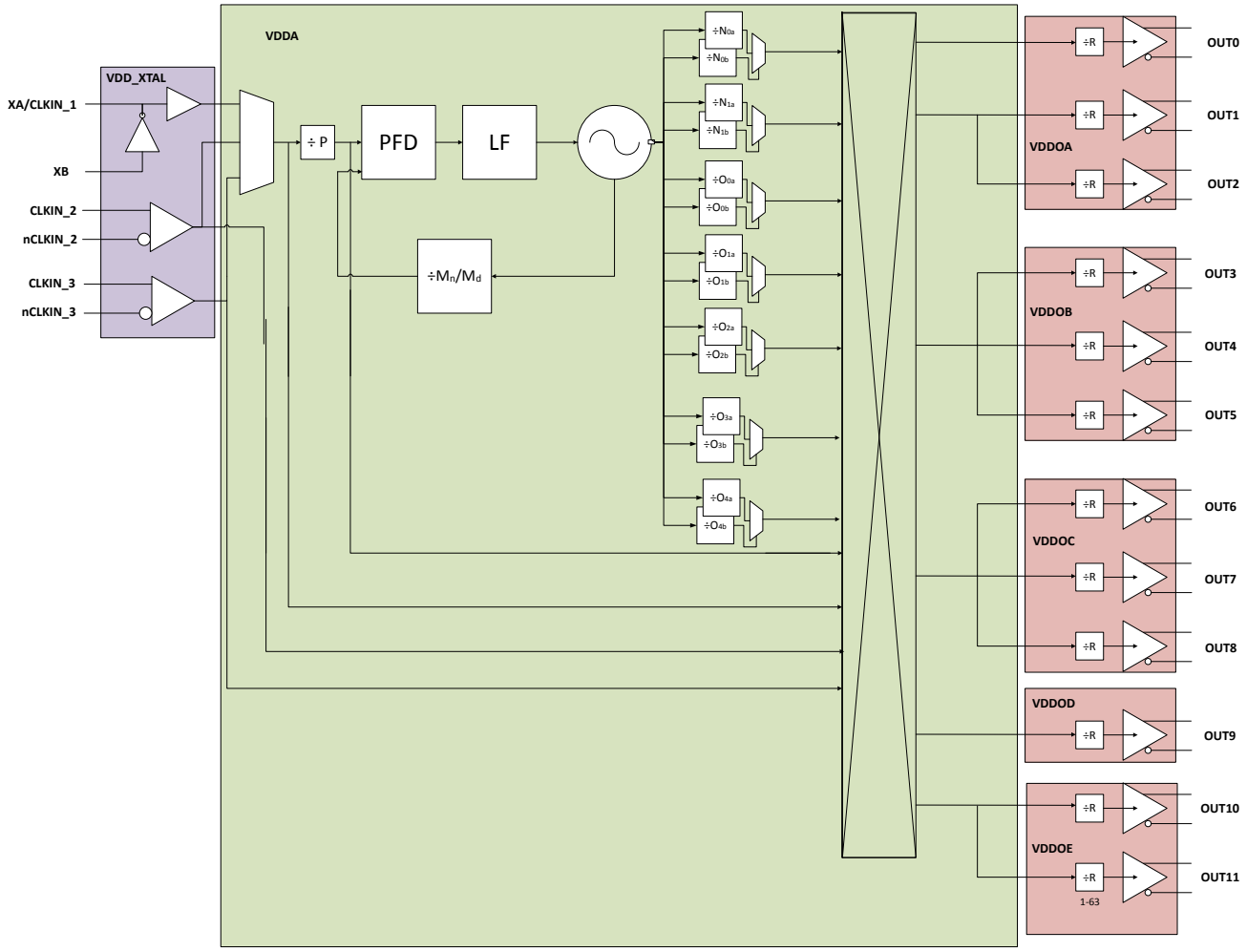


Figure 6.1. Top Level Block Diagram

6.1 Programming the PLL

The PLL programming involves three distinct constraints:

1. The minimum and the maximum frequencies possible for the PFD (Phase Frequency Detector) at lock. That is set by the reference frequency which is set the input divider P and the active input clock as selected by the IN SEL pins or registers.
2. The VCO frequency that is set by feedback divider (Mn/Md) and the PFD frequency also has a limited range that is unique to Si5332.
3. The PLL closed loop transfer function characterized by its loop band width and peaking is set by programming the loop parameters.

The table below lists the constraints for the PLL reference frequency and the VCO frequency. The PLL reference frequency (`pllRefFreq`) and the VCO frequency (`vcoFreq`) are related by the equation below:

$$vcoFreq = pllRefFreq \times \left(\frac{M_n}{M_d}\right)$$

For a given plan, the `pllRefFreq` can be readily solved as it is derived from the input clock frequency. To get to this optimization, the "active" input to the PLL must be selected from the XA/XB, CLKIN_1, CLKIN)2, in1p/m input clocks using either the IMUX_SEL register field or the CLKIN_SEL pins {if CKIN_SEL pins are available in the custom part that you choose to reprogram}. `PllRefFreq` is given by the In-Freq (active clock input frequency) and P as:

$$PllRefFreq = \frac{InFreq}{P}$$

Table 6.1. Constraints for PLL Reference Frequency and VCO Frequency

Field Name	Value	Description
`pllMinRefFreq`	10 MHz	The minimum reference frequency the PLL can tolerate
`pllMaxRefFreq`	50 MHz	The maximum reference frequency the PLL can tolerate
`vcoCenterFreq`	2.5 GHz	The center frequency of the VCO's tuning range
`vcoMinFreq`	2.375 GHz	The minimum frequency of the VCO's tuning range
`vcoMaxFreq`	2.625 GHz	The maximum frequency of the VCO's tuning range

List all required output frequencies, Fxy, in groups denoted by Gx, where x = 0,1,2,3,4,5 and y = a,b,c. This grouping is done such that frequencies related to each other by rational fractions of integers between 1 and 63 are in that group. For example, 100 MHz/80 MHz = 5/4 is a rational fraction. Each group Gx is associated with a single output voltage supply driver inside Si5332 and is shown in Table 6.2 Output Frequency Variables Grouping and Mapping to Actual Output Pins on page 19. The table also shows the output frequency symbol Fxy mapped to the output name in the Si5332 pin descriptions. The integer O-dividers are denoted by hsdiv. Each Oi divider maps to a hsdivi in the solver where i is an integer between 0 and 4. Similarly, the two Multisynth N-dividers, Nj map to IDj and j = 0 or 1.The constraints for these divider values are listed in Table 6.3 Constraints for `hsdiv` and `id` on page 19.

Table 6.2. Output Frequency Variables Grouping and Mapping to Actual Output Pins

Si5332 12 Output Part Output Pair	Si5332 8 Output Part Output Pair	Si5332 6 Output Part Output Pair	Output Frequency Variable for Solver	The Output Frequency Group
OUT0	OUT0	OUT0	F_{0A}	G_0
OUT1	OUT1	OUT1	F_{1A}	G_1
OUT2			F_{1B}	G_1
OUT3	OUT2	OUT2	F_{2A}	G_2
OUT4	OUT3		F_{2B}	G_2
OUT5			F_{2C}	G_2
OUT6	OUT4	OUT3	F_{3A}	G_3
OUT7	OUT5		F_{3B}	G_3
OUT8			F_{3C}	G_3
OUT9	OUT6	OUT4	F_{4A}	G_4
OUT10	OUT7	OUT5	F_{5A}	G_5
OUT11			F_{5B}	G_5

Table 6.3. Constraints for `hsdiv` and `id`

Field Name	Value	Description
`hsdivMinDiv`	8	The minimum divide value that the HSDIV can support
`hsdivMaxDiv`	255	The maximum divide value that the HSDIV can support
`idMinDiv`	10	The minimum divide value that the ID can support
`idMaxDiv`	255	The maximum divide value that the ID can support

Each output frequency `Foutxy` is given by:

$$Foutxy = \frac{vcoFreq}{\{hsdiv_j \times Rxy\}}$$

or

$$Foutxy = \frac{vcoFreq}{\{id_j \times Rxy\}}$$

An `hsdiv` or `id` divider is common for output frequencies grouped in a given Gx. Given these constraints, the solver must first choose a *PllRefFreq* that satisfies the constraints in Table 6.4 Loop BW Options on page 20. The search for `VcoFreq` can be broken down into the following steps.

1. From the output frequency set, form a set of “M” non-equal frequencies. Group the (N-M) equal frequencies into the same “x” in Foutxy grouping.

2. Now form ${}^{M}C_{2}$ groups of {M-2} output frequencies. Find the LCM of each group and find an integer "I" that can such that:
   a. `vcoFreq` = I*LCM can meet the constraint for `vcoFreq` in Table 6.1 Constraints for PLL Reference Frequency and VCO Frequency on page 18.
   b. List the "L" groups that provide a legal `vcoFreq`, i.e. a `vcoFreq` that satisfies the condition in step a.
   c. Choose the `vcoFreq` that has most number of performance critical clocks that do not need "spread spectrum" clock-ing as part of the "M-2" output clocks

Given that `vcoFreq`, calculate the feedback divider as:

$$\frac{M_n}{M_d} = \frac{vcoFreq}{pllRefFreq}$$

The Mn/Md fraction is represented in register fields IDPA_INTG, IDPA_RES and IDPA_DEN

$$IDPA\_INTG = floor\left(\frac{128 \times vcoFreq}{pllRefFreq}\right)$$

$$\frac{IDPA\_RES}{IDPA\_DEN} = \frac{128 \times vcoFreq}{pllRefFreq} - IDPA\_INTG$$

As can be seen from the above equations, the ratio IDPA_RES/ IDPA_DEN will always be less than 1.

Note: All these register fields are 15 bits wide. Therefore, the fraction will need to truncate to up to this precision. This section fully determines the VCO frequency, the P-divider and the feedback divider for this plan given the choice of using O-dividers {HSDIV} for M-2 output clocks and N-dividers {ID} for two output clocks.

The next step will be to determine the closed loop response that is required from the PLL. The table below lists the different loop BW settings possible and the register field value that will enable that loop BW setting:

Table 6.4. Loop BW Options

PLL_MODE	Loop Bandwidth (kHz)	PLL. Ref. Freq. Min (MHz)	PLL. Ref. Freq. Max. (MHz)
0	ILLEGAL IF PLL MODE IS ENABLED		
1	350	10	15
2	250	10	15
3	175	10	15
4	500	15	30
5	350	15	30
6	250	15	30
7	175	15	30
8	500	30	50
9	350	30	50
10	250	30	50
11	175	30	50

This algorithm will result in a final solution for a VCO frequency, vcoFreq, that can then be used to calculate the O-divider , N-divider, and R-divider values needed to derive each output frequency, Foutxy.

6.2 Programming the Clock Path

Given a valid VCO frequency for the M unique frequencies, segregate the N-M equal frequencies into outputs from each group Gx in Table 6.2 Output Frequency Variables Grouping and Mapping to Actual Output Pins on page 19. When arranging outputs, care must be taken to minimize crosstalk (without violating the contraints imposed from the grouping of output frequencies into the VDDO “banks”). Whenever several high frequencies, fast rise time, large amplitude signals are all close to one another, the laws of physics dictate that there will be some amount of crosstalk. The jitter of the Si5332 is low, and, therefore, crosstalk can become a significant portion of the final measured output jitter. Some of the source of the crosstalk will be the Si5332 and some will be introduced by the PCB. For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks:

1. Avoid adjacent frequency values that are close. A 155.52 MHz clock should not be next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz, then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are okay and these outputs should be grouped accordingly.
3. Unused outputs can be used to separate clock outputs that might otherwise interfere with one another. If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines typically only need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided whenever possible. When CMOS is unavoidable, even greater care must be taken with respect to the above guidelines.

An output multiplexer (output mux) or crosspoint mux needs to be programmed such that each group Gx is set to the correct O-divider, N-divider, or input clock (in the case of buffering). Each output, Foutxy, has this common divider or input clock reference that needs to be set. The multipler setting that routes the correct divider/clock source to the correct group is shown in the following table.

Table 6.5. Output Mux (Crosspoint Mux) Settings

Register field	Description
`omuxx_sel0`	Selects output mux clock for output clocks in group Gx: 0 = PLL reference clock before pre-scaler 1 = PLL reference clock after pre-scaler 2 = Clock from input buffer 0 3 = Clock from input buffer 1
`omuxx_sel1`	Selects output mux clock for output clocks in group Gx: 0 = HSDIV0 1 = HSDIV1 2 = HSDIV2 3 = HSDIV3 4 = HSDIV4 5 = ID0 6 = ID1 7 = Clock from omux1_sel0

The final steps will be to program the `hsdiv` and `id` dividers. The equations below show the relationship between `hsdiv`, `id` divider values with their associated output frequency. They also show the register fields that need to be programmed to set up the divider values correctly. The register field and the divider value are both denoted by:

$$hsdivxa\_div = \frac{vcoFrq}{Foutxa \times Rxa}$$

The `id` dividers are calculated as below:

$$idxa = \frac{vcoFrq}{Foutxa \times Rxa}$$

The ida fraction is represented in register fields IDPA_INTG, IDPA_RES and IDPA_DEN

$$IDxA\_INTG = floor\left(\frac{128 \times vcoFreq}{Foutxa \times Rxa}\right)$$

$$\frac{IDxA\_RES}{IDxA\_DEN} = \frac{128 \times vcoFreq}{Foutxa \times Rxa} - IDxA\_INTG$$

6.3 Programming the Output Clock Frequency

The Rxy register fields are programmed as shown in the table below. This last step completes the settings of all dividers that will result in the frequency plan. When a valid divider solution space cannot be determined, that frequency plan is not realizable in the Si5332.

Table 6.6. Rxy to Register Field Mapping for 12-output Si5332

Divider Value	Register Field	Description
R0A	OUT0_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R1A	OUT1_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R1B	OUT2_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R2A	OUT3_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R2B	OUT4_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R2C	OUT5_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R3A	OUT6_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R3B	OUT7_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R3C	OUT8_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R4A	OUT9_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value

Divider Value	Register Field	Description
R5A	OUT10_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value
R5B	OUT11_DIV	Driver divider ratio. 0 = disabled 1–63 = divide value

6.4 Programming the Output Clock Format

The following tables provide the method to fully define every driver.

Table 6.7. Driver Set Up Options

Driver	Register Field	Description
Driver for output OUTx	OUTx_mode	Software interpreted driver configuration. See Table 6.8 Driver Mode Options on page 25.
	OUTx _skew	Skew control. Programmed as an unsigned integer. Can add delay of 35 ps/step up to 280 ps.
	OUTx _stop_highz	Driver output state when stopped. 0 = low-z 1 = high-z
	OUTx _cmos_inv	Sets the polarity of the two outputs in dual CMOS mode. 0 = no inversion 1 = OUTx~ inverted
	OUTx _cmos_slew	Controls CMOS slew rate from fast to slow. 00 = fastest 01 = slow 10 = slower 11 = Slowest
	OUTx _cmos_str	CMOS output impedance control. 0 = 50 Ω 1 = 25 Ω

Table 6.8. Driver Mode Options

drvxy_MODE	Driver Mode
0	off
1	CMOS on positive output only
2	CMOS on negative output only
3	dual CMOS outputs
4	2.5 V/3.3 V LVDS
5	1.8 V LVDS
6	2.5 V/3.3 V LVDS fast
7	1.8 V LVDS fast
8	HCSL 50 Ω (external termination)
9	HCSL 50 Ω (internal termination)
10	HCSL 42.5 Ω (external termination)
11	HCSL 42.5 Ω (internal termination)
12	LVPECL
13	Reserved
14	Reserved
15	Reserved