Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SILICON LABS

Si5338

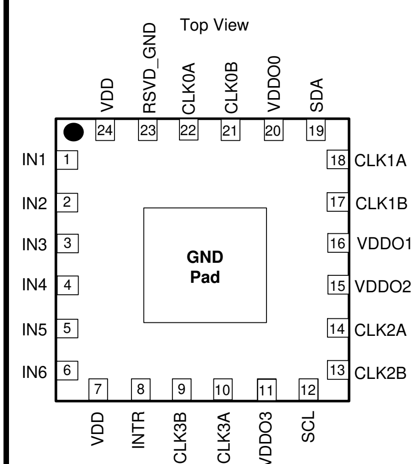
I²C-Programmable Any-Frequency, Any-Output Quad Clock Generator

Features

- Low power MultiSynth™ technology enables independent, any-frequency synthesis on four differential output drivers
- PCIe Gen 1/2/3/4 Common Clock and Gen 3 SRNS compliant
- Highly-configurable output drivers with up to four differential outputs, eight single-ended clock outputs, or a combination of both
- Low phase jitter of 0.7 ps RMS typ
- High precision synthesis allows true zero ppm frequency accuracy on all outputs
- Flexible input reference:
  - External crystal: 8 to 30 MHz
  - CMOS input: 5 to 200 MHz
  - SSTL/HSTL input: 5 to 350 MHz
  - Differential input: 5 to 710 MHz
- Independently configurable outputs support any frequency or format:
  - LVPECL/LVDS: 0.16 to 710 MHz
  - HCSL: 0.16 to 250 MHz
  - CMOS: 0.16 to 200 MHz
  - SSTL/HSTL: 0.16 to 350 MHz
- Independent output voltage per driver: 1.5, 1.8, 2.5, or 3.3 V
- Single supply core with excellent PSRR: 1.8, 2.5, 3.3 V
- Independent frequency increment/decrement feature enables glitchless frequency adjustments in 1 ppm steps
- Independent phase adjustment on each of the output drivers with an accuracy of ≤20 ps steps
- Highly configurable spread spectrum (SSC) on any output:
  - Any frequency from 5 to 350 MHz
  - Any spread from 0.5 to 5.0%
  - Any modulation rate from 33 to 63 kHz
- External feedback mode allows zero-delay mode
- Loss of lock and loss of signal alarms
- I²C/SMBus compatible interface
- Easy to use programming software
- Small size: 4 x 4 mm, 24-QFN
- Low power: 45 mA core supply typ
- Wide temperature range: –40 to +85 °C

Ordering Information:
See page 42.

Pin Assignments



Applications

- Ethernet switch/router
- PCIe Gen1/2/3/4
- Broadcast video/audio timing
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Description

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing any frequency on each of the device's four output drivers. This timing IC is capable of replacing up to four different frequency crystal oscillators or operating as a frequency translator. Using its patented MultiSynth™ technology, the Si5338 allows generation of four independent clocks with 0 ppm precision. Each output clock is independently configurable to support various signal formats and supply voltages. The Si5338 provides low-jitter frequency synthesis in a space-saving 4 x 4 mm QFN package. The device is programmable via an I²C/SMBus-compatible serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply. I²C device programming is made easy with the ClockBuilder™ Desktop software available at www.silabs.com/ClockBuilder. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

Functional Block Diagram

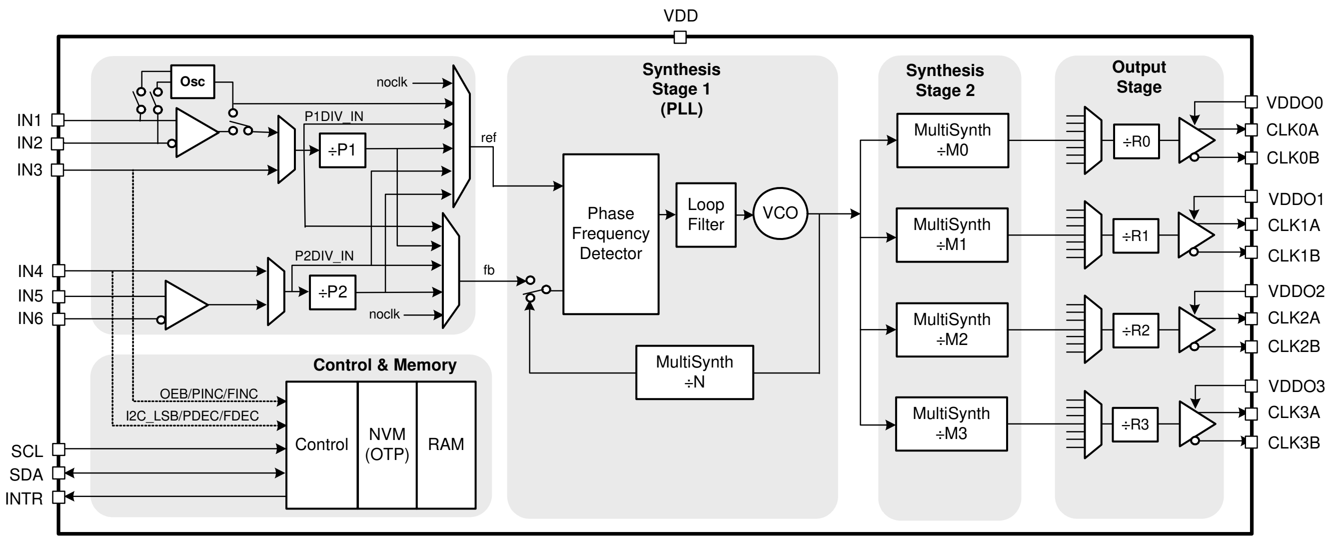


Table of Contents

1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.						

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2.5	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	
Junction Temperature	T_J		150	°C
Peak Soldering Reflow Temperature[2]			260	°C

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Refer to JEDEC J-STD-020 standard for more information.

Table 3. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	100 MHz on all outputs, 25 MHz refclk	—	45	60	mA
Core Supply Current (Buffer Mode)	I_{DDB}	50 MHz refclk	—	12	—	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	—	30	mA
		LVDS, 710 MHz	—	—	8	mA
		HCSL, 250 MHz 2 pF load	—	—	20	mA
		CML, 350 MHz	—	12	—	mA
		SSTL, 350 MHz	—	—	19	mA
		CMOS, 50 MHz 15 pF load[1]	—	6	9	mA
		CMOS, 200 MHz[1,2] 3.3 V VDD0	—	13	18	mA
		CMOS, 200 MHz[1,2] 2.5 V	—	10	14	mA
		CMOS, 200 MHz[1,2] 1.8 V	—	7	10	mA
		HSTL, 350 MHz	—	—	19	mA

Notes:

1. Single CMOS driver active.
2. Measured into a 5” 50 Ω trace with 2 pF load.

Table 4. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	10	°C/W

Table 5. Performance Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Acquisition Time	t_{ACQ}		—	—	25	ms
PLL Tracking Range	f_{TRACK}		5000	20000	—	ppm
PLL Loop Bandwidth	f_{BW}		—	1.6	—	MHz
MultiSynth Frequency Synthesis Resolution	f_{RES}	Output frequency $\leq$ Fvco/8	0	0	1	ppb
CLKIN Loss of Signal Detect Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Release Time	t_{LOSRLS}		0.01	0.2	1	µs
PLL Loss of Lock Detect Time	t_{LOL}		—	5	10	ms
POR to Output Clock Valid (Pre-programmed Devices)	t_{RDY}		—	—	2	ms
Input-to-Output Propagation Delay	t_{PROP}	Buffer Mode (PLL Bypass)	—	2.5	4	ns
Output-Output Skew	t_{DSKEW}	Rn divider = 1[1]	—	—	100	ps
POR to I^2C Ready			—	—	15	ms
Programmable Initial Phase Offset	P_{OFFSET}		–45	—	+45	ns
Phase Increment/Decrement Accuracy	P_{STEP}		—	—	20	ps
Phase Increment/Decrement Range	P_{RANGE}		–45	—	+45	ns
MultiSynth range for phase increment/decrement	f_{PRANGE}		5	—	Fvco/8[2]	MHz
Phase Increment/Decrement Update Time	P_{UPDATE}	Pin control[2,3] MultiSynth output >18 MHz	667	—	—	ns

Notes:
1. Outputs at integer-related frequencies and using the same driver format. See "3.10.3. Programmable Initial Phase Offset" on page 27.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and Fvco/8.
3. Update rate via I^2C is also limited by the time it takes to perform a write operation.
4. Default value is 0.5% down spread.
5. Default value is ~31.5 kHz.

Table 5. Performance Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Increment/Decrement Update Time	P_{UPDATE}	Pin control[2,3] MultiSynth output <18 MHz Number of periods of MultiSynth output frequency	—	10	12	Periods
Frequency Increment/ Decrement Step Size	f_{STEP}	R divider not used	1	—	See Note [2]	ppm
MultiSynth range for frequency increment/decrement	f_{RANGE}	R divider not used	5	—	Fvco/8	MHz
Frequency Increment/ Decrement Update Time	f_{UPDATE}	Pin control[2,3] MultiSynth output >18 MHz	—	—	667	ns
Frequency Increment/ Decrement Update Time	f_{UPDATE}	Pin control[2,3] MultiSynth output <18 MHz Number of periods of MultiSynth output frequency	—	10	12	Periods
Spread Spectrum PP Frequency Deviation	SS_{DEV}	MultiSynth Output ≤ ~Fvco/8	0.1	—	5.0[4]	%
Spread Spectrum Modulation Rate	SS_{DEV}	MultiSynth Output ≤ ~Fvco/8	30	—	63[5]	kHz

Notes:
1. Outputs at integer-related frequencies and using the same driver format. See "3.10.3. Programmable Initial Phase Offset" on page 27.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and Fvco/8.
3. Update rate via I^2C is also limited by the time it takes to perform a write operation.
4. Default value is 0.5% down spread.
5. Default value is ~31.5 kHz.

Table 6. Input and Output Clock Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Clock (AC Coupled Differential Input Clocks on Pins IN1/2, IN5/6)[1]						
Frequency	f_{IN}		5	—	710	MHz
Differential Voltage Swing	V_{PP}	710 MHz input	0.4	—	2.4	V_{PP}
Rise/Fall Time[2]	t_R/t_F	20%–80%	—	—	1.0	ns
Duty Cycle	DC	< 1 ns tr/tf	40	—	60	%
Duty Cycle	DC (PLL bypass)[3]	< 1 ns tr/tf	45	—	55	%
Input Impedance[1]	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (DC-Coupled Single-Ended Input Clock on Pins IN3/4)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
Input Voltage	V_I		–0.1	—	3.73	V
Input Voltage Swing		200 MHz	0.8	—	VDD+10%	Vpp
Rise/Fall Time[4]	t_R/t_F	10%–90%	—	—	4	ns
Rise/Fall Time[4]	t_R/t_F	20%–80%	—	—	2.3	ns
Duty Cycle[5]	DC	< 4 ns tr/tf	40	—	60	%
Input Capacitance	C_{IN}		—	2.0	—	pF
Output Clocks (Differential)						
Frequency[6]	f_{OUT}	LVPECL, LVDS, CML	0.16	—	350	MHz
			367	—	473.33	MHz
			550	—	710	MHz
		HCSL	0.16	—	250	MHz

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See Figure 3.
2. For best jitter performance, keep the midpoint differential input slew rate on pins 1,2,5,6 faster than 0.3 V/ns.
3. Minimum input frequency in clock buffer mode (PLL bypass) is 5 MHz. Operation to 1 MHz is also supported in buffer mode, but loss-of-signal (LOS) status is not functional.
4. For best jitter performance, keep the mid point input single ended slew rate on pins 3 or 4 faster than 1 V/ns.
5. Not in PLL bypass mode.
6. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6. See "3.3. Synthesis Stages" on page 19.
7. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver.
8. Includes effect of internal series 22 Ω resistor.

Table 6. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVPECL Output Voltage	V_{OC}	common mode	—	V_{DDO}– 1.45 V	—	V
	V_{SEPP}	peak-to-peak single-ended swing	0.55	0.8	0.96	V_{PP}
LVDS Output Voltage (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{SEPP}	Peak-to-Peak Single-Ended Swing	0.25	0.35	0.45	V_{PP}
LVDS Output Voltage (1.8 V)	V_{OC}	Common Mode	0.8	0.875	0.95	V
	V_{SEPP}	Peak-to-Peak Single-Ended Swing	0.25	0.35	0.45	V_{PP}
HCSL Output Voltage	V_{OC}	Common Mode	0.35	0.375	0.400	V
	V_{SEPP}	Peak-to-Peak Single-Ended Swing	0.575	0.725	0.85	V_{PP}
CML Output Voltage	V_{OC}	Common Mode	—	See Note 7	—	V
	V_{SEPP}	Peak-to-Peak Single-Ended Swing	0.67	0.860	1.07	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps
Duty Cycle[5]	DC		45	—	55	%
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	0.16	—	200	MHz
		SSTL, HSTL	0.16	—	350	MHz
CMOS 20%–80% Rise/Fall Time	t_R/t_F	2 pF load	—	0.45	0.85	ns
CMOS 20%–80% Rise/Fall Time	t_R/t_F	15 pF load	—	—	2.0	ns

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See Figure 3.
2. For best jitter performance, keep the midpoint differential input slew rate on pins 1,2,5,6 faster than 0.3 V/ns.
3. Minimum input frequency in clock buffer mode (PLL bypass) is 5 MHz. Operation to 1 MHz is also supported in buffer mode, but loss-of-signal (LOS) status is not functional.
4. For best jitter performance, keep the mid point input single ended slew rate on pins 3 or 4 faster than 1 V/ns.
5. Not in PLL bypass mode.
6. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6. See "3.3. Synthesis Stages" on page 19.
7. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver.
8. Includes effect of internal series 22 Ω resistor.

Table 6. Input and Output Clock Characteristics (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CMOS Output Resistance			—	50	—	Ω
SSTL Output Resistance			—	50	—	Ω
HSTL Output Resistance			—	50	—	Ω
CMOS Output Voltage[8]	V_{OH}	4 mA load	VDDO – 0.3	—		V
	V_{OL}	4 mA load		—	0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	0.45xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.45xVDDO –0.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.5xVDDO–0.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+0.34	—		V
	V_{OL}		—	—	0.5xVDDO–0.34	V
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO+0.3	—	—	V
	V_{OL}		—	—	0.5xVDDO – 0.3	V
Duty Cycle[5]	DC		45	—	55	%

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See Figure 3.
2. For best jitter performance, keep the midpoint differential input slew rate on pins 1,2,5,6 faster than 0.3 V/ns.
3. Minimum input frequency in clock buffer mode (PLL bypass) is 5 MHz. Operation to 1 MHz is also supported in buffer mode, but loss-of-signal (LOS) status is not functional.
4. For best jitter performance, keep the mid point input single ended slew rate on pins 3 or 4 faster than 1 V/ns.
5. Not in PLL bypass mode.
6. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6. See "3.3. Synthesis Stages" on page 19.
7. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver.
8. Includes effect of internal series 22 Ω resistor.

Table 7. Control Pins

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Control Pins (IN3, IN4)						
Input Voltage Low	V_{IL}		–0.1	—	0.3 x V_{DD}	V
Input Voltage High	V_{IH}		0.7 x V_{DD}	—	3.73	V
Input Capacitance	C_{IN}		—	—	4	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Output Control Pins (INTR)						
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time 20–80%	t_R/t_F	C_L < 10 pf, pull up = 1 kΩ	—	—	10	ns

Table 8. Crystal Specifications for 8 to 11 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	8	—	11	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O	—	—	6	pF
Equivalent Series Resistance	r_{ESR}	—	—	300	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to adjust the registers to accommodate a 12 pF crystal C_L.

Table 9. Crystal Specifications for 11 to 19 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	11	—	19	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	200	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to adjust the registers to accommodate a 12 pF crystal C_L.

Table 10. Crystal Specifications for 19 to 26 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	19		26	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			100	Ω
Crystal Max Drive Level	d_L	100			µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to adjust the registers to accommodate a 12 pF crystal C_L.

Table 11. Crystal Specifications for 26 to 30 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	26		30	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			75	Ω
Crystal Max Drive Level	d_L	100			µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to adjust the registers to accommodate a 12 pF crystal C_L.

Table 12. Jitter Specifications[1,2,3]
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GbE Random Jitter (12 kHz–20 MHz)[4]	J_{GbE}	CLKIN = 25 MHz All CLKn at 125 MHz[5]	—	0.7	1	ps RMS
GbE Random Jitter (1.875–20 MHz)	R_{JGbE}	CLKIN = 25 MHz All CLKn at 125 MHz[5]	—	0.38	0.79	ps RMS
OC-12 Random Jitter (12 kHz–5 MHz)	J_{OC12}	CLKIN = 19.44 MHz All CLKn at 155.52 MHz[5]	—	0.7	1	ps RMS
PCI Express 1.1 Common Clocked		Total Jitter[6]	—	20.1	33.6	ps pk-pk
PCI Express 2.1 Common Clocked		RMS Jitter[6], 10 kHz to 1.5 MHz	—	0.15	1.47	ps RMS
		RMS Jitter[6], 1.5 MHz to 50 MHz	—	0.58	0.75	ps RMS
PCI Express 3.0 Common Clocked		RMS Jitter[6]	—	0.15	0.45	ps RMS
PCIe Gen 3 Separate Reference No Spread, SRNS		PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.11	0.32	ps RMS
PCIe Gen 4, Common Clock		PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.15	0.45	ps RMS
Period Jitter	J_{PER}	N = 10,000 cycles[7]	—	10	30	ps pk-pk

Notes:
1. All jitter measurements apply for LVDS/HCSL/LVPECL/CML output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. For best jitter performance, keep the single ended clock input slew rates at Pins 3 and 4 more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.
3. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 3 ps rms, contact Silicon Labs for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
4. D_J for PCI and GbE is < 5 ps pp
5. Output MultiSynth in Integer mode.
6. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is measured with the Intel Clock Jitter Tool, Ver. 1.6.4.
7. Input frequency to the Phase Detector between 25 and 40 MHz and any output frequency $\geq$ 5 MHz.
8. Measured in accordance with JEDEC standard 65.
9. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.
10. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
11. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 12. Jitter Specifications[1,2,3] (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-Cycle Jitter	J_{CC}	N = 10,000 cycles Output MultiSynth operated in integer or fractional mode[7]	—	9	29	ps pk[8]
Random Jitter (12 kHz–20 MHz)	R_J	Output and feedback MultiSynth in integer or fractional mode[7]	—	0.7	1.5	ps RMS
Deterministic Jitter	D_J	Output MultiSynth operated in fractional mode[7]	—	3	15	ps pk-pk
		Output MultiSynth operated in integer mode[7]	—	2	10	ps pk-pk
Total Jitter (12 kHz–20 MHz)	$T_J = D_J + 14 \times R_J$ (See Note [9])	Output MultiSynth operated in fractional mode[7]	—	13	36	ps pk-pk
		Output MultiSynth operated in integer mode[7]	—	12	20	ps pk-pk

Notes:

1. All jitter measurements apply for LVDS/HCSL/LVPECL/CML output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. For best jitter performance, keep the single ended clock input slew rates at Pins 3 and 4 more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.
3. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 3 ps rms, contact Silicon Labs for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
4. D_J for PCI and GbE is < 5 ps pp
5. Output MultiSynth in Integer mode.
6. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is measured with the Intel Clock Jitter Tool, Ver. 1.6.4.
7. Input frequency to the Phase Detector between 25 and 40 MHz and any output frequency $\geq$ 5 MHz.
8. Measured in accordance with JEDEC standard 65.
9. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.
10. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
11. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 13. Jitter Specifications, Clock Buffer Mode (PLL Bypass)*
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additive Phase Jitter (12 kHz–20 MHz)	t_{RPHASE}	0.7 V pk-pk differential input clock at 622.08 MHz with 70 ps rise/fall time	—	0.165	—	ps RMS
Additive Phase Jitter (50 kHz–80 MHz)	$t_{RPHASEWB}$	0.7 V pk-pk differential input clock at 622.08 MHz with 70 ps rise/fall time	—	0.225	—	ps RMS
***Note:** All outputs are in Clock Buffer mode (PLL Bypass).						

Table 14. Typical Phase Noise Performance

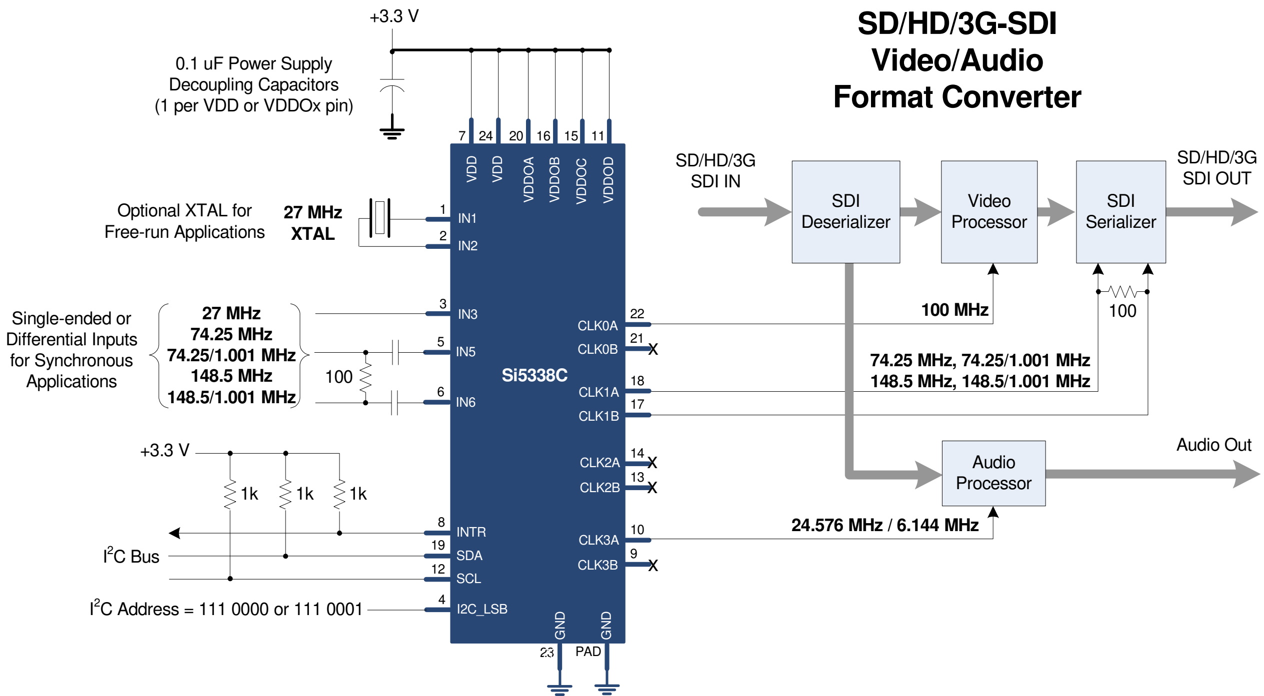
Offset Frequency	25 MHz XTAL to 156.25 MHz	27 MHz Ref In to 148.3517 MHz	19.44 MHz Ref In to 155.52 MHz	Units
100 Hz	–90	–87	–110	dBc/Hz
1 kHz	–120	–117	–116	dBc/Hz
10 kHz	–126	–123	–123	dBc/Hz
100 kHz	–132	–130	–128	dBc/Hz
1 MHz	–132	–132	–128	dBc/Hz
10 MHz	–145	–145	–145	dBc/Hz

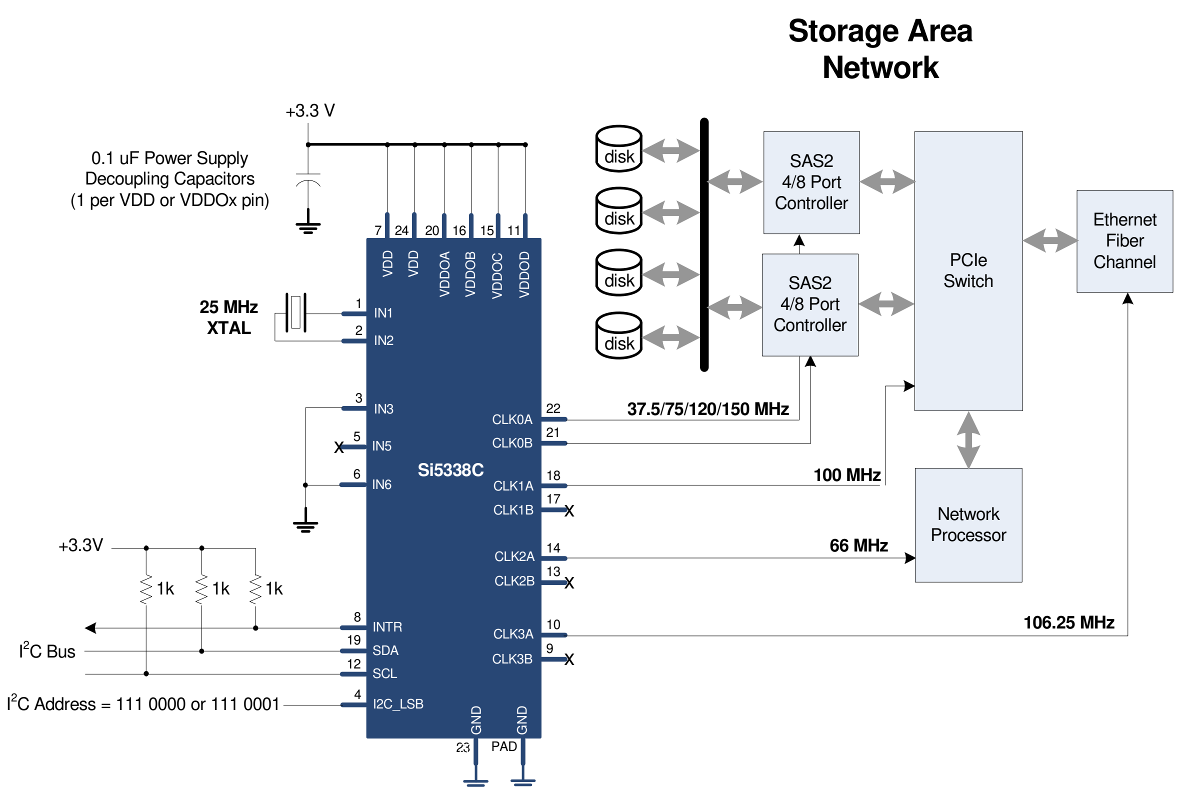
Table 15. I²C Specifications (SCL,SDA)[1]

Parameter	Symbol	Test Condition	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
LOW Level Input Voltage	V_{ILI2C}		–0.5	0.3 x V_{DDI2C}	–0.5	0.3 x V_{DDI2C}[2]	V
HIGH Level Input Voltage	V_{IHI2C}		0.7 x V_{DDI2C}	3.63	0.7 x V_{DDI2C}[2]	3.63	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		N/A	N/A	0.1	—	V
LOW Level Output Voltage (open drain or open collector) at 3 mA Sink Current	V_{OLI2C}[2]	V_{DDI2C}[2] = 2.5/3.3 V	0	0.4	0	0.4	V
		V_{DDI2C}[2] = 1.8 V	N/A	N/A	0	0.2 x V_{DDI2C}	V
Input Current	I_{I2C}		–10	10	–10	10	µA
Capacitance for each I/O Pin	C_{I2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I²C Bus Timeout	—	Timeout Enabled	25	35	25	35	ms
Data Rate		Standard Mode	100		400		kbps
Hold Time (Repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Set-Up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time[3,4]	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-Up Time	$t_{SU:DAT}$		250	—	150	—	ns

Notes:
1. Refer to NXP's UM10204 I²C-bus specification and user manual, Revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
2. I²C pullup voltages (VDDI2C) of 1.71 to 3.63 V are supported. Must write register 27[7] = 1 if the I²C bus voltage is less than 2.5 V to maintain compatibility with the I²C bus standard.
3. Hold time is defined as the time that data should hold its logical value after clock has transitioned to a logic low.
4. Guaranteed by characterization.

2. Typical Application Circuits





3. Functional Description

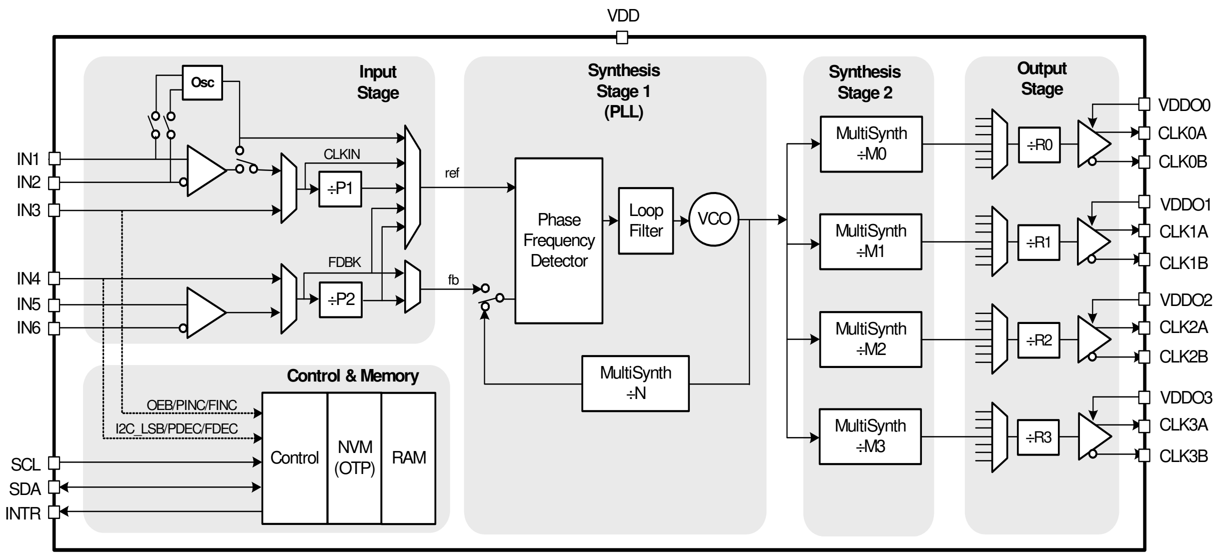


Figure 1. Si5338 Block Diagram

3.1. Overview

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing four independent user-programmable clock frequencies up to 350 MHz and select frequencies up to 710 MHz. The device supports free-run operation using an external crystal, or it can lock to an external clock for generating synchronous clocks. The output drivers support four differential clocks or eight single-ended clocks or a combination of both. The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, CMOS, HSTL, and SSTL. Separate output supply pins allow supply voltages of 3.3, 2.5, 1.8, and 1.5 V to support the multi-format output driver. The core voltage supply accepts 3.3, 2.5, or 1.8 V and is independent from the output supplies.

Using its two-stage synthesis architecture and patented high-resolution MultiSynth technology, the Si5338 can generate four independent frequencies from a single input frequency. In addition to clock generation, the inputs can bypass the synthesis stage enabling the Si5338 to be used as a high-performance clock buffer or a combination of a buffer and generator.

For applications that need fine frequency adjustments, such as clock margining, each of the synthesized frequencies can be incremented or decremented in user-defined steps as low as 1 ppm per step.

Output-to-output phase delays are also adjustable in user-defined steps with an error of <20 ps to compensate for PCB trace delays or for fine tuning of setup and hold margins.

A zero-delay mode is also available to help minimize input-to-output delay. Spread spectrum is available on each of the clock outputs for EMI-sensitive applications, such as PCI Express.

Configuration and control of the Si5338 is mainly handled through the I^2C/SMBus interface. Some features, such as output enable and frequency or phase adjustments, can optionally be pin controlled. The device has a maskable interrupt pin that can be monitored for loss of lock or loss of input signal conditions.

The device also provides the option of storing a user-definable clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up.

3.1.1. ClockBuilder™ Desktop Software

To simplify device configuration, Silicon Labs provides ClockBuilder Desktop software, which can operate stand alone or in conjunction with the Si5338 EVB. When the software is connected to an Si5338 EVB it will control both the supply voltages to the Si5338 as well as the entire clock path within the Si5338. Clockbuilder Desktop can also measure the current delivered by the EVB regulators to each supply voltage of the Si5338. A Si5338 configuration can be written to a text file to be used by any system to configure the Si5338 via I^2C.

ClockBuilder Desktop can be downloaded from www.silabs.com/ClockBuilder and runs on Windows XP, Windows Vista, and Windows 7.

3.2. Input Stage

The input stage supports four inputs. Two are used as the *clock inputs* to the synthesis stage, and the other two are used as *feedback inputs* for zero delay or external feedback mode. In cases where external feedback is not required, all four inputs are available to the synthesis stage. The *reference selector* selects one of the inputs as the reference to the synthesis stage. The input configuration is selectable through the I^{2}C interface. The input MUXes are set automatically in ClockBuilder Desktop (see “3.1.1. ClockBuilder™ Desktop Software”). For information on setting the input MUXs manually, see the Si5338 Reference Manual: Configuring the Si5338 without ClockBuilder Desktop.

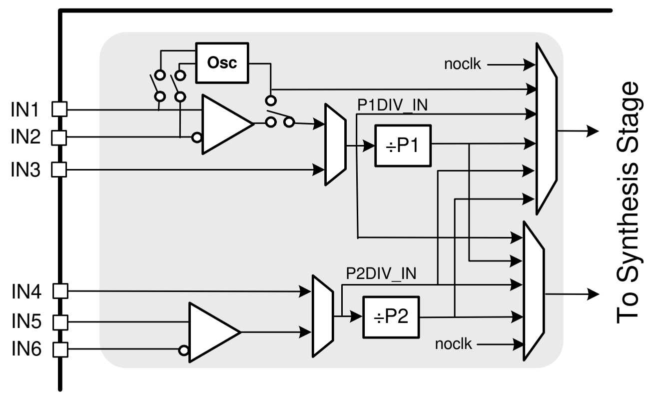


Figure 2. Input Stage

IN1/IN2 and IN5/IN6 are differential inputs capable of accepting clock rates from 5 to 710 MHz. The differential inputs are capable of interfacing to multiple signals, such as LVPECL, LVDS, HSCT, HCSL, and CML. Differential signals must be ac-coupled as shown in Figure 3. A termination resistor of 100 Ω placed close to the input pins is also required. Refer to Table 6 for signal voltage limits.

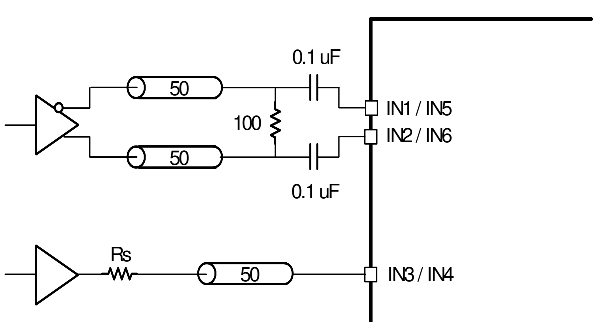


Figure 3. Interfacing Differential and Single-Ended Signals to the Si5338

IN3 and IN4 accept single-ended signals from 5 MHz to 200 MHz. The single-ended inputs are internally ac-coupled; so, they can accept a wide variety of signals without requiring a specific dc level. The input signal only needs to meet a minimum voltage swing and must not exceed a maximum VIH or a minimum VIL. Refer to Table 6 for signal voltage limits. A typical single-ended connection is shown in Figure 3. For additional termination options, refer to “AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers—Si5338, Si5334, Si5330”.

For free-run operation, the internal oscillator can operate from a low-frequency fundamental mode crystal (XTAL) with a resonant frequency between 8 and 30 MHz. A crystal can easily be connected to pins IN1 and IN2 without external components as shown in Figure 4. See Tables 8–11 for crystal specifications that are guaranteed to work with the Si5338.

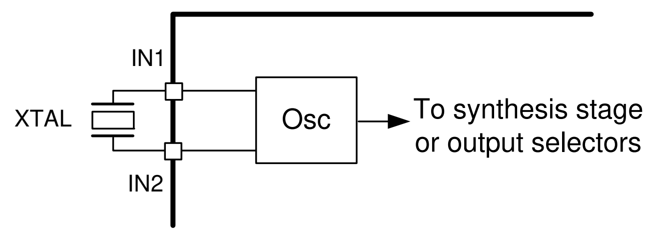


Figure 4. Connecting an XTAL to the Si5338

Refer to “AN360: Crystal Selection Guide for Si533x/5x Devices” for information on the crystal selection.

3.2.1. Loss-of-Signal (LOS) Alarm Detectors

There are two LOS detectors: LOS_CLKIN and LOS_FDBK. These detectors are tied to the outputs of the P1 and P2 frequency dividers, which are always enabled. See "3.6. Status Indicators" on page 24 for details on the alarm indicators. These alarms are used during programming to ensure that a valid input clock is detected. The input MUXs are set automatically in ClockBuilder Desktop (see the Si5338 Reference Manual to set manually).

3.3. Synthesis Stages

Next-generation timing applications require a wide range of frequencies that are often non-integer related. Traditional clock architectures address this by using multiple single PLL ICs, often at the expense of BOM complexity and power. The Si5338 uses patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of four Phase-Locked Loops (PLLs) in a single device, greatly reducing size and power requirements versus traditional solutions.

Synthesis of the output clocks is performed in two stages, as shown in Figure 5. The first stage consists of a high-frequency analog phase-locked loop (PLL) that multiplies the input stage to a frequency within the range of 2.2 to 2.84 GHz. Multiplication of the input frequency is accomplished using a proprietary and highly precise MultiSynth feedback divider (N), which allows the PLL to generate any frequency within its VCO range with much less jitter than typical fractional N PLL.

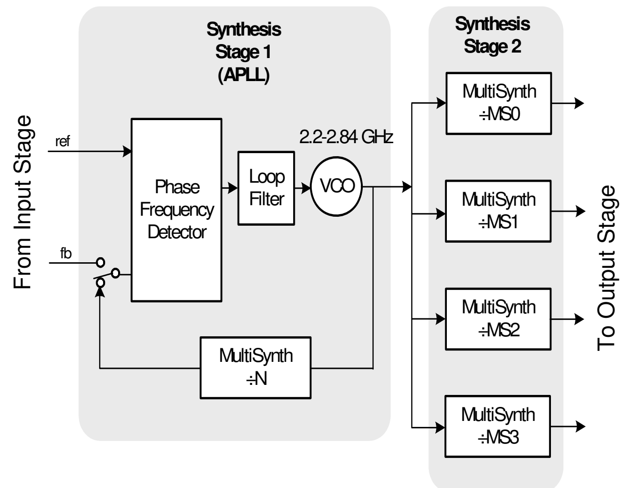


Figure 5. Synthesis Stages

The second stage of synthesis consists of the output MultiSynth dividers (MS_x). Based on a fractional N divider, the MultiSynth divider shown in Figure 6 switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error.

To eliminate phase error generated by this process, the MultiSynth block calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance.

This architecture allows the output of each MultiSynth to produce any frequency from 5 to F_{vco}/8 MHz. To support higher frequency operation, the MultiSynth divider can be bypassed. In bypass mode, integer divide ratios of 4 and 6 are supported. This allows for output frequencies of F_{vco}/4 and F_{vco}/6 MHz, which translates to 367–473.33 MHz and 550–710 MHz respectively. Because each MultiSynth uses the same VCO output, there are output frequency limitations when output frequencies greater than F_{vco}/8 are desired.

For example, if 375 MHz is needed at the output of MultiSynth0, the VCO frequency would need to be 2.25 GHz. Now, all the other MultiSynths can produce any frequency from 5 MHz up to a maximum frequency of 2250/8 = 281.25 MHz. MultiSynth1,2,3 could also produce F_{vco}/4 = 562.5 MHz or F_{vco}/6 = 375 MHz. Only two unique frequencies above F_{vco}/8 can be output: F_{vco}/6 and F_{vco}/4.

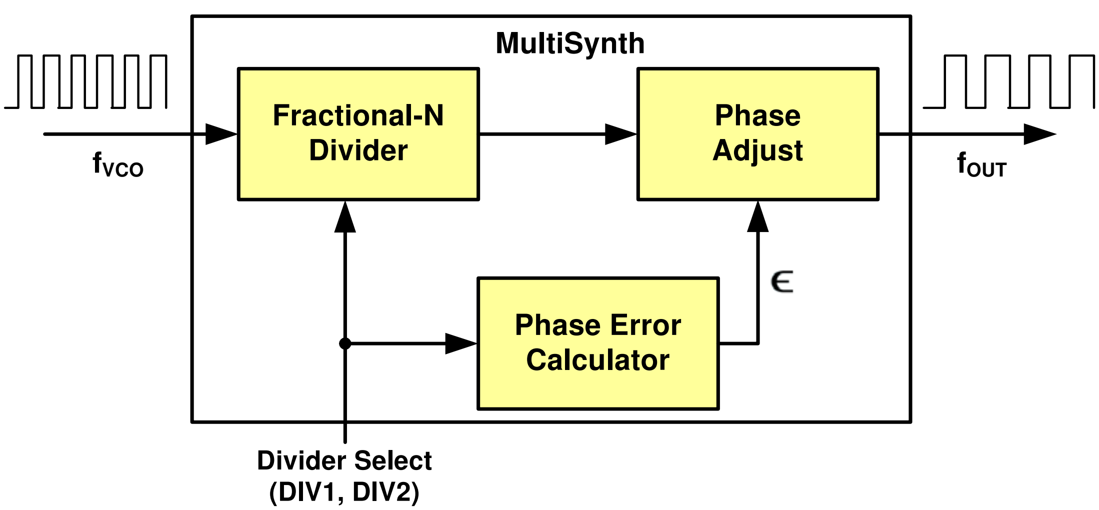


Figure 6. Silicon Labs' MultiSynth Technology

3.4. Output Stage

The output stage consists of output selectors, output dividers, and programmable output drivers as shown in Figure 7.

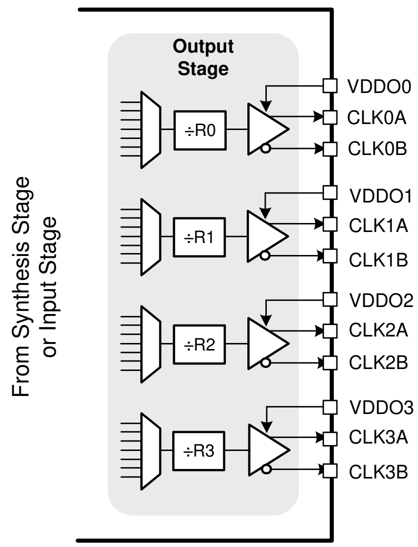


Figure 7. Output Stage

The output selectors select the clock source for the output drivers. By default, each output driver is connected to its own MultiSynth block (e.g. MS0 to CLK0, MS1 to CLK1, etc), but other combinations are possible by reconfiguring the device. The PLL can be bypassed by connecting the input stage signals (osc, ref, refdiv, fb, or fbdiv) directly to the output divider. Bypassing an input directly to an output will not allow phase alignment of that output to other outputs. Each of the output drivers can also connect to the first MultiSynth block (MS0) enabling a fan-out function. This allows the Si5338 to act as a clock generator, a fanout buffer, or a combination of both in the same package.

The output dividers (R0, R1, R2, R3) allow another stage of clock division.These dividers are configurable as divide by 1 (default), 2, 4, 8, 16, or 32. When an Rn does not equal 1, the phase alignment function for that output will not work.

The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, CMOS, HSTL, and SSTL. Separate output supply pins ($VDDO_n$) are provided for each output buffer.

The voltage on these supply pins can be 3.3, 2.5, 1.8, or 1.5 V as needed for the possible output formats. Additionally, the outputs can be configured to stop high, low, or tri-state when the PLL has lost lock. If the Si5338 is used in a zero delay mode, the output that is fed back must be set for always on, which will override any output disable signal.

Each of the outputs can also be enabled or disabled through the I^2C port. A single pin to enable/disable all outputs is available in the Si5338K/L/M.

3.5. Configuring the Si5338

The Si5338 is a highly-flexible clock generator that is entirely configurable through its I^2C interface. The device's default configuration is stored in non-volatile memory (NVM) as shown in Figure 8. The NVM is a one-time programmable memory (OTP), which can store a custom user configuration at power-up. This is a useful feature for applications that need a clock present at power-up (e.g., for providing a clock to a processor).

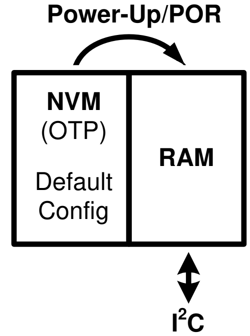


Figure 8. Si5338 Memory Configuration

During a power cycle or a power-on reset (POR), the contents of the NVM are copied into random access memory (RAM), which sets the device configuration that will be used during operation. Any changes to the device configuration after power-up are made by reading and writing to registers in the RAM space through the I^2C interface. ClockBuilder Desktop (see "3.1.1. ClockBuilder™ Desktop Software" on page 18) can be used to easily configure register map files that can be written into RAM (see "3.5.2. Creating a New Configuration for RAM" for details). Alternatively, the register map file can be created manually with the help of the equations in the Si5338 Reference Manual.

Two versions of the Si5338 are available. First, standard, non-customized Si5338 devices are available in which the RAM can be configured in-circuit via I^2C (example part number Si5338C-A-GM). Alternatively, standard Si5338 devices can be field-programmed using the Si5338/56-PROG-EVB field programmer. Second, custom factory-programmed Si5338 devices are available that include a user-specified startup frequency configuration (example part number Si5338C-Axxxxx-GM). See "12. Ordering Information" on page 42 for details.

3.5.1. Ordering a Custom NVM Configuration

The Si5338 is orderable with a factory-programmed custom NVM configuration. This is the simplest way of using the Si5338 since it generates the desired output frequencies at power-up or after a power-on reset (POR). This default configuration can be reconfigured in RAM through the I^2C interface after power-up (see “3.5.2. Creating a New Configuration for RAM”).

Custom 7-bit I^2C addresses may also be requested. Note that for the A/B/C devices, the I^2C LS bit address is the logical “or” of the I^2C address LS bit in Register 27 and the state of the I2C_LSB pin. If I2C_LSB pin functionality is required, custom I^2C addresses may only be even numbers. For all other variants of the device, custom I^2C addresses may be even or odd numbers. See the Si5338 Reference Manual: Configuring the Si5338 without ClockBuilder Desktop for more details.

The first step in ordering a custom device is generating an NVM file which defines the input and output clock frequencies and signal formats. This is easily done using the ClockBuilder Desktop software (see "3.1.1. ClockBuilder™ Desktop Software" on page 18). This GUI based software generates an NVM file, which is used by the factory to manufacture custom parts. Each custom part is marked with a unique part number identifying the specific configuration (e.g., Si5338C-A00100-GM). Consult your local sales representative for more details on ordering a custom Si5338.

3.5.2. Creating a New Configuration for RAM

Any Si5338 device can be configured by writing to registers in RAM through the I^2C interface. A non-factory programmed device must be configured in this manner.

The first step is to determine all the register values for the required configuration. This can be accomplished by one of two methods.

1. Create a device configuration (register map) using ClockBuilder Desktop (v3.0 or later; see "3.1.1. ClockBuilder™ Desktop Software" on page 18).
    a. Configure the frequency plan.
    b. Configure the output driver format and supply voltage.
    c. Configure frequency and/or phase inc/dec (if desired).
    d. Configure spread spectrum (if desired).
    e. Configure for zero-delay mode (if desired, see "3.10.6. Zero-Delay Mode" on page 28).
    f. If needed go to the Advanced tab and make additional configurations.
    g. Save the configuration using the Options > Save Register Map File or Options > Save C code Header.
2. Create a device configuration, register by register, using the Si5338 Reference Manual.

3.5.3. Writing a Custom Configuration to RAM

Writing a new configuration (register map) to the RAM consists of pausing the LOL state-machine, writing new values to the IC accounting for the write-allowed mask (see the Si5338 Reference Manual, “10. Si5338 Registers”), validating the input clock or crystal, locking the PLL to the input with the new configuration, restarting the LOL state-machine, and calibrating the VCO for robust operation across temperature. The flow chart in Figure 9 enumerates the details:

Note: The write-allowed mask specifies which bits must be read and modified before writing the entire register byte (a.k.a. read-modify-write). “AN428: Jump Start: In-System, Flash-Based Programming for Silicon Labs’ Timing Products” illustrates the procedure defined in Section 3.5.2 with ANSI C code.

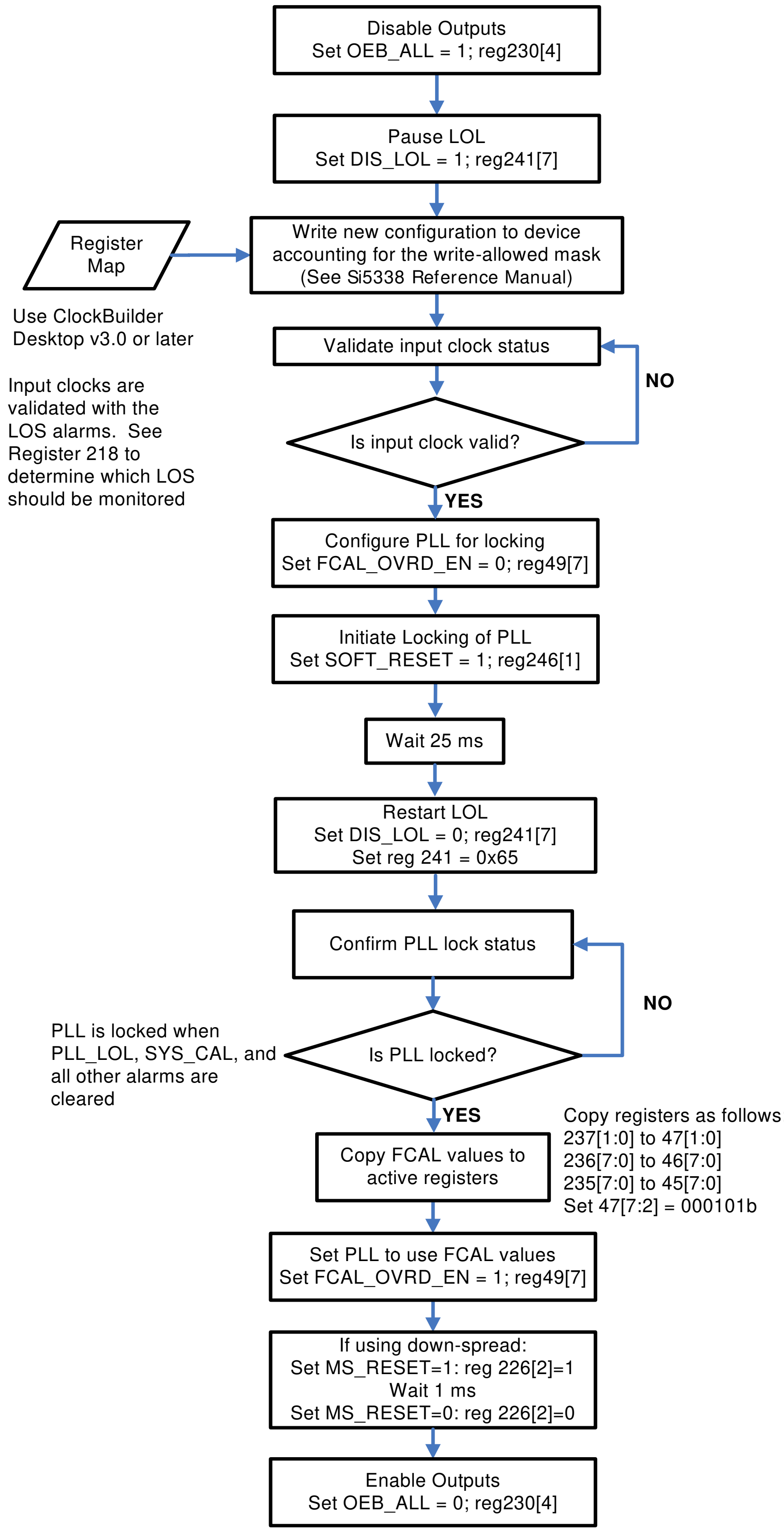


Figure 9. I²C Programming Procedure

3.5.4. Writing a Custom Configuration to NVM

An alternative to ordering an Si5338 with a custom NVM configuration is to use the field programming kit (Si5338/56-PROG-EVB) to write directly to the NVM of a “blank” Si5338. Since NVM is an OTP memory, it can only be written once. The default configuration can be reconfigured by writing to RAM through the I^2C interface (see “3.5.2. Creating a New Configuration for RAM”).

3.6. Status Indicators

A logic-high interrupt pin (INTR) is available to indicate a loss of signal (LOS) condition, a PLL loss of lock (PLL_LOL) condition, or that the PLL is in process of acquiring lock (SYS_CAL). PLL_LOL is held high when the input frequency drifts beyond the PLL tracking range. It is held low during all other times and during a POR or soft_reset. SYS_CAL is held high during a POR or SOFT reset so that no chattering occurs during the locking process. As shown in Figure 10, a status register at address 218 is available to help identify the exact event that caused the interrupt pin to become active. Register 247 is the sticky version of Register 218, and Register 6 is the interrupt mask for Register 218.

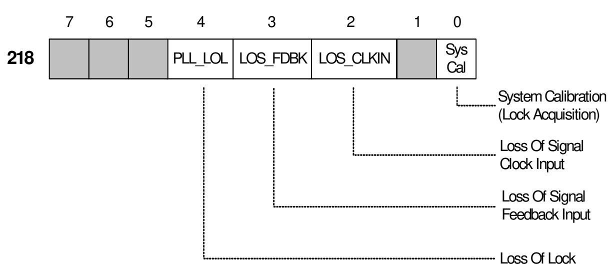


Figure 10. Status Register

Figure 11 shows a typical connection with the required pull-up resistor to VDD.

3.6.1. Using the INTR Pin in Systems with I^2C

The INTR output pin is not latched and thus it should not be a polled input to an MCU but an edge-triggered interrupt. An MCU can process an interrupt event by reading the sticky register 247 to see what event caused the interrupt. The same register can be cleared by writing zeros to the bits that were set. Individual interrupt bits can be masked by register 6[4:0].

3.6.2. Using the INTR Pin in Systems without I^2C

The INTR pin also provides a useful function in systems that require a pin-controlled fault indicator. Pre-setting the interrupt mask register allows the INTR pin to become an indicator for a specific event, such as LOS and/or LOL. Therefore, the INTR pin can be used to indicate a single fault event or even multiple events.

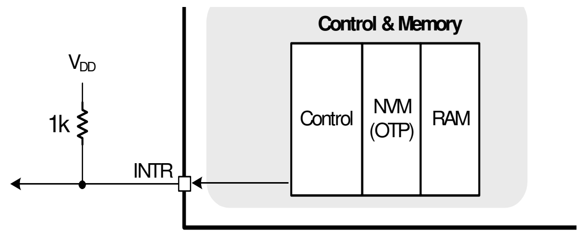


Figure 11. INTR Pin with Required Pull-Up

3.7. Output Enable

There are two methods of enabling and disabling the output drivers: Pin control, and I^2C control.

3.7.1. Enabling Outputs Using Pin Control

The Si5338K/L/M devices provide an Output Enable pin (OEB) as shown in Figure 12. Pulling this pin high will turn all outputs off. The state of the individual drivers when turned off is controllable. If an individual output is set to always on, then the OEB pin will not have an effect on that driver. Drive state options and always on are explained in “3.7.2. Enabling Outputs through the I^2C Interface”.

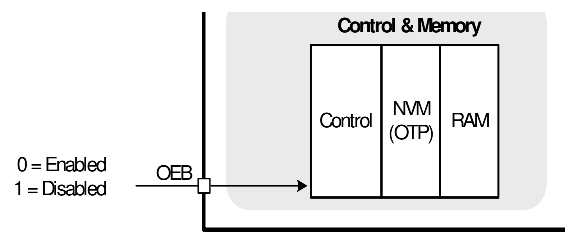


Figure 12. Output Enable Pin (Si5338K/L/M)

3.7.2. Enabling Outputs through the I^2C Interface

Output enable can be controlled through the I^2C interface. As shown in Figure 13, register 230[3:0] allows control of each individual output driver. Register 230[4] controls all drivers at once. When register 230[4] is set to disable all outputs, the individual output enables will have no effect. Registers 110[7:6], 114[7:6], 118[7:6], and 112[7:6] control the output disabled state as tri-state, low, high, or always on. If always on is set, that output will always be on regardless of any other register or chip state. In addition, the always on mode must be selected for an output that is fed back in a Zero Delay application.

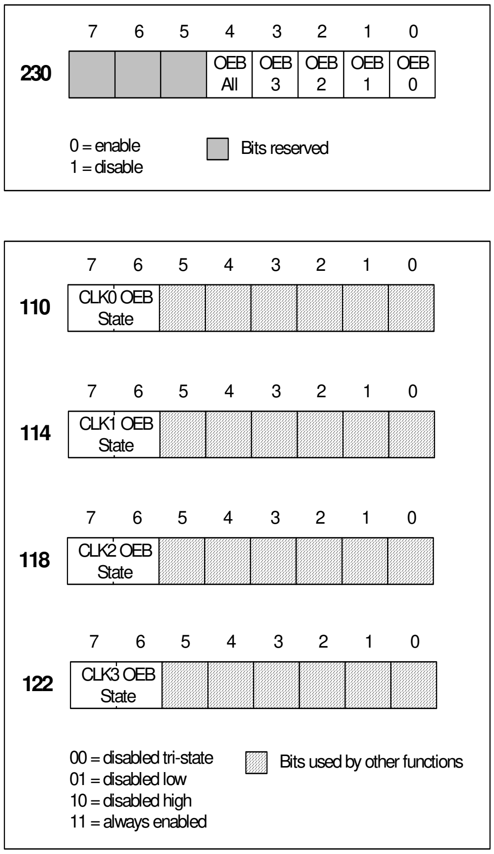


Figure 13. Output Enable Control Registers

3.8. Power Consumption

The Si5338 Power consumption is a function of

- Supply voltage
- Frequency of output Clocks
- Number of output Clocks
- Format of output Clocks

Because of internal voltage regulation, the current from the core V_{DD} is independent of the V_{DD} voltage and hence the plot shown in Figure 14 can be used to estimate the V_{DD} core (pins 7 and 24) current.

The current from the output supply voltages can be estimated from the values provided in Table 3, “DC Characteristics,” on page 5. To get the most accurate value for V_{DD} currents, the Si5338-EVB with Clockbuilder software should be used. To do this, go to the “Power” tab of the Clockbuilder and press “Measure”. In this manner, a specific configuration can be implemented on the EVB and the actual current for each supply voltage measured. When doing this it is critical that the output drivers have the proper load impedance for the selected format.

When testing for output driver current with HSTL and SSTL, it is required to have load circuitry as shown in “AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers”. The Si5338 EVB has layout pads that can be used for this purpose. When testing for output driver current with LVPECL the same layout pads can be used to implement the LVPECL bias resistor of 130 Ω (2.5 V VDDx) or 200 Ω (3.3 V VDDx). See the schematic in the Si5338-EVB data sheet and AN408 for additional information.