Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

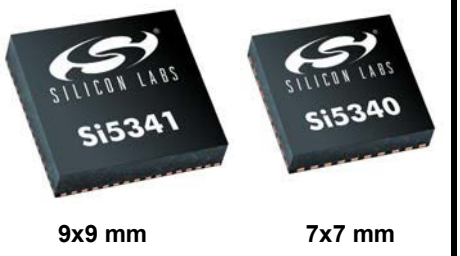
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Si5341/40

Low-Jitter, 10-Output, Any-Frequency, Any-Output Clock Generator

Features

- Generates up to 10 independent output clocks
- Ultra-low jitter: <100 fs RMS typical
- MultiSynth™ technology enables any-frequency synthesis on any-output
- Highly configurable outputs compatible with LVDS, LVPECL, CML, LVCMOS, HCSL, or programmable voltage
- Input frequency range:
  - External crystal: 25, 48-54 MHz
  - Differential clock: 10 to 750 MHz
  - LVCMOS clock: 10 to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 712.5 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Output-output skew: 20 ps typ
- Adjustable output-output delay
- Optional zero delay mode
- Independent glitchless on-the-fly output frequency changes
- DCO mode with frequency steps as low as 0.001 ppb
- Independent output clock supply pins: 3.3 V, 2.5 V, or 1.8 V
- Built-in power supply filtering and regulation
- Status monitoring: LOS, LOL
- Serial Interface: I^2C or SPI (3-wire or 4-wire)
- User programmable (2x) non-volatile OTP memory
- ClockBuilder™ Pro software utility simplifies device configuration and assigns customer part numbers
- **Si5341**: 4 input, 10 output, compact 9x9 mm, 64 QFN
- **Si5340**: 4 input, 4 output, compact 7x7 mm, 44 QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant



9x9 mm **7x7 mm**

Ordering Information

See Section 8.

Device Selector Guide

Grade	Max Output Frequency	Frequency Synthesis Mode
Si534xA	712.5 MHz	Integer + Fractional
Si534xB	350 MHz	
Si534xC	712.5 MHz	Integer Only
Si534xD	350 MHz	

Applications

- Clock tree generation replacing XOs, buffers, signal format translators
- Any-frequency clock translation
- Clocking for FPGAs, processors, memory
- Ethernet switches/routers
- OTN framers/mappers/processors
- Test equipment & instrumentation
- Broadcast video

Description

The any-frequency, any-output Si5341/40 clock generators combine a wide-band PLL with proprietary MultiSynth fractional synthesizer technology to offer a versatile and high performance clock generator platform. This highly flexible architecture is capable of synthesizing a wide range of integer and non-integer related frequencies up to 712.5 MHz on 10 differential clock outputs while delivering sub-100 fs rms phase jitter performance with 0 ppm error. Each of the clock outputs can be assigned its own format and output voltage enabling the Si5341/40 to replace multiple clock ICs and oscillators with a single device making it a true “clock tree on a chip”.

The Si5341/40 can be quickly and easily configured using ClockBuilder Pro software. Custom part numbers are automatically assigned using a ClockBuilder Pro for fast, free, and easy factory pre-programming, or the Si5341/40 can be programmed in-circuit via I^2C and SPI serial interfaces.

Functional Block Diagram

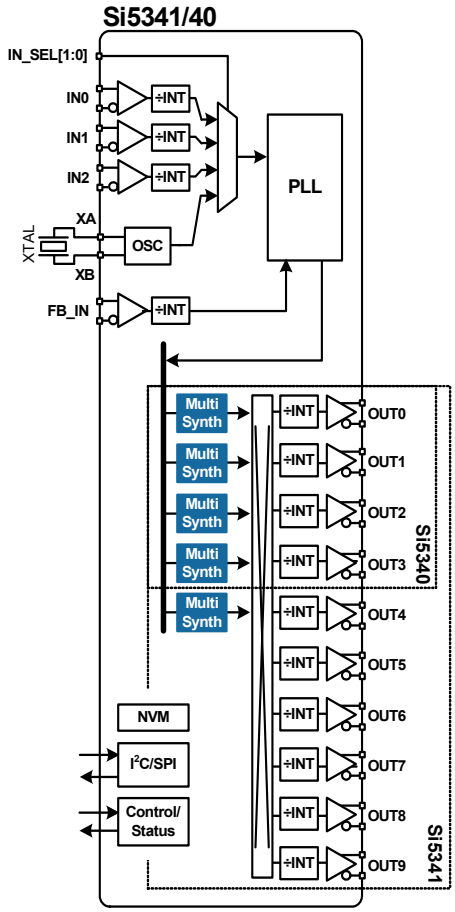
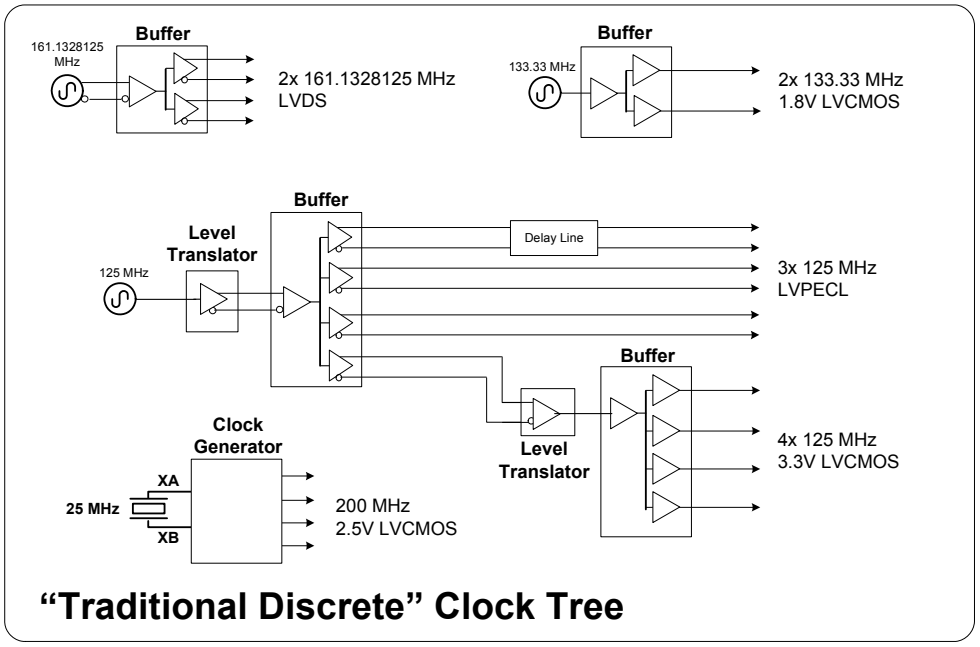


TABLE OF CONTENTS

1. Typical Application Schematic



One Si5341 replaces:
- 3x crystal oscillators (XO)
- 2x buffers
- 1x Clock Generator
- 2x level translators
- 1x delay line

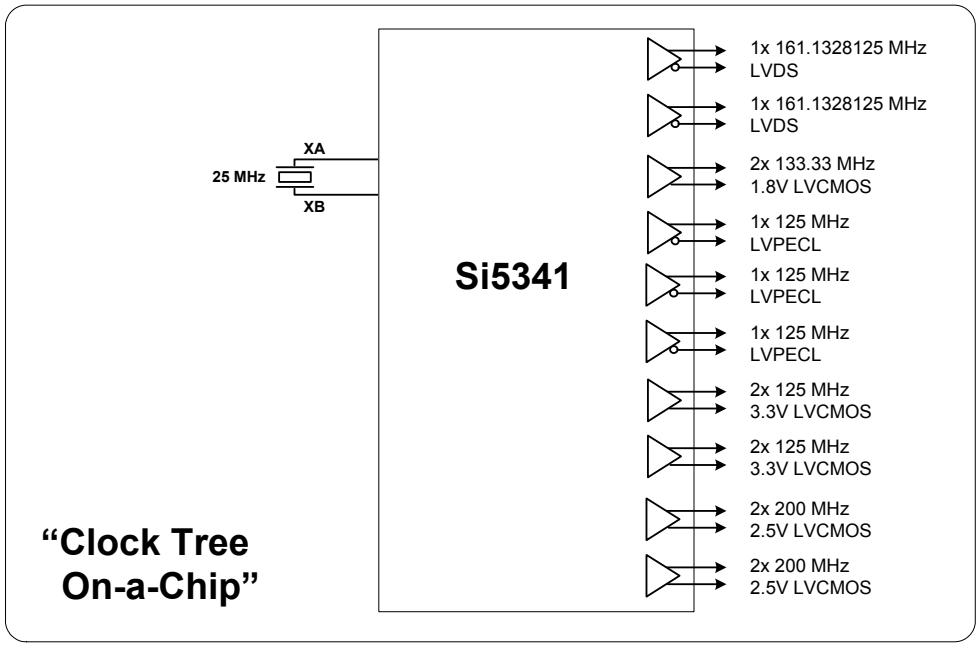


Figure 1. Using The Si5341 to Replace a Traditional Clock Tree

2. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.					

Table 2. DC Characteristics

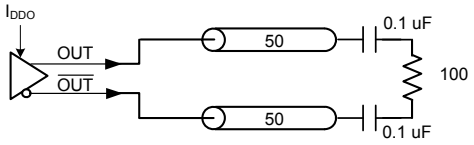
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}	Si5341	Note [1]	—	100	150	mA
		Si5340	Note [2]	—	85	130	mA
	I_{DDA}	Si5341	Note [1]	—	115	125	mA
		Si5340	Note [2]	—	115	125	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[3] @ 156.25 MHz		—	21	25	mA
		LVDS Output[3] @ 156.25 MHz		—	15	18	mA
		3.3 V LVCMOS[4] output @ 156.25 MHz		—	21	25	mA
		2.5 V LVCMOS[4] output @ 156.25 MHz		—	16	18	mA
		1.8 V LVCMOS[4] output @ 156.25 MHz		—	12	13	mA
Total Power Dissipation	P_d	Si5341	Notes [1,5]	—	830	980	mW
		Si5340	Notes [2,5]	—	685	815	mW

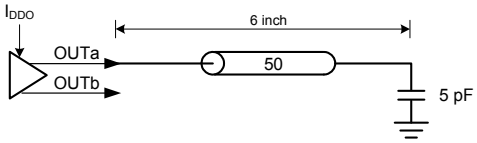
Notes:

1. Si5341 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5340 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an ac-coupled 100 Ω load.
4. LVCMOS outputs measured into a 6-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV=3, which is the strongest driver setting. Refer to the Si5341/40 Family Reference Manual for more details on register settings.

Differential Output Test Configuration



LVCMOS Output Test Configuration



5. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential or Single-Ended/LVCMOS — AC-Coupled (IN0/$\overline{IN0}$, IN1/$\overline{IN1}$, IN2/$\overline{IN2}$, FB_IN/$\overline{FB\_IN}$)						
Input Frequency Range	f_{IN}	Differential	10	—	750	MHz
		Single-ended/LVCMOS	10	—	250	
Input Voltage Swing[5]	V_{IN}	Differential AC Coupled fin < 250 MHz	100	—	1800	mVpp_se
		Differential AC Coupled 250 MHz < fin < 750 MHz	225	—	1800	mVpp_se
		Single-ended AC Coupled fin < 250 MHz	100	—	3600	mVpp_se
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
DC-Coupled CMOS Input Buffer (IN0, IN1, IN2)[4]						
Input Frequency	f_{IN}		10	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.33	V
	V_{IH}		0.49	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC	Clock Input	40	—	60	%
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
Differential or Single-Ended/LVCMOS Clock at XA/XB						
Input Frequency Range	f_{IN}	Frequency range for best output jitter performance	48	—	200	MHz
			10	—	200	MHz
Input Single-ended Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) * V_{IN\_Vpp\_se}) / SR$.
3. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.
4. DC-coupled CMOS Input Buffer selection is not supported in ClockBuilder Pro for new designs. For single-ended LVCMOS inputs to IN0,1,2 it is required to ac-couple into the differential input buffer.
5. Voltage swing is specified as single-ended mVpp.

6. Contact Silicon Labs Technical Support for more details.

Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Differential Voltage Swing	V_{IN_DIFF}		365	—	2500	mVpp_diff
Slew rate[1, 2]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) * V_{IN\_Vpp\_se}) / SR$.
3. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.
4. DC-coupled CMOS Input Buffer selection is not supported in ClockBuilder Pro for new designs. For single-ended LVCMOS inputs to IN0,1,2 it is required to ac-couple into the differential input buffer.
5. Voltage swing is specified as single-ended mVpp.

6. Contact Silicon Labs Technical Support for more details.

Table 4. Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5341 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{RST}$, $\overline{OE}$, $\overline{SYNC}$, A1, SCLK, A0/$\overline{CS}$, FINC, FDEC, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	$0.3xV_{DDIO}$*	V
	V_{IH}		$0.7xV_{DDIO}$*	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	T_{PW}	$\overline{RST}$, $\overline{SYNC}$, FINC, and FDEC	100	—	—	ns
Frequency Update Rate	F_{UR}	FINC and FDEC	—	—	1	MHz
Si5340 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{RST}$, $\overline{OE}$, A1, SDA, SDI, SCLK, A0/$\overline{CS}$, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	$0.3xV_{DDIO}$*	V
	V_{IH}		$0.7xV_{DDIO}$*	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	T_{PW}	$\overline{RST}$ only	100	—	—	ns

***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. Refer to the Reference Manual for more details on register settings.

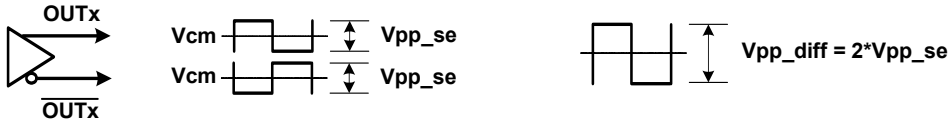
Table 5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f_{OUT}			0.0001	—	712.5	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 712.5 MHz		45	—	55	%
Output-Output Skew	T_{SK}	Outputs on same Multisynth, Normal Mode		—	20	50	ps
		Outputs on same Multisynth, Pow Power Mode		—	20	100	ps
OUT-$\overline{OUT}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	100	ps
Output Amplitude[1, 5]	**Normal Mode**						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	470	550	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	660	810	1000	
	Low Power Mode						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	300	420	530	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	620	820	1060	

Notes:

1. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. For normal and low-power modes, the amplitudes are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. See Appendix A of the Si5341/40 Reference Manual.
2. Driver output impedance depends on selected output mode (Normal, Low Power).
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.



4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems”, guidance on crosstalk minimization.
5. For other amplitudes see Appendix A of the Si5341/40 Reference Manual.
6. See Note 4, but in this case the measurement is across two output clocks that have a single clock between them.
7. Same as Note 4, but the Si5340 has less crosstalk due to the spacing of adjacent outputs.

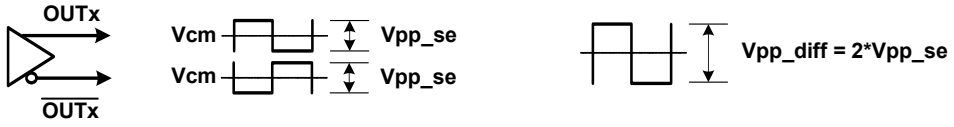
Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Common Mode Voltage[1]	**Normal Mode or Low Power Modes**						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.25	1.35	V
			LVPECL	1.90	2.05	2.15	
		V_{DDO} = 2.5 V	LVPECL LVDS	1.15	1.25	1.35	
		V_{DDO} = 1.8 V	Sub-LVDS	0.87	0.93	1.0	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Mode		—	170	240	ps
		Low Power Mode		—	300	430	
Differential Output Impedance[2]	Z_O	Normal Mode		—	100	—	Ω
		Low Power Mode		—	650	—	Ω
Power Supply Noise Rejection[3]	PSRR	**Normal Mode**					
		10 kHz sinusoidal noise		—	–93	—	dBc
		100 kHz sinusoidal noise		—	–93	—	
		500 kHz sinusoidal noise		—	–84	—	
		1 MHz sinusoidal noise		—	–79	—	
		Low Power Mode					
		10 kHz sinusoidal noise		—	–98	—	dBc
		100 kHz sinusoidal noise		—	–95	—	
		500 kHz sinusoidal noise		—	–84	—	
		1 MHz sinusoidal noise		—	–76	—	

Notes:

1. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. For normal and low-power modes, the amplitudes are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. See Appendix A of the Si5341/40 Reference Manual.
2. Driver output impedance depends on selected output mode (Normal, Low Power).
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.



4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems”, guidance on crosstalk minimization.
5. For other amplitudes see Appendix A of the Si5341/40 Reference Manual.
6. See Note 4, but in this case the measurement is across two output clocks that have a single clock between them.
7. Same as Note 4, but the Si5340 has less crosstalk due to the spacing of adjacent outputs.

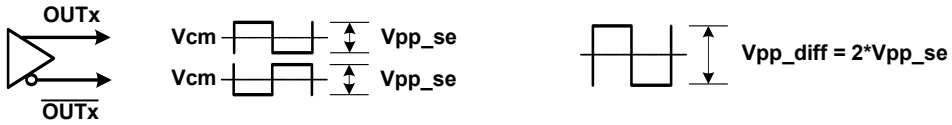
Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output-Output Crosstalk	XTALK	Si5341	Note [4]	—	–75	—	dBc
		Si5341	Note [6]	—	–85	—	dBc
		Si5340	Note [7]	—	–85	—	dBc

Notes:

1. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. For normal and low-power modes, the amplitudes are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. See Appendix A of the Si5341/40 Reference Manual.
2. Driver output impedance depends on selected output mode (Normal, Low Power).
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.



4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems”, guidance on crosstalk minimization.
5. For other amplitudes see Appendix A of the Si5341/40 Reference Manual.
6. See Note 4, but in this case the measurement is across two output clocks that have a single clock between them.
7. Same as Note 4, but the Si5340 has less crosstalk due to the spacing of adjacent outputs.

Table 6. Output Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5341 Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{INTR}}$), SDA/SDIO[2], SDO						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[1] x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[1] x 0.15	V
Si5340 Status Output Pins ($\overline{\text{INTR}}$), $\overline{\text{LOL}}$, $\overline{\text{LOS\_XAXB}}$, SDA/SDIO[2], SDO						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[1] x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[1] x 0.15	V

Notes:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. Refer to the Reference Manual for more details on register settings.
2. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high. V_{OL} remains valid in all cases.

Table 7. LVCMOS Clock Output Specifications

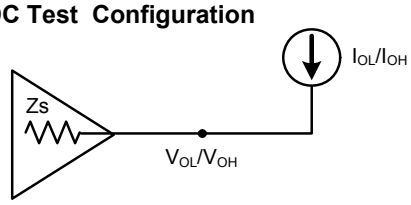
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency				0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} < 100 MHz		47	—	53	%
		100 MHz < f_{OUT} < 250 MHz		44	—	55	
Output-to-Output Skew	T_{SK}			—	—	100	ps
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OH} = –10 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OH} = –6 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OH} = –4 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=3	I_{OH} = –5 mA		—	—	

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



AC Test Configuration

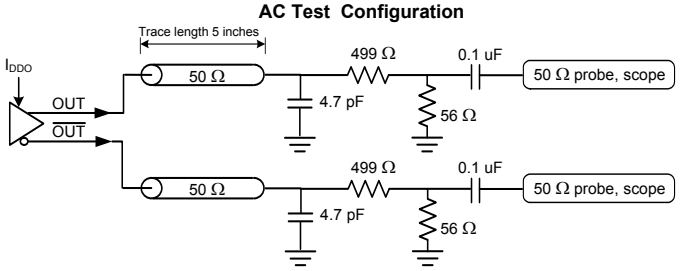


Table 7. LVCMOS Clock Output Specifications (Continued)

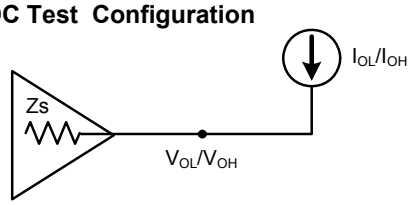
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3V		—	420	550	ps
		VDDO = 2.5 V		—	475	625	ps
		VDDO = 1.8 V		—	525	705	ps

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



AC Test Configuration

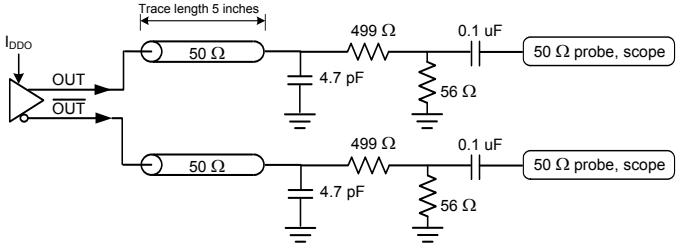


Table 8. Performance Characteristics
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{CO} Frequency Range	F_{VCO}		13.5	—	14.256	GHz
PLL Loop Bandwidth	f_{BW}		—	1.0	—	MHz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates clocks (Input Frequency > 48 MHz)	—	30	45	ms
POR[1] to Serial Interface Ready	t_{RDY}		—	—	15	ms
PLL Lock Time[6]	t_{ACQ}	f_{IN} = 19.44 MHz	22	—	180	ms
Output Delay Adjustment	t_{DELAY_frac}	f_{VCO} = 14 GHz Delay is controlled by the Multi-Synth	—	0.28	—	ps
	t_{DELAY_int}		—	71.4	—	ps
	t_{RANGE}		—	±9.14	—	ns
Jitter Generation Locked to External Clock[2]	J_{GEN}	Integer Mode[3] 12 kHz to 20 MHz	—	0.135	0.175	ps RMS
		Fractional/DCO Mode[4] 12 kHz to 20 MHz	—	0.160	0.205	ps RMS
	J_{PER}	Derived from integrated phase noise	—	0.140	—	ps pk-pk
	J_{CC}		—	0.250	—	ps pk
	J_{PER}	N = 10,000 cycles Integer or Fractional Mode[3,4]. Measured in the time domain. Performance is limited by the noise floor of the equipment.	—	7.3	—	ps pk-pk
	J_{CC}		—	8.1	—	ps pk

Notes:
1. Measured as time from valid V_{DD} and V_{DD33} rails (90% of their value) to when the serial interface is ready to respond to commands. Measured in SPI 4-wire mode, with SCLK @ 10 MHz.
2. Jitter generation test conditions f_{IN} = 100 MHz, f_{OUT} = 156.25 MHz LVPECL.
3. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.
4. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer.
5. Initiate a soft reset command to align the outputs to within +/- 100 ps.
6. PLL lock time is measured by first letting the PLL lock, then turning off the input clock, and then turning on the input clock. The time from the first edge of the input clock being re-applied until LOL de-asserts is the PLL lock time.

Table 8. Performance Characteristics (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Jitter Generation Locked to External XTAL	XTAL Frequency = 48 MHz					
	J_{GEN}	Integer Mode[3] 12 kHz to 20 MHz	—	0.090	0.150	ps RMS
		Fractional/DCO Mode[4] 12 kHz to 20 MHz	—	0.120	0.165	ps RMS
	J_{PER}	Derived from integrated phase noise	—	0.150	—	ps pk-pk
	J_{CC}		—	0.270	—	ps pk
	J_{PER}	N = 10, 000 cycles Integer or Fractional Mode[3,4] . Measured in the time domain. Performance is limited by the noise floor of the equipment.	—	7.3	—	ps pk-pk
	J_{CC}		—	7.8	—	ps pk
	XTAL Frequency = 25 MHz					
	J_{GEN}	Integer Mode 12 kHz to 20 MHz		0.125	0.330	ps RMS
		Fractional 12 kHz to 20 MHz		0.170	0.360	ps RMS

Notes:
1. Measured as time from valid V_{DD} and V_{DD33} rails (90% of their value) to when the serial interface is ready to respond to commands. Measured in SPI 4-wire mode, with SCLK @ 10 MHz.
2. Jitter generation test conditions f_{IN} = 100 MHz, f_{OUT} = 156.25 MHz LVPECL.
3. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.
4. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer.
5. Initiate a soft reset command to align the outputs to within +/- 100 ps.
6. PLL lock time is measured by first letting the PLL lock, then turning off the input clock, and then turning on the input clock. The time from the first edge of the input clock being re-applied until LOL de-asserts is the PLL lock time.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Units
			Standard Mode 100 kbps		Fast Mode 400 kbps		
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
Hold Time (Repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_f		—	300	—	300	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

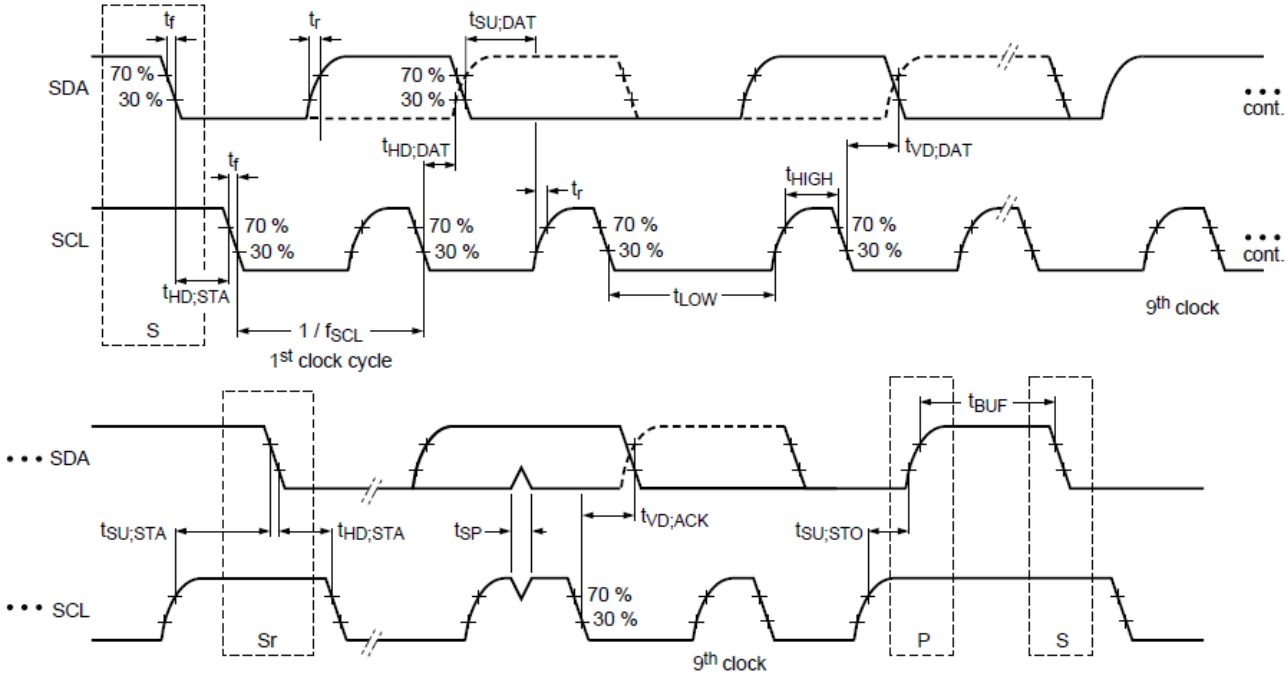


Figure 2. I²C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications (4-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	12.5	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	10	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

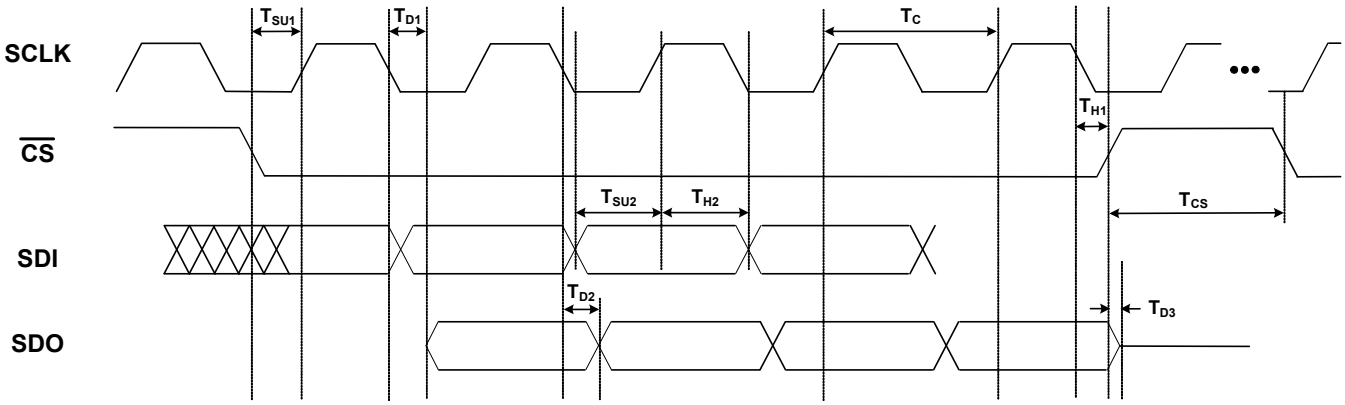


Figure 3. 4-Wire SPI Serial Interface Timing

Table 11. SPI Timing Specifications (3-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	12.5	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	10	15	ns
Delay Time, $\overline{CS}$ Rise to SDIO Tri-State	T_{D3}	—	10	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

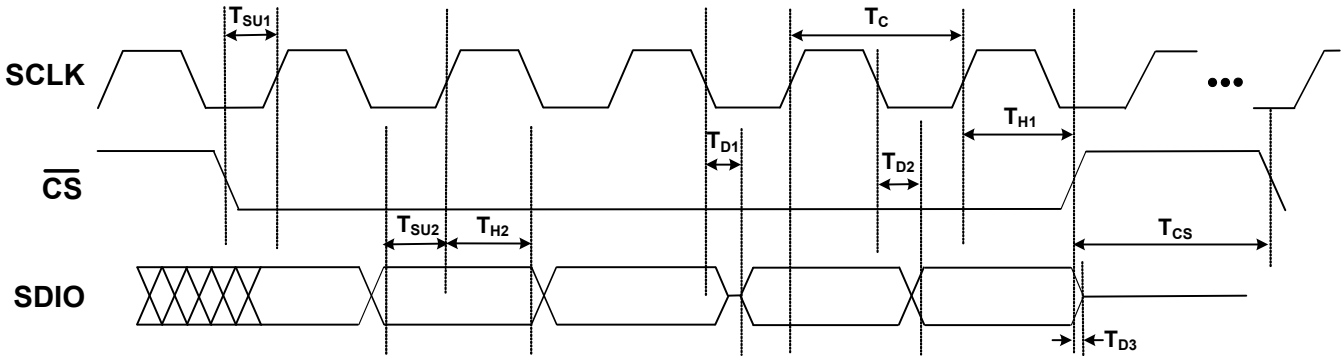


Figure 4. 3-Wire SPI Serial Interface Timing

Table 12. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency Range	$f_{XTAL\_48\text{-}54}$	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	$C_{L\_48\text{-}54}$		—	8	—	pF
Shunt Capacitance	$C_{O\_48\text{-}54}$		—	—	2	pF
Crystal Drive Level	$d_{L\_48\text{-}54}$		—	—	200	µW
Equivalent Series Resistance	$r_{ESR\_48\text{-}54}$	Refer to the Si5341/40 Family Reference Manual to determine ESR.				
Crystal Frequency Range	f_{XTAL_25}		—	25	—	MHz
Load Capacitance	C_{L_25}		—	8	—	pF
Shunt Capacitance	C_{O_25}		—	—	3	pF
Crystal Drive Level	d_{L_25}		—	—	200	µW
Equivalent Series Resistance	r_{ESR_25}	Refer to the Si5341/40 Family Reference Manual to determine ESR				

Notes:
1. The Si5341/40 is designed to work with crystals that meet the specifications in Table 12.
2. Refer to the Si5341/40 Family Reference Manual for recommended 48 to 54 MHz crystals.

Table 13. Thermal Characteristics

Parameter	Symbol	Test Condition*	Value	Units
Si5341 — 64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5340–44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	

***Note:** Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GND pad: 36, Number of Cu Layers: 4

Table 14. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0-IN2, FB_IN	–0.85 to 3.8	V
	V_{I2}	IN_SEL[1:0], $\overline{RST}$, $\overline{OE}$, $\overline{SYNC}$, I2C_SEL, SDI, SCLK, A0/$\overline{CS}$ A1, SDA/SDIO FINC/FDEC	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[4]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20-40	sec

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For MSL and more packaging information, go to www.silabs.com/support/quality/pages/rohsinformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

3. Typical Operating Characteristics

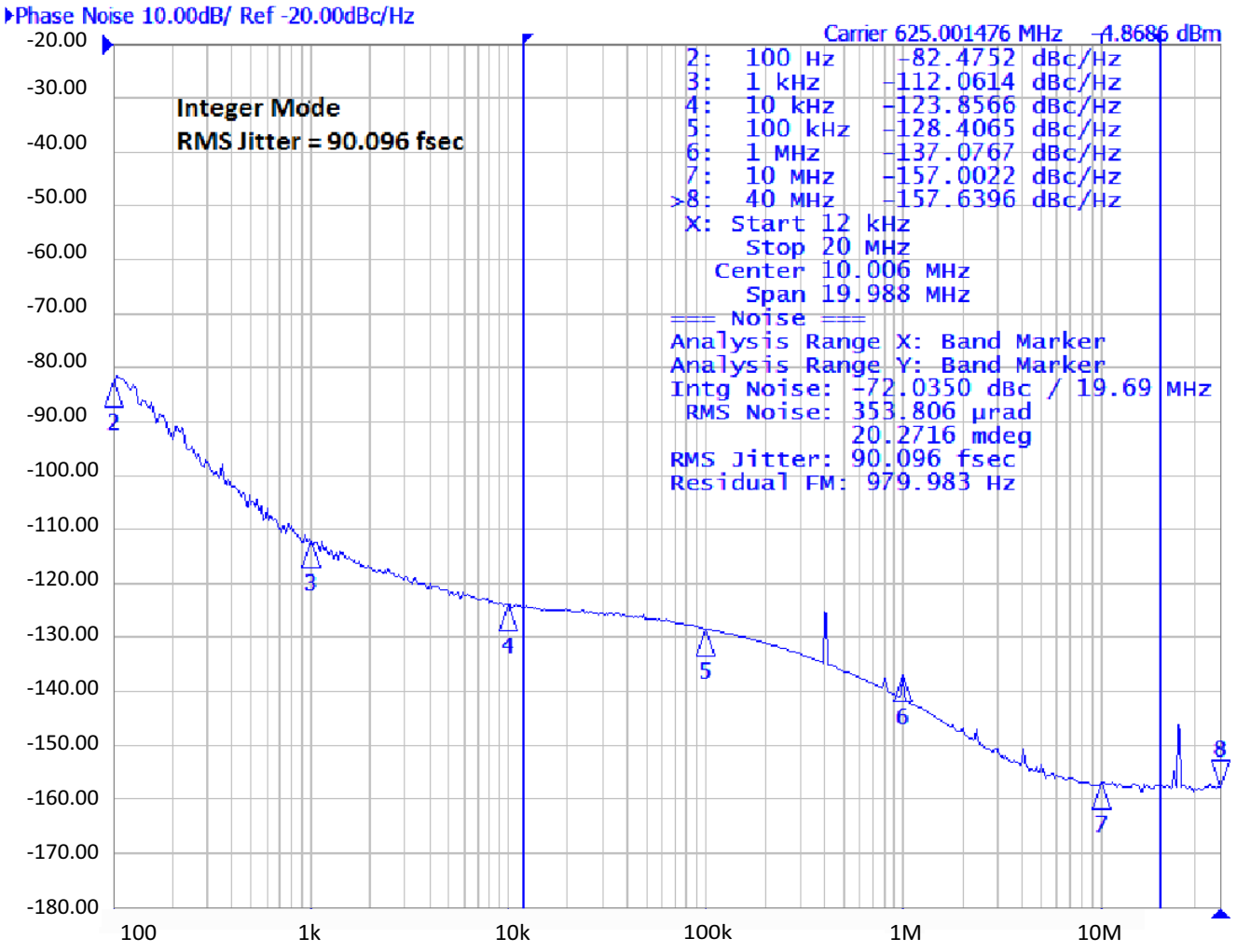


Figure 5. Integer Mode—48 MHz Crystal, 625 MHz Output (2.5 V LVDS)

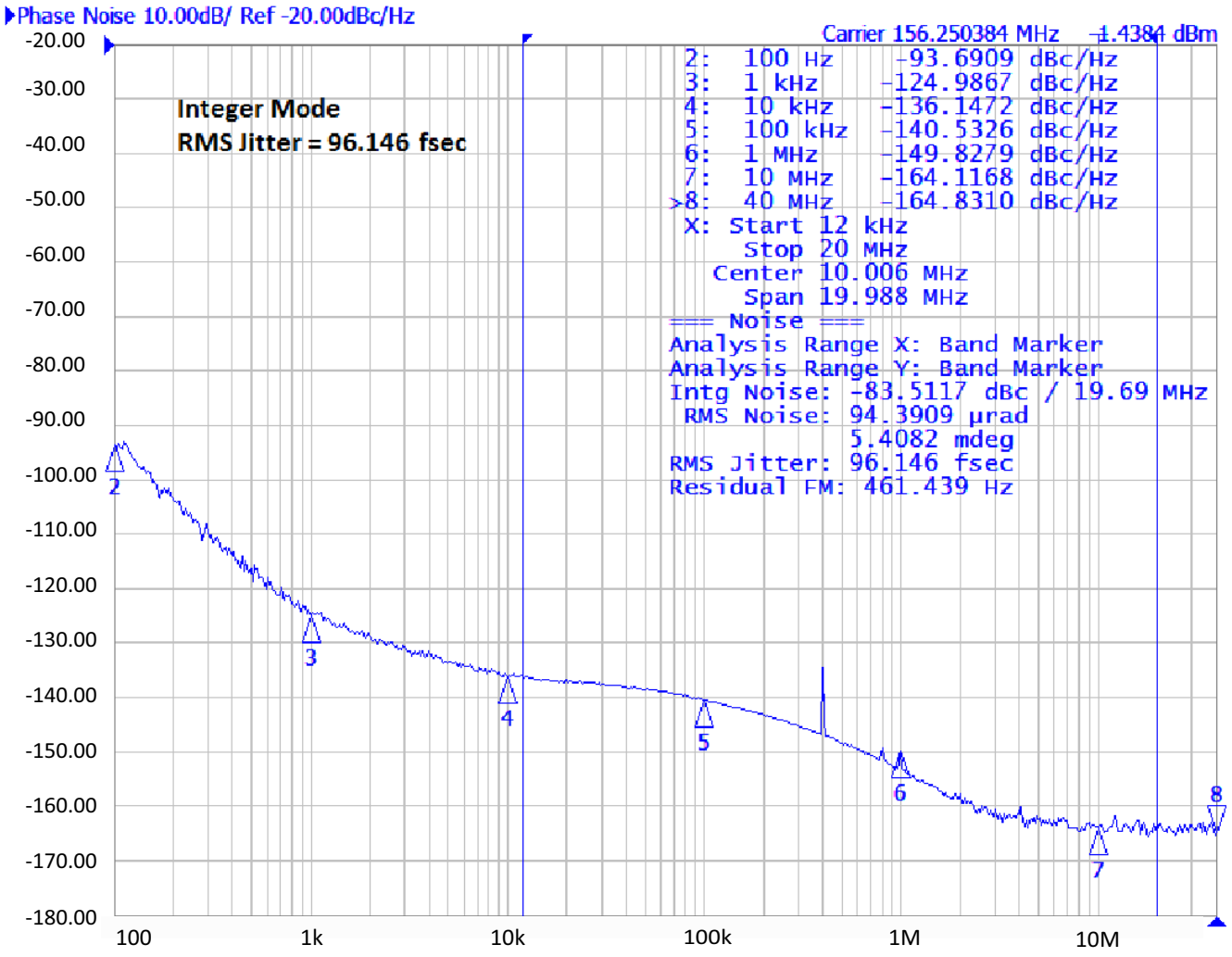


Figure 6. Integer Mode—48 MHz Crystal, 156.25 MHz Output (2.5 V LVDS)

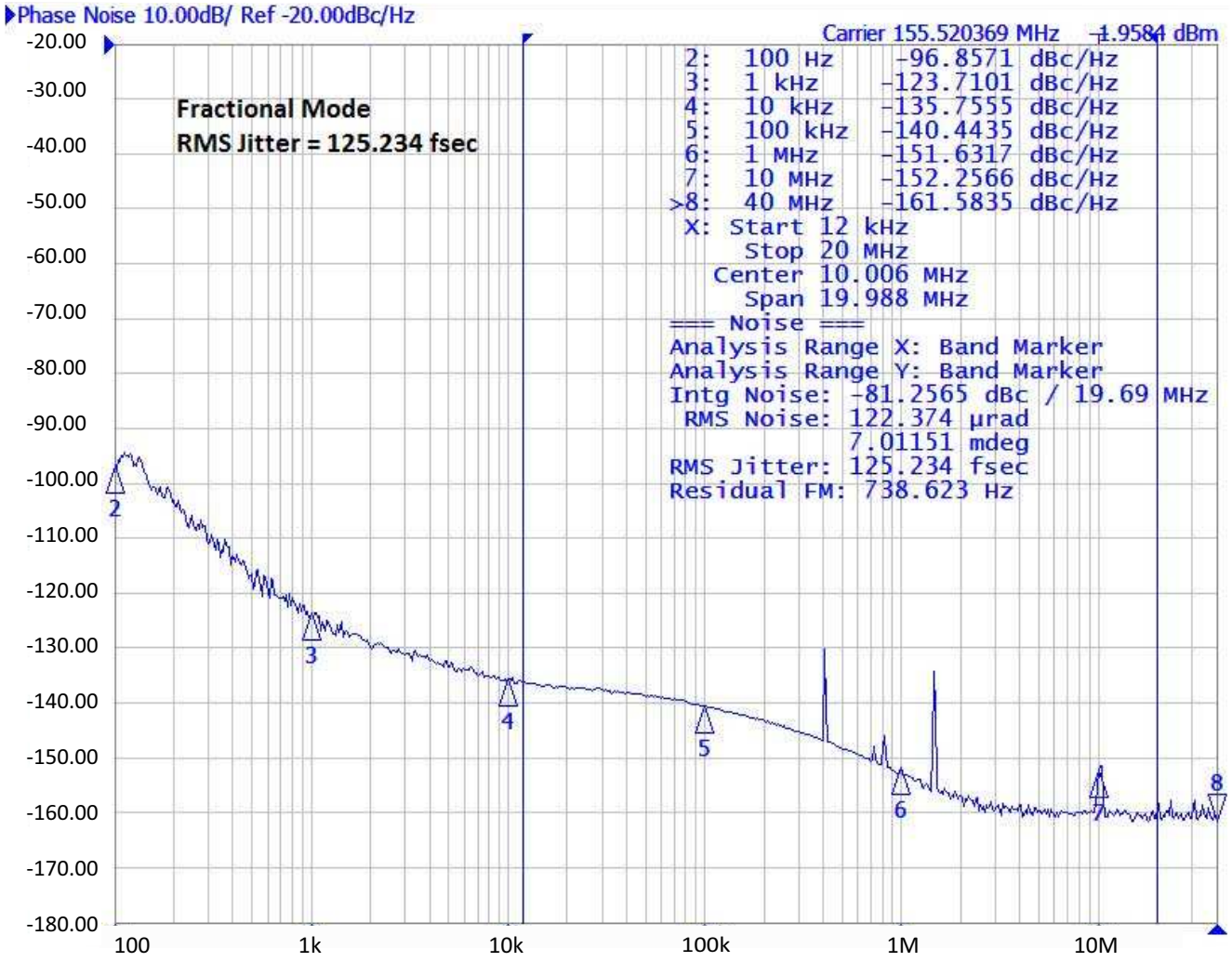


Figure 7. Fractional Mode—48 MHz Crystal, 155.52 MHz Output (2.5 V LVDS)