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Si5345/44/42

10-Channel, Any-Frequency, Any-Output Jitter Attenuator/Clock Multiplier

Features

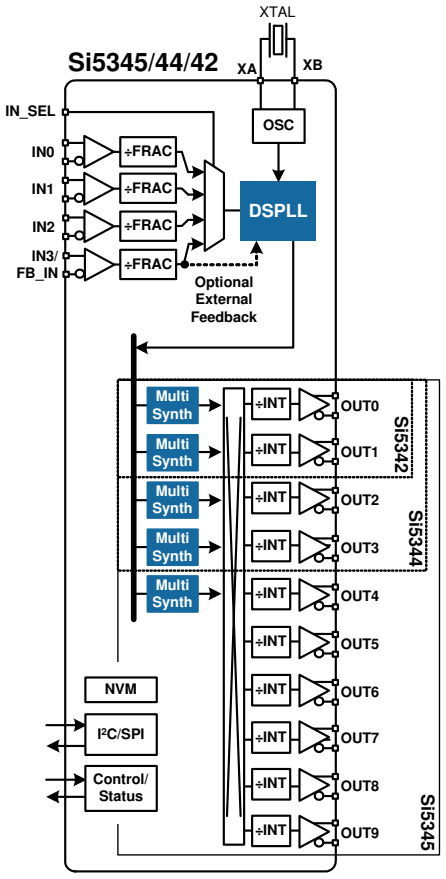
- Generates any combination of output frequencies from any input frequency
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: up to 712.5 MHz
  - LVCMOS: up to 250 MHz
- Ultra-low jitter:
  <100 fs typ (12 kHz–20 MHz)
- Programmable jitter attenuation bandwidth from 0.1 Hz to 4 kHz
- Meets G.8262 EEC Opt 1, 2 (SyncE)
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Locks to gapped clock inputs
- Automatic free-run and holdover modes
- Optional zero delay mode
- Fastlock feature for low nominal bandwidths
- Glitchless on the fly output frequency changes
- DCO mode: as low as 0.001 ppb steps.
- Core voltage
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output clock supply pins: 3.3 V, 2.5 V, or 1.8 V
- Output-output skew: 20 ps typ
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro™ software simplifies device configuration
- Si5345: 4 input, 10 output, 64 QFN
- Si5344: 4 input, 4 output, 44 QFN
- Si5342: 4 input, 2 output, 44 QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

Ordering Information:
See section 8

Device Selector Guide

Grade	Max Output Frequency	Frequency Synthesis Modes
Si534fA	712.5 MHz	Integer+Fractional
Si534fB	350 MHz	Integer+Fractional
Si534fC	712.5 MHz	Integer
Si534fD	350 MHz	Integer

Functional Block Diagram



Applications

- OTN Muxponders and Transponders
- 10/40/100G networking line cards
- GbE/10GbE/100GbE Synchronous Ethernet (ITU-T G.8262)
- Carrier Ethernet switches
- SONET/SDH Line Cards
- Broadcast video
- Test and measurement
- ITU-T G.8262 (SyncE) Compliant

Description

These jitter attenuating clock multipliers combine fourth-generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation and jitter attenuation for applications requiring the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) so they always power up with a known frequency configuration. They support free-run, synchronous, and holdover modes of operation, and offer both automatic and manual input clock switching. The loop filter is fully integrated on-chip, eliminating the risk of noise coupling associated with discrete solutions. Further, the jitter attenuation bandwidth is digitally programmable, providing jitter performance optimization at the application level. Programming the Si5345/44/42 is easy with Silicon Labs' ClockBuilder Pro software. Factory preprogrammed devices are also available.

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1. Typical Application Schematic

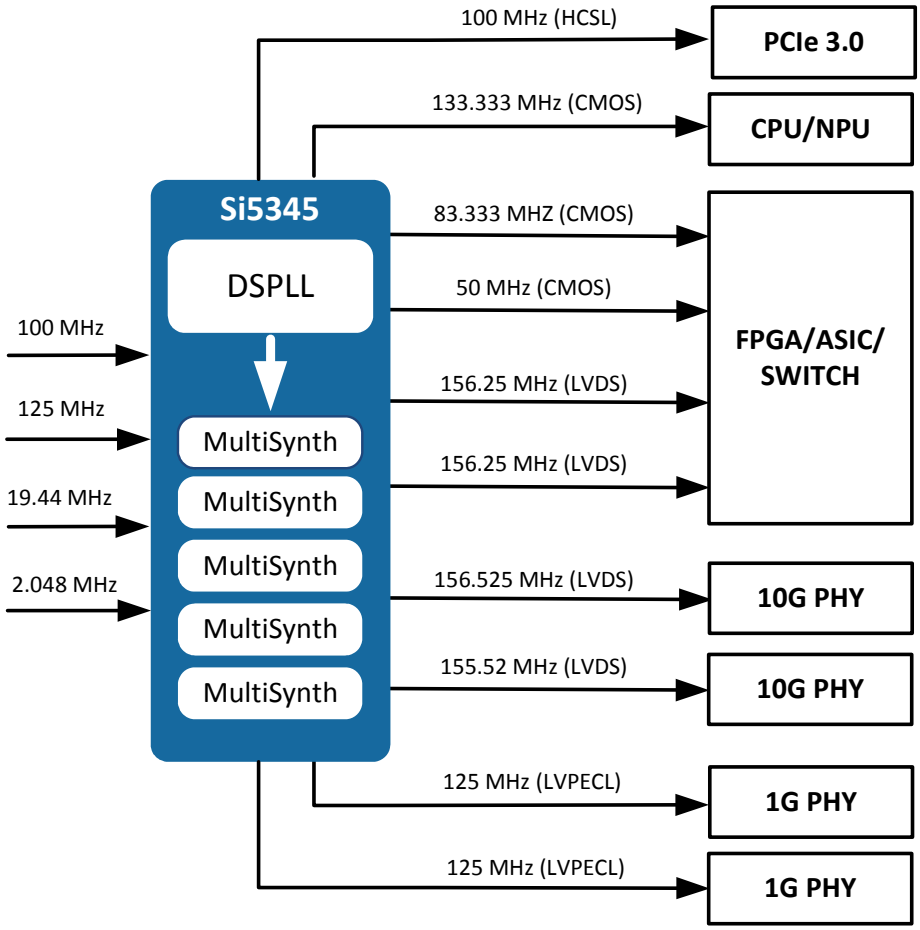


Figure 1. 10G Ethernet Data Center Switch and Compute Blade Schematic

2. Electrical Specifications

Table 1. Recommended Operating Conditions*

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Clock Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

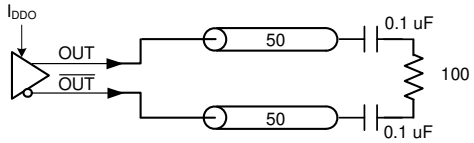
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Si5345		—	125	185	mA
		Si5344		—	105	155	mA
		Si5342		—	105	155	mA
	I_{DDA}	Si5345		—	120	125	mA
		Si5344		—	115	120	mA
		Si5342		—	115	120	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[4] @ 156.25 MHz		—	21	25	mA
		LVDS Output[4] @ 156.25 MHz		—	15	18	mA
		3.3 V LVCMOS[5] output @ 156.25 MHz		—	21	25	mA
		2.5 V LVCMOS[5] output @ 156.25 MHz		—	16	18	mA
		1.8 V LVCMOS[5] output @ 156.25 MHz		—	12	13	mA
Total Power Dissipation	P_d	Si5345	Notes 1, 6	—	880	1040	mW
		Si5344	Notes 2, 6	—	720	850	mW
		Si5342	Notes 3, 6	—	715	840	mW

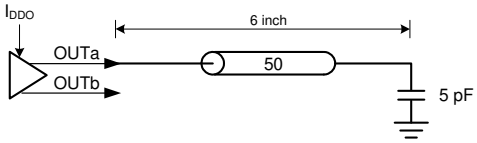
Notes:

1. Si5345 test configuration: 10x 3.3 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5344 test configuration: 4x 3.3 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Si5342 test configuration: 2x 3.3 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
4. Differential outputs terminated into an AC coupled 100 Ω load.
5. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load. Measurements were made in CMOS3 mode.

Differential Output Test Configuration



LVCMOS Output Test Configuration



6. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

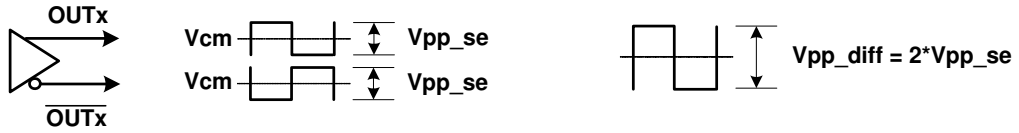
Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended - AC Coupled (IN0/$\overline{\text{IN0}}$, IN1/$\overline{\text{IN1}}$, IN2/$\overline{\text{IN2}}$, IN3/$\overline{\text{IN3}}$, FB_IN/$\overline{\text{FB\_IN}}$)						
Input Frequency Range	f_{IN_DIFF}	Differential	0.008	—	750	MHz
		Single-ended/LVCMOS	0.008	—	250	MHz
Voltage Swing[1]	V_{IN}	Differential AC Coupled f_{in} < 250 MHz	100	—	1800	mVpp_se
		Differential AC Coupled 250 MHz < f_{in} < 750 MHz	225	—	1800	mVpp_se
		Single-Ended AC Coupled f_{in} < 250 MHz	100	—	3600	mVpp_se
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
Pulsed CMOS - DC Coupled (IN0, IN1, IN2, IN3)						
Input Frequency	$f_{IN\_PULSED\_CMOS}$[4]		0.008	—	250	MHz
Input Voltage[4]	V_{IL}		–0.2	—	0.33	V
	V_{IH}		0.49	—	—	V
Slew Rate[2, 3]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (applied to XA/XB)						

Notes:

1. Voltage swing is specified as single-ended mVpp.



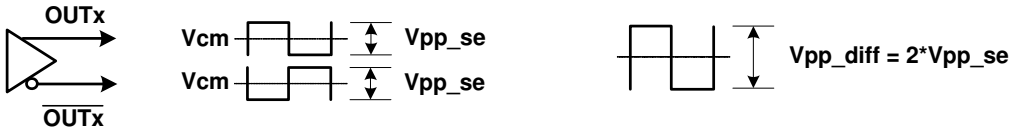
2. Imposed for jitter performance.
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN\_Vpp\_se}) / SR$
4. This mode is intended primarily for single-ended LVCMOS input clocks ≤ 1 MHz that must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low-frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.33 and 0.49 V, respectively) refer to the input attenuator circuit for dc-coupled pulsed LVCMOS in the Family Reference Manual at: www.silabs.com/Support%20Documents/TechnicalDocs/Si5345-44-42-RM.pdf. Otherwise, for standard LVCMOS input clocks, use the Standard Differential or Single-Ended ac-coupled input mode.

Table 3. Input Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REFCLK Frequency	f_{IN_REF}	Frequency range for best output jitter performance	48	—	54	MHz
		TCXO frequency for SyncE applications. Jitter performance may be reduced	—	40	—	MHz
Input Single-ended Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
Input Differential Voltage Swing	V_{IN_DIFF}		365		2500	mVpp_diff
Slew rate[2, 3]	SR		400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Notes:

1. Voltage swing is specified as single-ended mVpp.



2. Imposed for jitter performance.
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN\_Vpp\_se}) / SR$
4. This mode is intended primarily for single-ended LVCMOS input clocks ≤ 1 MHz that must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low-frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.33 and 0.49 V, respectively) refer to the input attenuator circuit for dc-coupled pulsed LVCMOS in the Family Reference Manual at: www.silabs.com/Support%20Documents/TechnicalDocs/Si5345-44-42-RM.pdf. Otherwise, for standard LVCMOS input clocks, use the Standard Differential or Single-Ended ac-coupled input mode.

Table 4. Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5345 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{RST}$, $\overline{OE}$, A1, SCLK, A0/$\overline{CS}$, FINC, FDEC, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	$\overline{RST}$, FINC and FDEC	50	—	—	ns
Update Rate	T_{UR}	FINC and FDEC	1	—	—	µs
Si5344/42 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{RST}$, $\overline{OE}$, A1, SCLK, A0/$\overline{CS}$, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	$\overline{RST}$	50	—	—	ns

***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5345/44/42 Family Reference Manual for more details on the proper register settings.

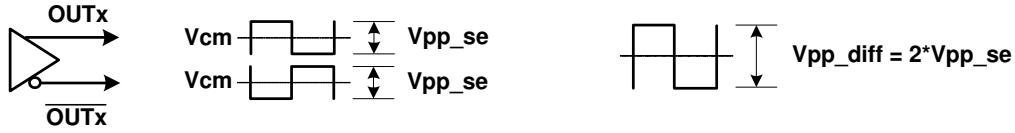
Table 5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	712.5	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 712.5 MHz		45	—	55	%
Output-Output Skew	T_{SK}	Outputs on same Multisynth (Normal Mode)		—	20	50	ps
		Outputs on same Multisynth (Low-Power Mode)		—	20	100	ps
OUT-$\overline{OUT}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	100	ps
Output Voltage Swing[1]	**Normal Mode**						
	V_{OUT}	V_{DDO} = 3.3 V or 2.5 V or 1.8 V	LVDS	350	470	550	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	660	810	1000	mVpp_se
	Low-Power Mode						
	V_{OUT}	V_{DDO} = 3.3 V or 2.5 V or 1.8 V	LVDS	300	420	530	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	620	820	1060	mVpp_se

Note:

1. For normal and low-power modes, the amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low-power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Also note that the output voltage swing specifications are given in peak-to-peak single-ended swing.



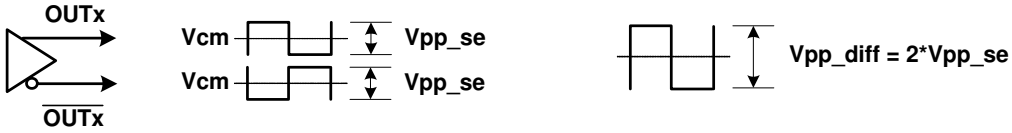
2. Not all combinations of voltage swing and common mode voltages settings are possible. See the Si5345/44/42 Family Reference Manual for details.
3. Driver output impedance depends on selected output mode (Normal, Low-Power).
4. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
5. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 5. Differential Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Common Mode Voltage[1,2] (100 Ω load line-to-line)	**Normal Mode or Low-Power Mode**						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.25	1.35	V
			LVPECL	1.90	2.05	2.15	V
		V_{DDO} = 2.5 V	LVPECL LVDS	1.15	1.25	1.35	V
		V_{DDO} = 1.8 V	Sub-LVDS	0.87	0.93	1.0	V
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Mode		—	170	240	ps
		Low-Power Mode		—	300	430	
Differential Output Impedance[3]	Z_O	Normal Mode		—	100	—	Ω
		Low-Power Mode		—	650	—	Ω

Note:

1. For normal and low-power modes, the amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low-power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Also note that the output voltage swing specifications are given in peak-to-peak single-ended swing.



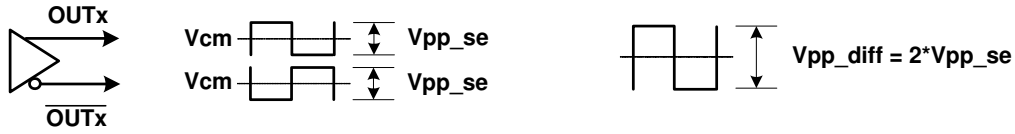
2. Not all combinations of voltage swing and common mode voltages settings are possible. See the Si5345/44/42 Family Reference Manual for details.
3. Driver output impedance depends on selected output mode (Normal, Low-Power).
4. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
5. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 5. Differential Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Noise Rejection[4]	PSRR	**Normal Mode**				
		10 kHz sinusoidal noise	—	–93	—	dBc
		100 kHz sinusoidal noise	—	–93	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–79	—	
		Low Power Mode				
		10 kHz sinusoidal noise	—	–98	—	dBc
		100 kHz sinusoidal noise	—	–95	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–76	—	
Output-output Crosstalk	XTALK	Si5345 Measured spur from adjacent output[5]	—	–75	—	dBc
		Si5342/44 Measured spur from adjacent output[5]	—	–85	—	dBc

Note:

1. For normal and low-power modes, the amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low-power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Also note that the output voltage swing specifications are given in peak-to-peak single-ended swing.



2. Not all combinations of voltage swing and common mode voltages settings are possible. See the Si5345/44/42 Family Reference Manual for details.
3. Driver output impedance depends on selected output mode (Normal, Low-Power).
4. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
5. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 6. LVCMOS Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} <100 MHz		47	—	53	%
		100 MHz < f_{OUT} < 250 MHz		44	—	55	
Output-to-Output Skew	T_{SK}			—	—	100	ps
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV = 3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV = 3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OH} = –4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –5 mA		—	—	

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5345/44/42 Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

AC Test Configuration

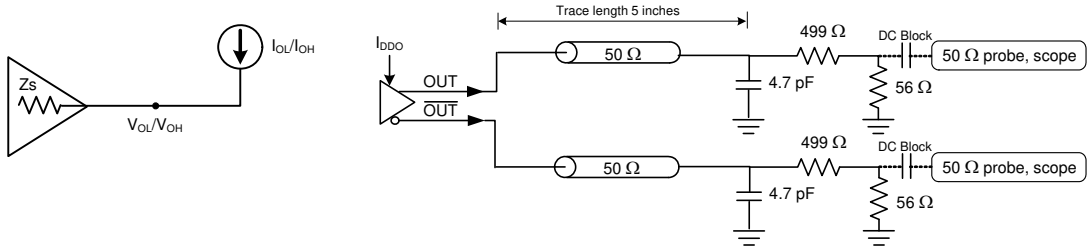


Table 6. LVCMOS Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3V		—	420	550	ps
		VDDO = 2.5 V		—	475	625	ps
		VDDO = 1.8 V		—	525	705	ps

Notes:
1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5345/44/42 Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

AC Test Configuration

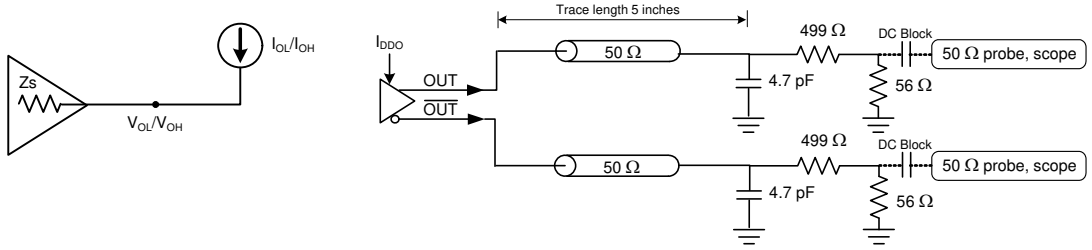


Table 7. Output Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5345 Status Output Pins ($\overline{LOL}$, $\overline{INTR}$, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO} x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5344 Status Output Pins ($\overline{LOL}$, $\overline{INTR}$, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5342 Status Output Pins ($\overline{LOL}$, $\overline{LOS0}$, $\overline{LOS1}$, $\overline{LOS2}$, $\overline{LOS3}$, $\overline{LOS\_XAXB}$, $\overline{INTR}$, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

Notes:

1. Note that the V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. VOL remains valid in all cases.
2. VDDIO is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5345/44/42 Family Reference Manual for more details on the proper register settings.

Table 8. Performance Characteristics

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}		0.1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time[2]	t_{ACQ}	f_{IN} = 19.44 MHz	—	500	600	ms
Output Delay Adjustment	t_{DELAY_frac}	f_{VCO} = 14 GHz	—	0.28	—	ps
	t_{DELAY_int}		—	71.4	—	ps
	t_{RANGE}		—	±9.14	—	ns
POR to Serial Interface Ready[3]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a Loop Bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1 and 2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Only valid for a single switch between two input clocks running at the same frequency	—	—	2.8	ns
Pull-in Range	ω_P		—	500	—	ppm
Input-to-Output Delay Variation	$t_{IODELAY}$		—	2	—	ns
	t_{ZDELAY}	In Zero Delay Mode. Measured as the time delay difference between the reference input and the feedback input, with both clocks running at 10 MHz and having the same slew rate. The rise time of the reference input should not exceed 200 ps in order to meet this spec.	—	110	—	ps
RMS Phase Jitter[4]	J_{GEN}	Integer Mode 12 kHz to 20 MHz	—	0.090	0.140	ps RMS
		Fractional Mode 12 kHz to 20 MHz	—	0.130	0.165	ps RMS

Notes:

1. Actual loop bandwidth might be lower; please refer to CBPro for actual value for your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL tresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths set to 100 Hz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator deassertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
			Standard Mode 100 kbps		Fast Mode 400 kbps		
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

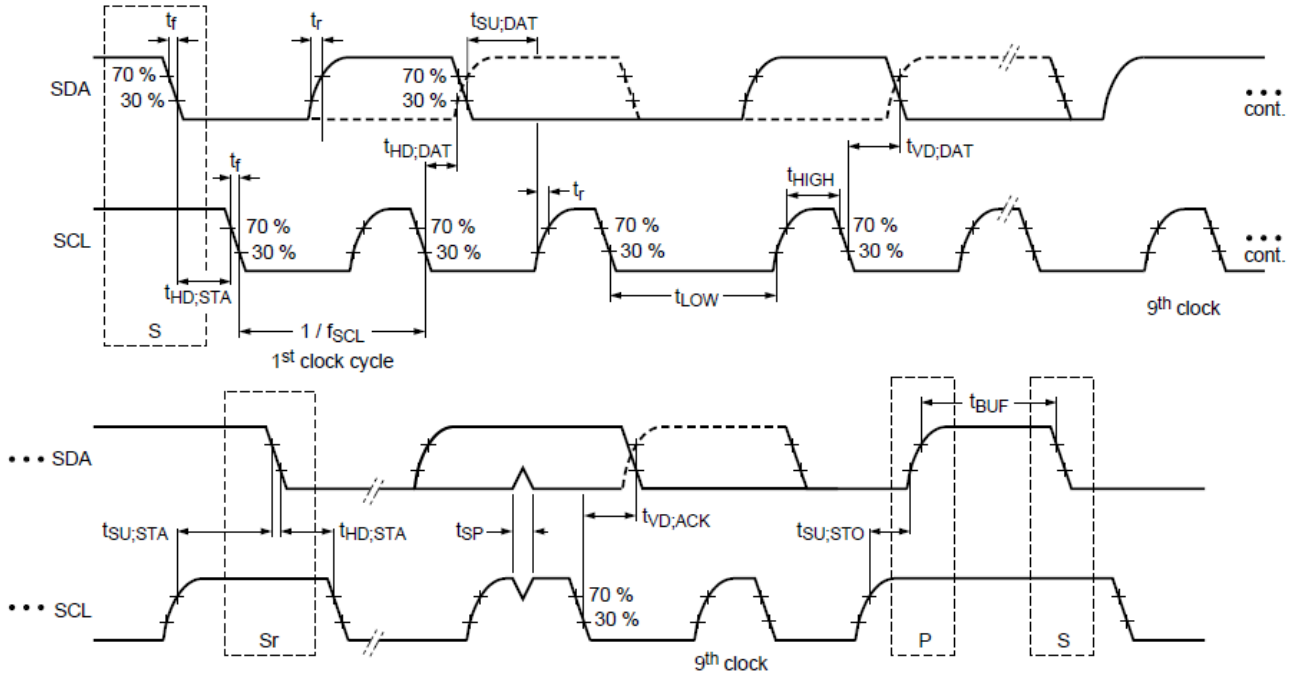


Figure 2. I²C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications (4-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	12.5	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	10	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to $\overline{CS}$	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

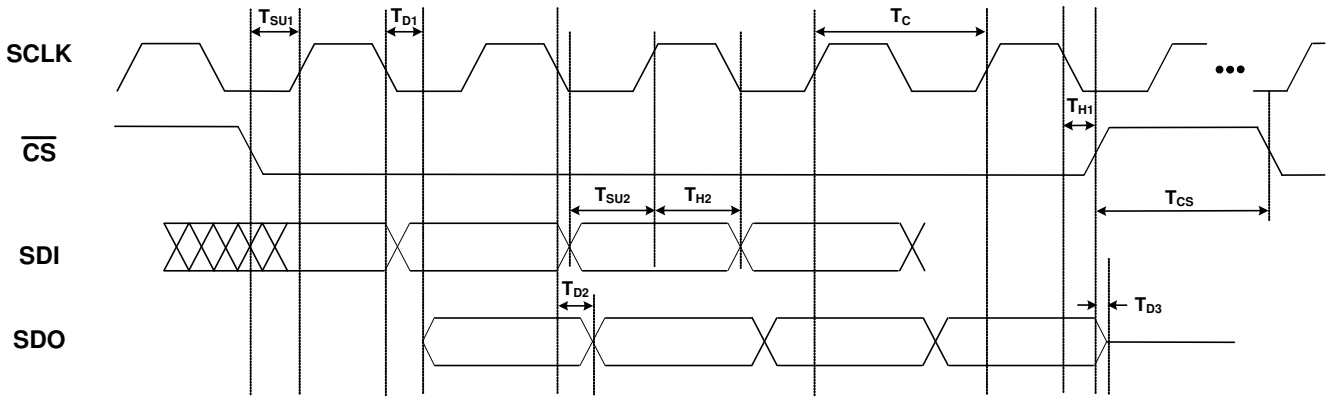


Figure 3. 4-Wire SPI Serial Interface Timing

Table 11. SPI Timing Specifications (3-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	12.5	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	10	15	ns
Delay Time, $\overline{CS}$ Rise to SDIO Tri-State	T_{D3}	—	10	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Fall	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

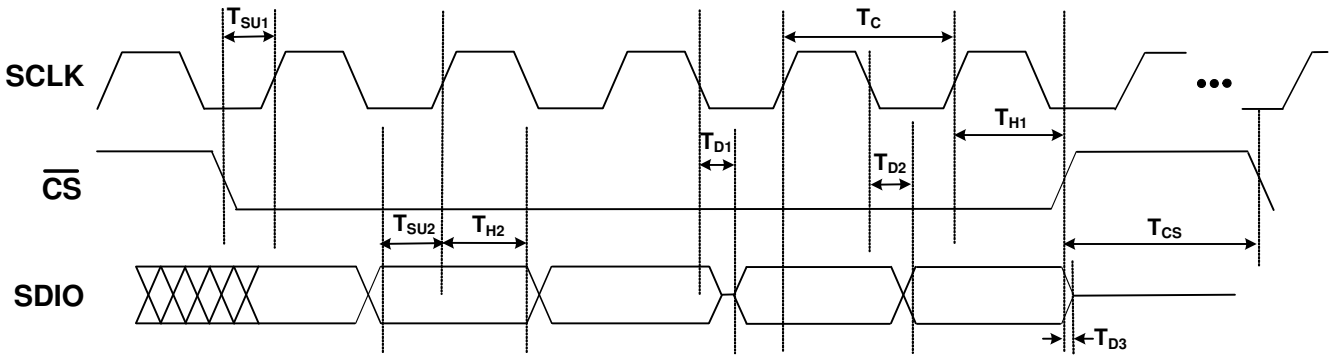


Figure 4. 3-Wire SPI Serial Interface Timing

Table 12. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	$f_{XTAL\_48\text{-}54}$	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	$C_{L\_48\text{-}54}$		—	8	—	pF
Shunt Capacitance	$C_{O\_48\text{-}54}$		—	—	2	pF
Crystal Drive Level	$d_{L\_48\text{-}54}$		—	—	200	µW
Equivalent Series Resistance	$r_{ESR\_48\text{-}54}$	Refer to the Si5345/44/42 Family Reference Manual to determine ESR.				
Crystal Frequency Range	f_{XTAL_25}		—	25	—	MHz
Load Capacitance	C_{L_25}		—	8	—	pF
Shunt Capacitance	C_{O_25}		—	—	3	pF
Crystal Drive Level	d_{L_25}		—	—	200	µW
Equivalent Series Resistance	r_{ESR_25}	Refer to the Si5345/44/42 Family Reference Manual to determine ESR.				

Notes:
1. The Si5345/44/42 is designed to work with crystals that meet the specifications in Table 12.
2. Refer to the Si5345/44/42 Family Reference Manual for recommended 48 to 54 MHz crystals.

Table 13. Thermal Characteristics

Parameter	Symbol	Test Condition*	Value	Unit
Si5345-64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5344, Si5342-44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	
***Note:** Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.				

Table 14. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0 – IN3/FB_IN	–0.85 to 3.8	V
	V_{I2}	IN_SEL1, IN_SEL0, $\overline{RST}$, $\overline{OE}$, I2C_SEL, FINC, FDEC, SDI, SCLK, A0/$\overline{CS}$, A1, SDA/SDIO	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Junction Temperature	T_{JCT}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[4]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20–40	s

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For more packaging information, including MSL rating, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

3. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V, V_{DDA} = 3.3 V, V_{DDS} = 3.3 V, 1.8 V, and T_A = 25 °C.

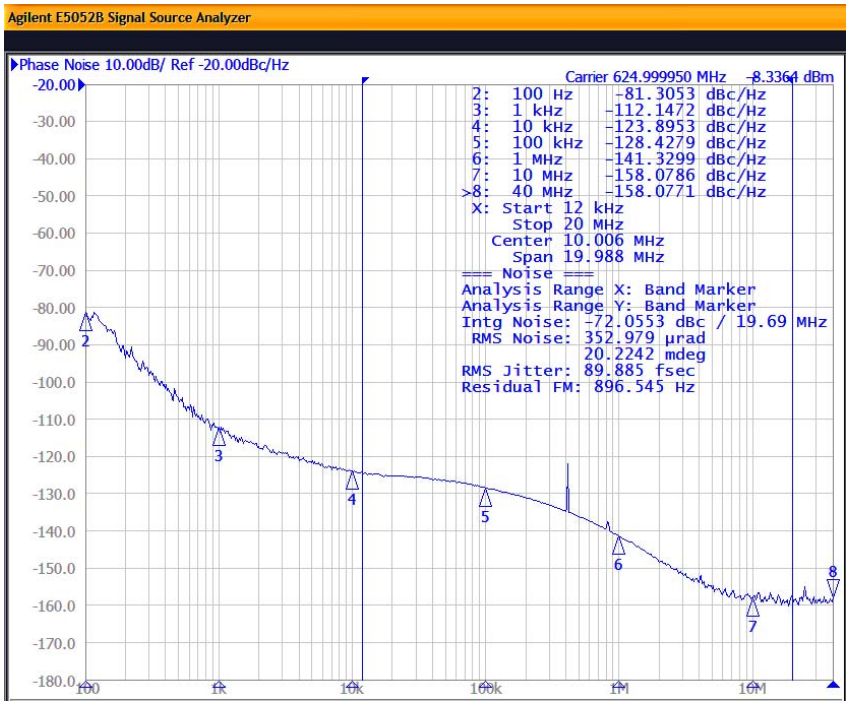


Figure 5. Input = 25 MHz; Output = 625 MHz, 2.5 V LVDS

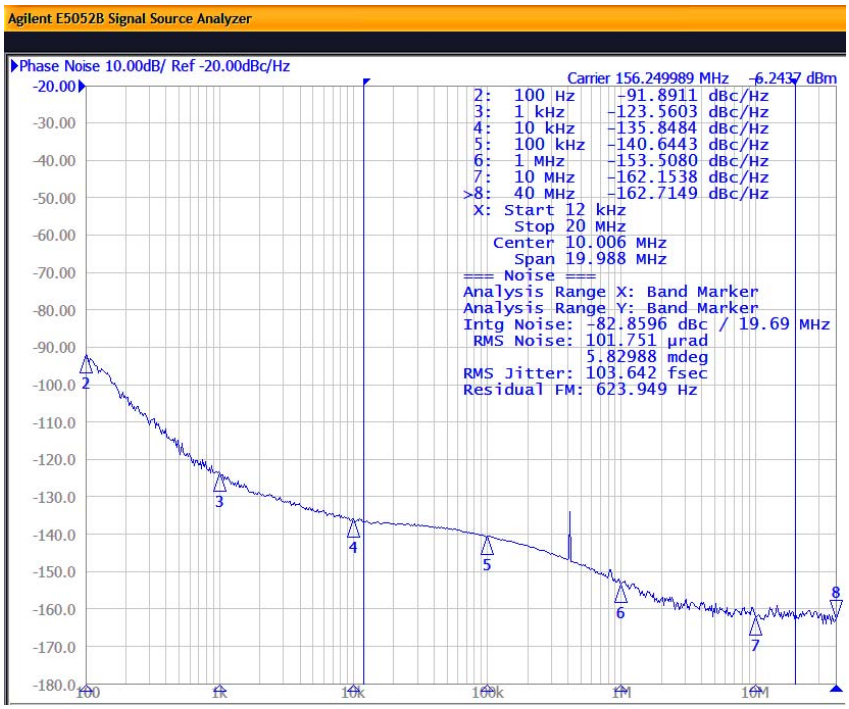


Figure 6. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS

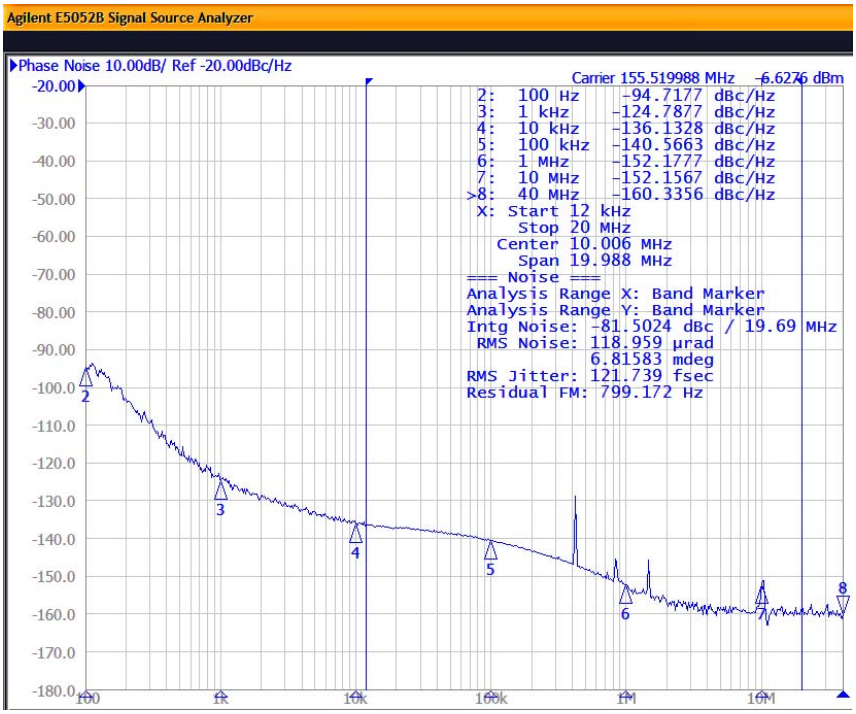


Figure 7. Input = 25 MHz; Output = 155.52 MHz, 2.5 V LVDS

4. Detailed Block Diagrams

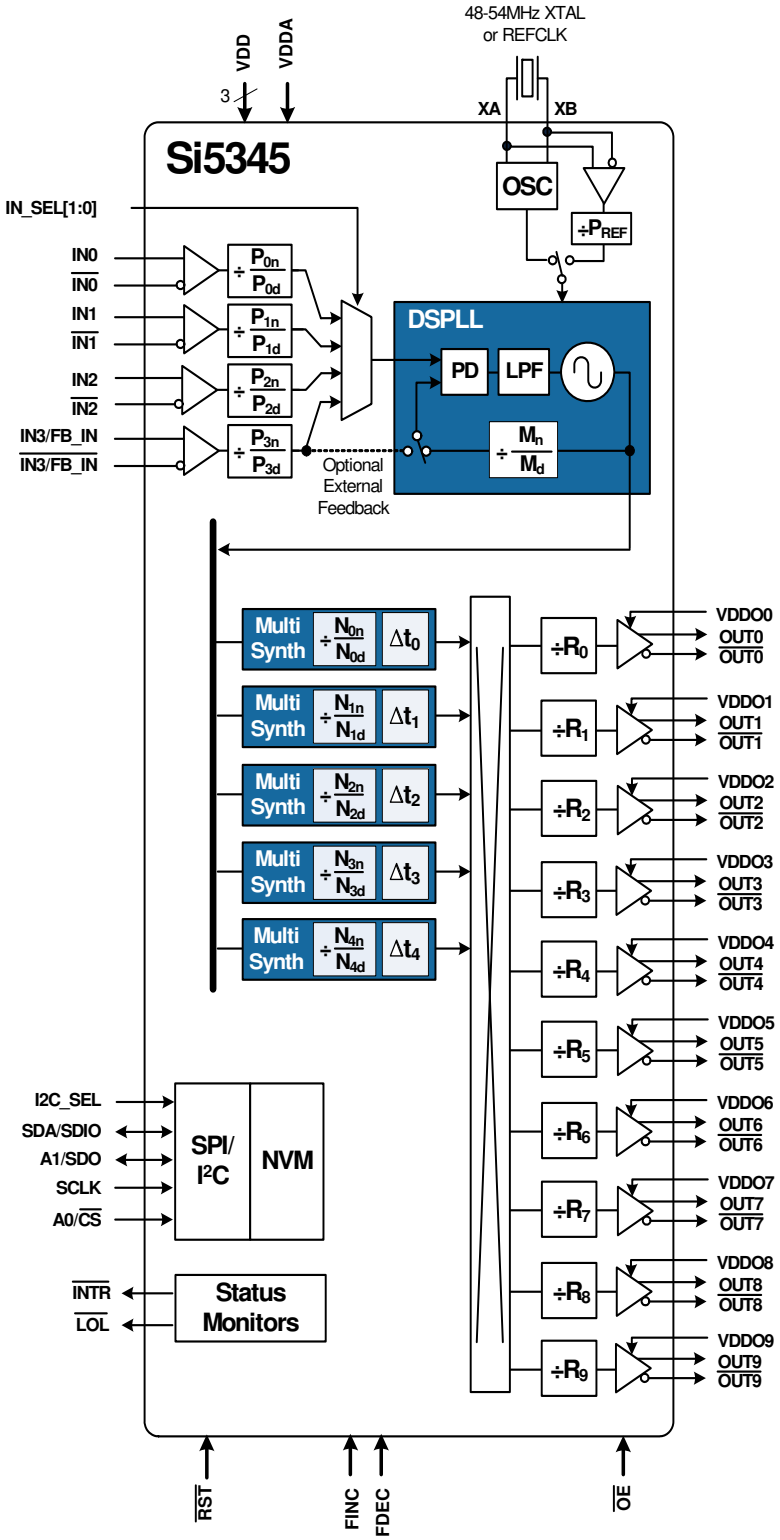


Figure 8. Si5345 Block Diagram