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Si5347/46

DUAL/QUAD DSPLL ANY-FREQUENCY, ANY-OUTPUT JITTER ATTENUATORS

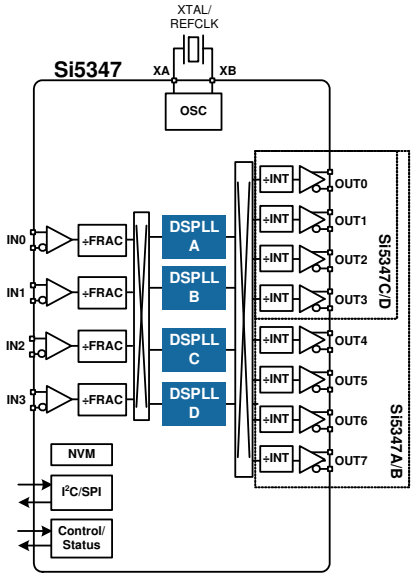
Features

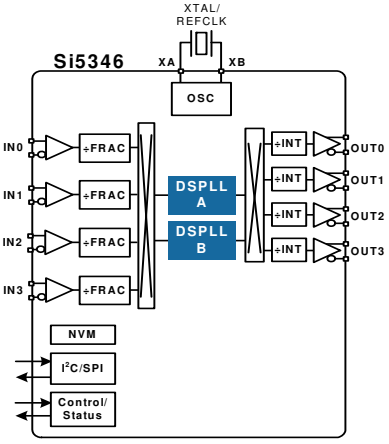
- Four or two independent DSPLLs in a single monolithic IC
- Each DSPLL generates any output frequency from any input frequency
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: up to 712.5 MHz
  - LVCMOS: up to 250 MHz
- Ultra low jitter: <100 fs typ (12 kHz–20 MHz)
- Flexible crosspoints route any input to any output clock
- Programmable jitter attenuation bandwidth per DSPLL: 0.1 Hz to 4 kHz programming range
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Locks to gapped clock inputs
- Automatic free-run and holdover modes
- Fastlock feature for low nominal bandwidths
- Glitchless on-the-fly DSPLL frequency changes
- DCO mode: as low as 0.01 ppb steps per DSPLL
- Core voltage:
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output clock supply pins: 3.3, 2.5, or 1.8 V
- Output-output skew:
  - <20 ps (typ) per DSPLL
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder™ Pro software tool simplifies device configuration
- Si5347: Quad DSPLL, 4 input, 4 or 8 output, 64 QFN
- Si5346: Dual DSPLL, 4 input, 4 output, 44 QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

9x9 mm 7x7 mm

Ordering Information:
See section 8

Functional Block Diagram





Device Selector Guide

Grade	PLLs/OUTs	Max Output Freq	Frequency Synthesis Modes
Si5347A	4/8	712.5 MHz	Integer + Fractional
Si5347C	4/4	712.5 MHz	Integer + Fractional
Si5346A	2/4	712.5 MHz	Integer + Fractional
Si5347B	4/8	350 MHz	Integer + Fractional
Si5347D	4/4	350 MHz	Integer + Fractional
Si5346B	2/4	350 MHz	Integer + Fractional

Applications

- OTN Muxponders and Transponders
- 10/40/100G network line cards
- GbE/10 GbE/100 GbE Synchronous Ethernet (ITU-T G.8262)
- Carrier Ethernet switches
- Broadcast video

Description

The Si5347 is a high performance jitter attenuating clock multiplier which integrates four any-frequency DSPLLs for applications that require maximum integration and independent timing paths. The Si5346 is a dual DSPLL version in a smaller package. Each DSPLL has access to any of the four inputs and can provide low jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency conversion with typical jitter performance under 100 fs. Each DSPLL supports independent free-run, holdover modes of operation, as well as automatic and hitless input clock switching. The Si5347/46 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up in a known configuration. Programming the Si5347/46 is easy with Silicon Labs' ClockBuilder Pro software. Factory pre-programmed devices are also available.

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1. Typical Application Schematic

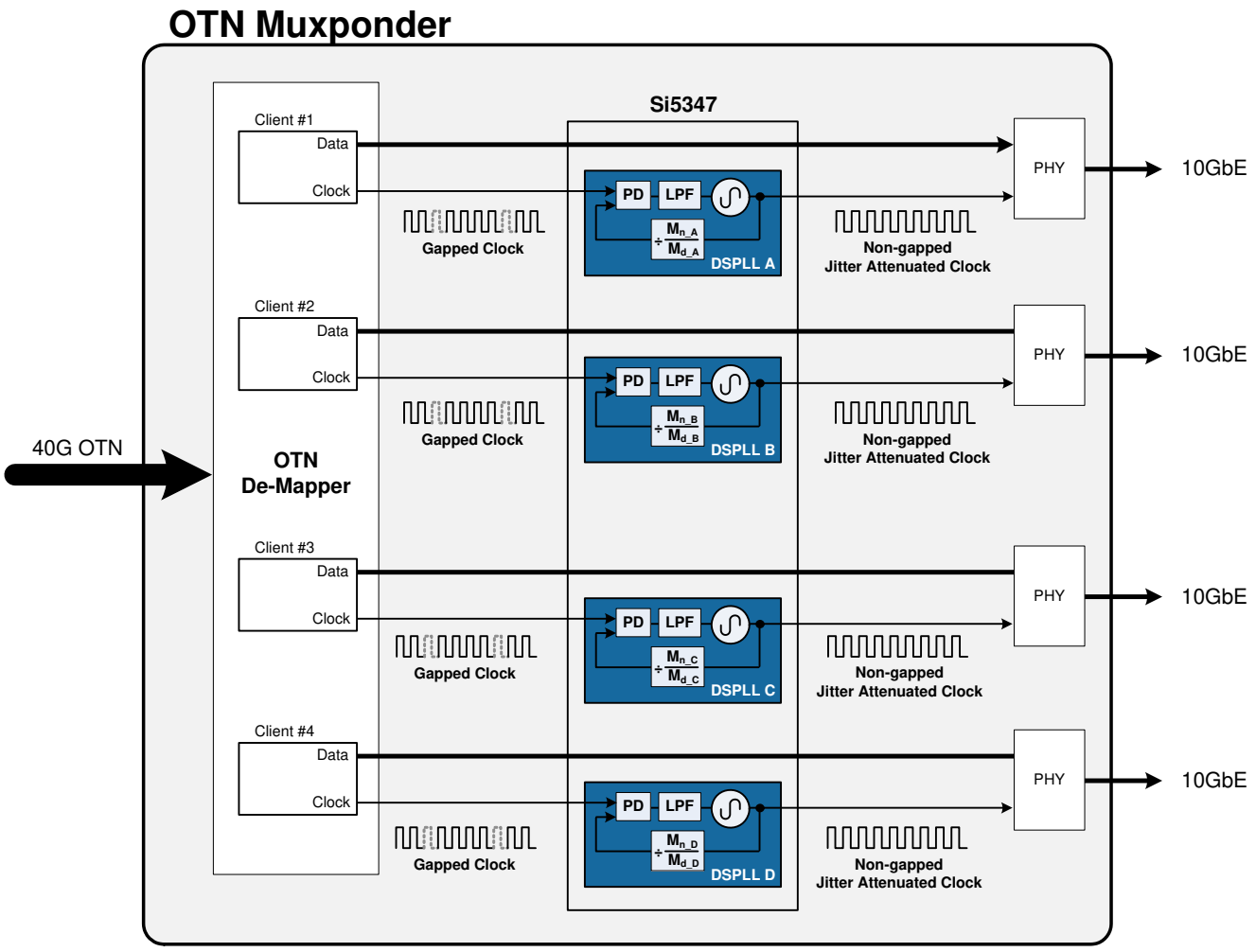


Figure 1. Using the Si5347 to Clean Gapped Clocks in an OTN Application

2. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

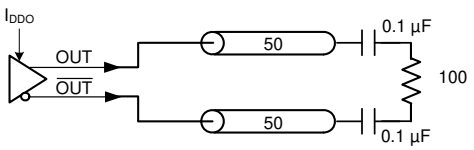
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Si5347	Notes [1, 2]	—	175	240	mA
		Si5346		—	170	230	mA
	I_{DDA}	Si5347		—	120	130	mA
		Si5346			120	130	mA

Notes:

1. Si5347 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5346 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting. Refer to the Si5347/46 Family Reference Manual for more details on register settings.
5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

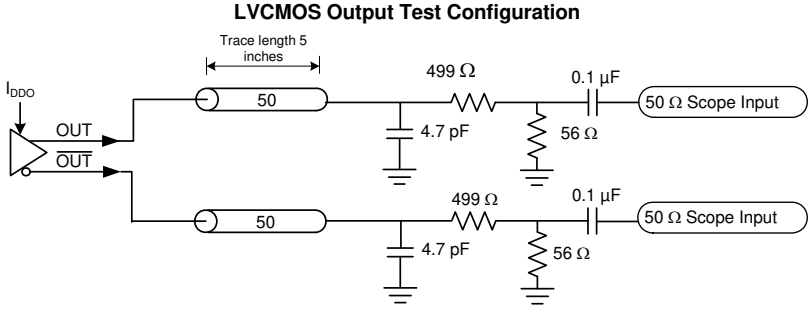


Table 2. DC Characteristics (Continued)

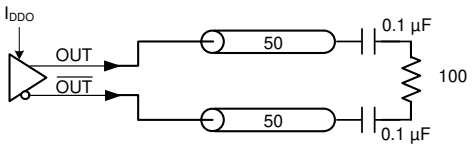
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Buffer Supply Current	I_{DDO}	LVPECL Output[3] @ 156.25 MHz		—	21	25	mA
		LVDS Output[3] @ 156.25 MHz		—	15	18	mA
		3.3V LVCMOS[4] output @ 156.25 MHz		—	21	25	mA
		2.5V LVCMOS[4] output @ 156.25 MHz		—	16	18	mA
		1.8V LVCMOS[4] output @ 156.25 MHz		—	12	13	mA
Total Power Dissipation	P_d	Si5347	Note [1,5]	—	980	1160	mW
		Si5346	Note [2,5]	—	840	1000	mW

Notes:

1. Si5347 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5346 test configuration: 4 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting. Refer to the Si5347/46 Family Reference Manual for more details on register settings.
5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

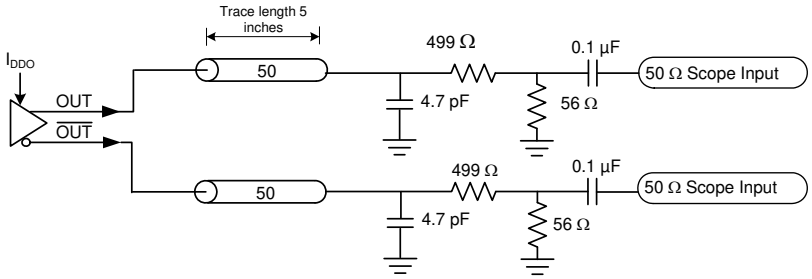


Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended/LVCMOS — AC-coupled (IN0, IN1, IN2, IN3/FB_IN)						
Input Frequency Range	f_{IN_DIFF}	Differential	0.008	—	750	MHz
		Single-ended/LVCMOS	0.008	—	250	
Input Voltage Swing	V_{IN_DIFF}	f_{IN}< 250 MHz, Differential	100	—	1800	mVpp_se
		250 MHz < f_{IN}< 750 MHz, Differential	225	—	1800	mVpp_se
Input Voltage Amplitude	V_{IN_SE}	f_{IN}< 250 MHz, Single-ended	100	—	3600	mVpp_se
Slew Rate[1,2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
Pulsed CMOS — DC-coupled (IN0, IN1, IN2, IN3)[3]						
Input Frequency	f_{IN_PULSED}		0.008	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.33	V
	V_{IH}		0.49	—	—	V
Slew Rate[1,2]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Frequency range for best output jitter performance	48	—	54	MHz
Input Voltage Swing	V_{IN_DIFF}		365	—	2500	mVpp_diff
	V_{IN_SE}		365	—	2000	mVpp_se
Slew rate[1,2]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) \times V_{IN\_Vpp\_se}) / SR$.
3. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks ≤ 1 MHz, which must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (VIL, VIH) of this buffer are non-standard (0.33 and 0.49 V, respectively), refer to the input attenuator circuit for DC-coupled Pulsed LVCMOS in the Si5347-46 Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard AC-coupled, Single-ended input mode.

Table 4. Serial and Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5347 Serial and Control Input Pins (I2C_SEL, $\overline{RST}$, $\overline{OE0}$, A1/SDO, SCLK, A0/$\overline{CS}$, FINC, A0/$\overline{CS}$, SDA/SDIO, DSPLL_SEL[1:0])						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_L		—	20	—	kΩ
Minimum Pulse Width	PW	$\overline{RST}$, FINC	100	—	—	ns
Update Rate	F_{UR}	FINC	—	—	1	MHz
Si5347 Control Input Pins (FDEC, $\overline{OE1}$)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDS}	V
	V_{IH}		0.7 x V_{DDS}	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Minimum Pulse Width	PW	FDEC	100	—	—	ns
Update Rate	F_{UR}	FDEC	—	—	1	MHz
Si5346 Serial and Control Input Pins (I2C_SEL, $\overline{RST}$, $\overline{OE0}$, $\overline{OE1}$, A1/SDO, SCLK, A0/$\overline{CS}$, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_L		—	20	—	kΩ
Minimum Pulse Width	PW	$\overline{RST}$	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

Table 5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	712.5	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 712.5 MHz		44	—	55	%
Output-Output Skew	T_{SK}	Differential Output, Normal Swing Mode		—	20	50	ps
		Differential Output, Low Power Swing Mode		—	20	100	ps
OUT-$\overline{OUT}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	100	ps
Output Voltage Amplitude[1]	**Normal Mode**						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	470	550	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	660	810	1000	
	Low Power Mode						
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	300	420	530	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	620	820	1060	

Notes:

1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum.Refer to the Si5347/46 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.
2. Driver output impedance depends on selected output mode (Normal, Low Power). Refer to the Si5347/46 Family Reference Manual for more information.
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.
4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.

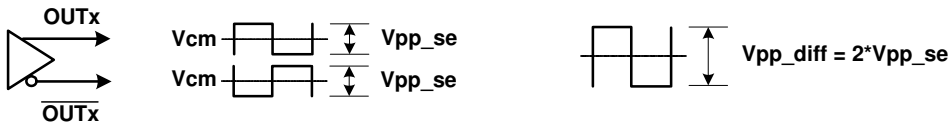


Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Common Mode Voltage[1,2,3]	**Normal Mode or Low Power Modes**						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.25	1.35	V
			LVPECL	1.90	2.05	2.15	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.15	1.25	1.35	
		V_{DDO} = 1.8 V	sub-LVDS	0.87	0.93	1.00	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Mode		—	170	240	ps
		Low Power Mode		—	300	430	
Differential Output Impedance[2]	Z_O	Normal Mode		—	100	—	Ω
		Low Power Mode		—	650	—	Ω

Notes:

1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum.Refer to the Si5347/46 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.
2. Driver output impedance depends on selected output mode (Normal, Low Power). Refer to the Si5347/46 Family Reference Manual for more information.
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.
4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.

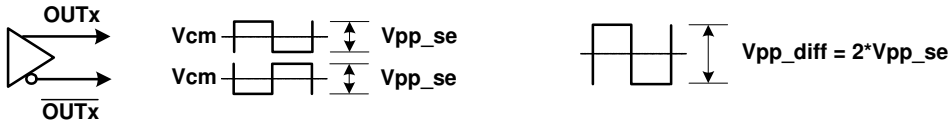


Table 5. Differential Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Noise Rejection[3]	PSRR	**Normal Mode**				
		10 kHz sinusoidal noise	—	–93	—	dBc
		100 kHz sinusoidal noise	—	–93	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–79	—	
		Low Power Mode				
		10 kHz sinusoidal noise	—	–98	—	dBc
		100 kHz sinusoidal noise	—	–95	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–76	—	
Output-output Crosstalk[4]	XTALK	Si5347	—	–75	—	dB
		Si5346	—	–85	—	dB

Notes:
1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum.Refer to the Si5347/46 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.
2. Driver output impedance depends on selected output mode (Normal, Low Power). Refer to the Si5347/46 Family Reference Manual for more information.
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/ 3.3 V = 100 mVpp) and noise spur amplitude measured.
4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.

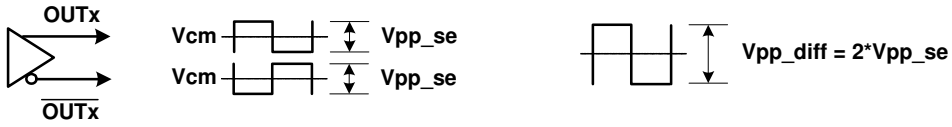


Table 6. LVCMOS Clock Output Specifications

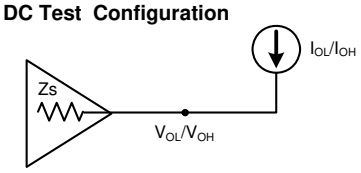
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} <100 MHz		47	—	53	%
		100 MHz < f_{OUT} < 250 MHz		44	—	55	
Output-to-Output Skew	T_{SK}	LVCMOS outputs		—	—	100	ps
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OH} = –10 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OH} = –6 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OH} = –4 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=3	I_{OH} = –5 mA		—	—	

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5347/46 Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



LVCMOS Output Test Configuration

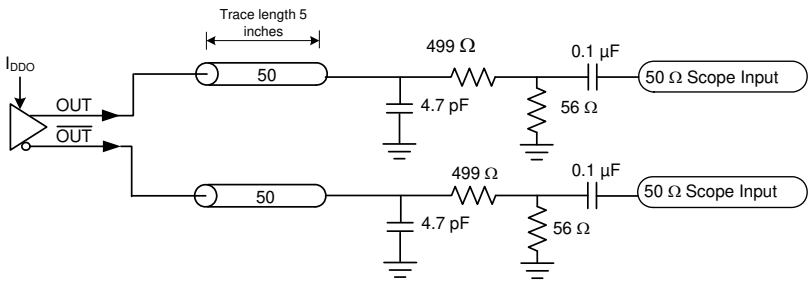


Table 6. LVCMOS Clock Output Specifications (Continued)

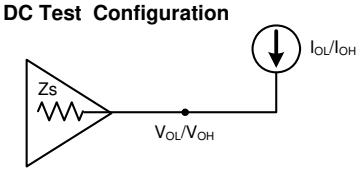
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3V		—	420	550	ps
		VDDO = 2.5 V		—	475	625	ps
		VDDO = 1.8 V		—	525	705	ps

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5347/46 Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



LVCMOS Output Test Configuration

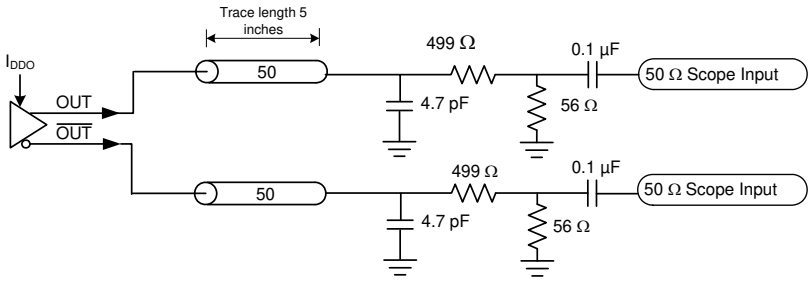


Table 7. Output Serial and Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5347 Serial and Status Output Pins ($\overline{\text{LOL\_A}}$, $\overline{\text{LOL\_B}}$, $\overline{\text{LOL\_C}}$, $\overline{\text{LOL\_D}}$, $\overline{\text{INTR}}$, $\overline{\text{LOS\_XAXB}}$, SDA/SDIO[1], A1/SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5346 Status Output Pins ($\overline{\text{INTR}}$, $\overline{\text{LOS\_XAXB}}$, SDA/SDIO[1], A1/SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5346 Serial and Status Output Pins ($\overline{\text{LOL\_A}}$, $\overline{\text{LOL\_B}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

Notes:

1. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. V_{OL} remains valid in all cases.
2. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. Users normally select this option in the ClockBuilder Pro GUI. Alternatively, refer to the Si5347-46 Family Reference Manual for more details on register settings.

Table 8. Performance Characteristics

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[3]	f_{BW}		0.1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time	t_{ACQ}	With Fastlock enabled, f_{IN} = 19.44 MHz[1]	—	500	600	ms
POR to Serial Interface Ready[2]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1&2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Only valid for a single switch between two input clocks running at the same frequency	—	—	2.8	ns
Pull-in Range	ω_P		—	500	—	ppm
Input-to-Output Delay Variation	$t_{IODELAY}$		—	2	—	ns
RMS Phase Jitter[4]	J_{GEN}	12 kHz to 20 MHz	—	0.090	0.165	ps RMS

Notes:

1. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths, both set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
2. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
3. Actual loop bandwidth might be lower; please refer to CBPro for actual value on your frequency plan.
4. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz. Does not include jitter from input reference.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold Time (repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_f		—	300	—	300	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

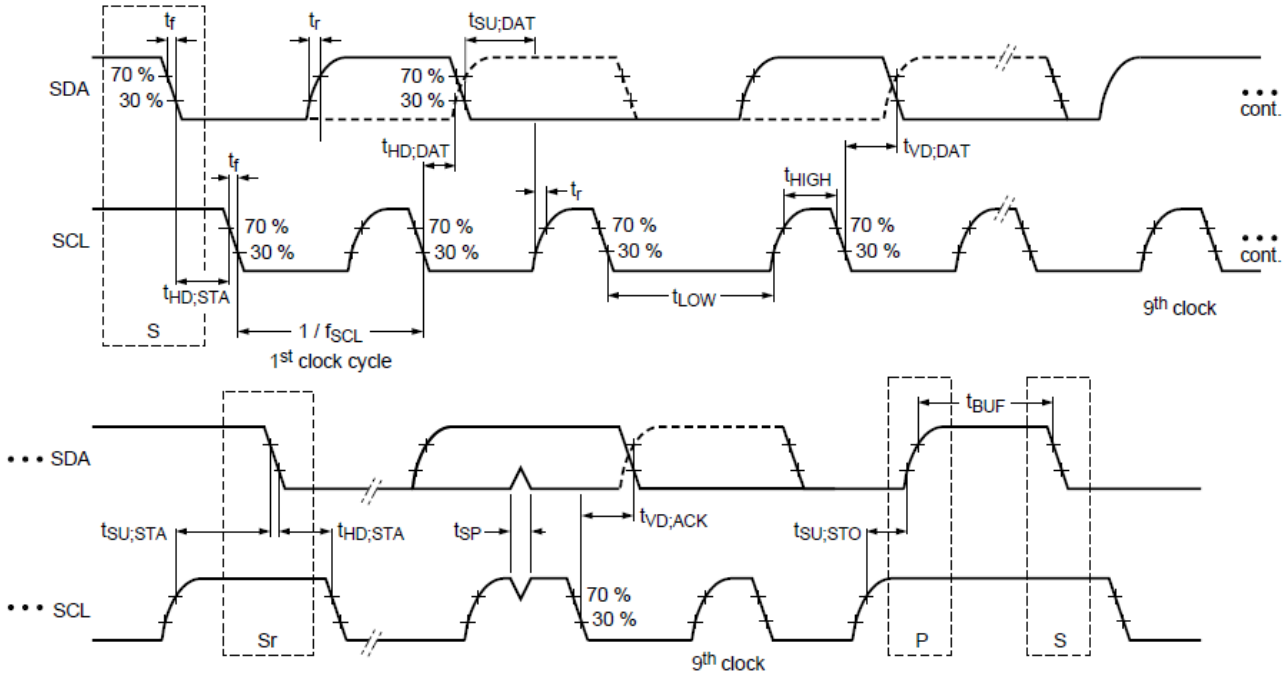


Figure 2. I²C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications (4-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	15	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	—	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to $\overline{CS}$	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

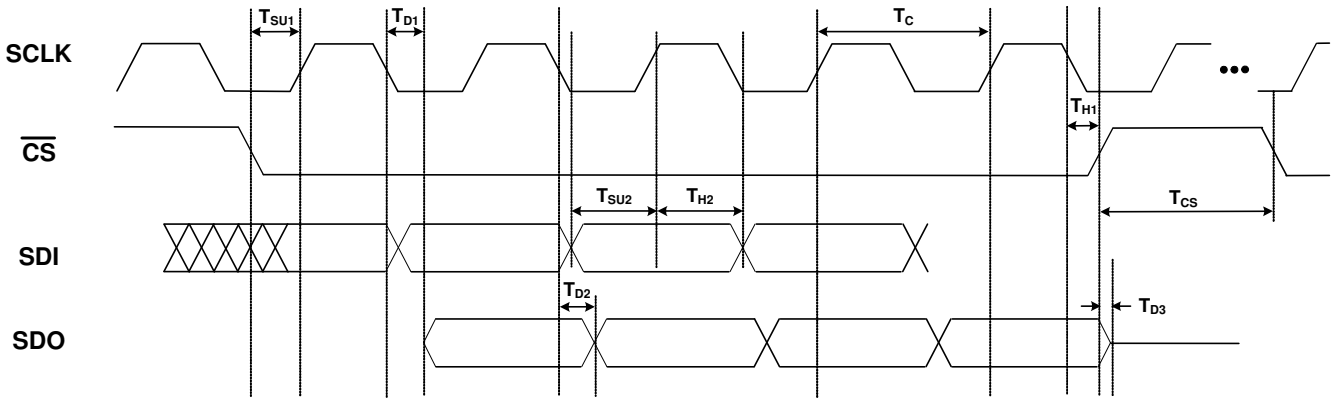


Figure 3. 4-Wire SPI Serial Interface Timing

Table 11. SPI Timing Specifications (3-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, $\overline{CS}$ Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to $\overline{CS}$	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

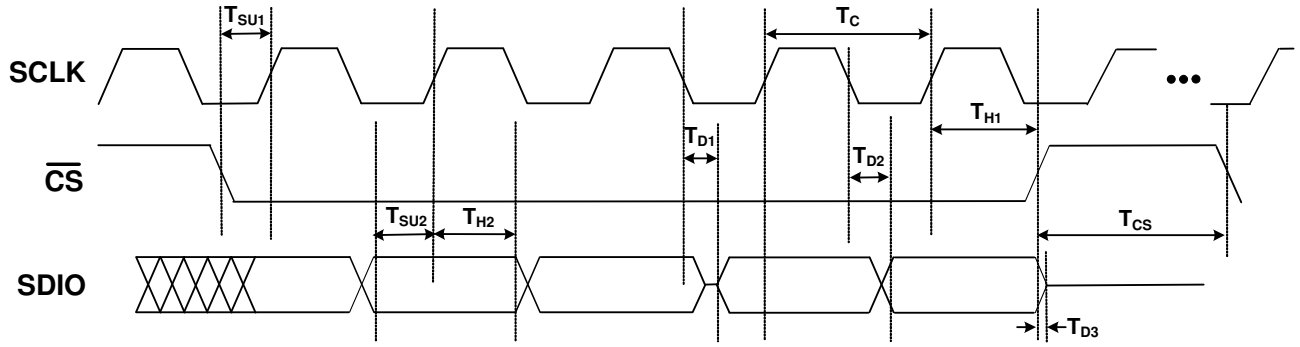


Figure 4. 3-Wire SPI Serial Interface Timing

Table 12. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	$f_{XTAL\_48\text{-}54}$	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	$C_{L\_48\text{-}54}$		—	8	—	pF
Shunt Capacitance	$C_{O\_48\text{-}54}$		—	—	2	pF
Crystal Drive Level	$d_{L\_48\text{-}54}$		—	—	200	µW
Equivalent Series Resistance	$r_{ESR\_48\text{-}54}$	Refer to the Si5347/46 Family Reference Manual to determine ESR.				
Crystal Frequency Range	f_{XTAL_25}		—	25	—	MHz
Load Capacitance	C_{L_25}		—	8	—	pF
Shunt Capacitance	C_{O_25}		—	—	3	pF
Crystal Drive Level	d_{L_25}		—	—	200	µW
Equivalent Series Resistance	r_{ESR_25}	Refer to the Si5347/46 Family Reference Manual to determine ESR.				

Notes:
1. The Si5347/46 is designed to work with crystals that meet the frequencies and specifications in Table 12.
2. Refer to the Si5347/46 Family Reference Manual for recommended 48 to 54 MHz crystals.

Table 13. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Unit
Si5347–64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5346–44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	

Notes:
1. Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 14. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0 – IN3/FB_IN	–0.85 to 3.8	V
	V_{I2}	$\overline{RST}$, $\overline{OE0}$, $\overline{OE1}$, I2C_SEL, FINC, FDEC, PLL_SEL[1:0] SDA/SDIO, A1/$\overline{SDO}$, SCLK, A0/$\overline{CS}$	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 150	°C
Storage Temperature Range	T_{STG}		–55 to +150	°C
Soldering Temperature (Pb-free profile)[3]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20–40	s

Note:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For detailed MSL and packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

3. Typical Operating Characteristics (Jitter and Phase Noise)

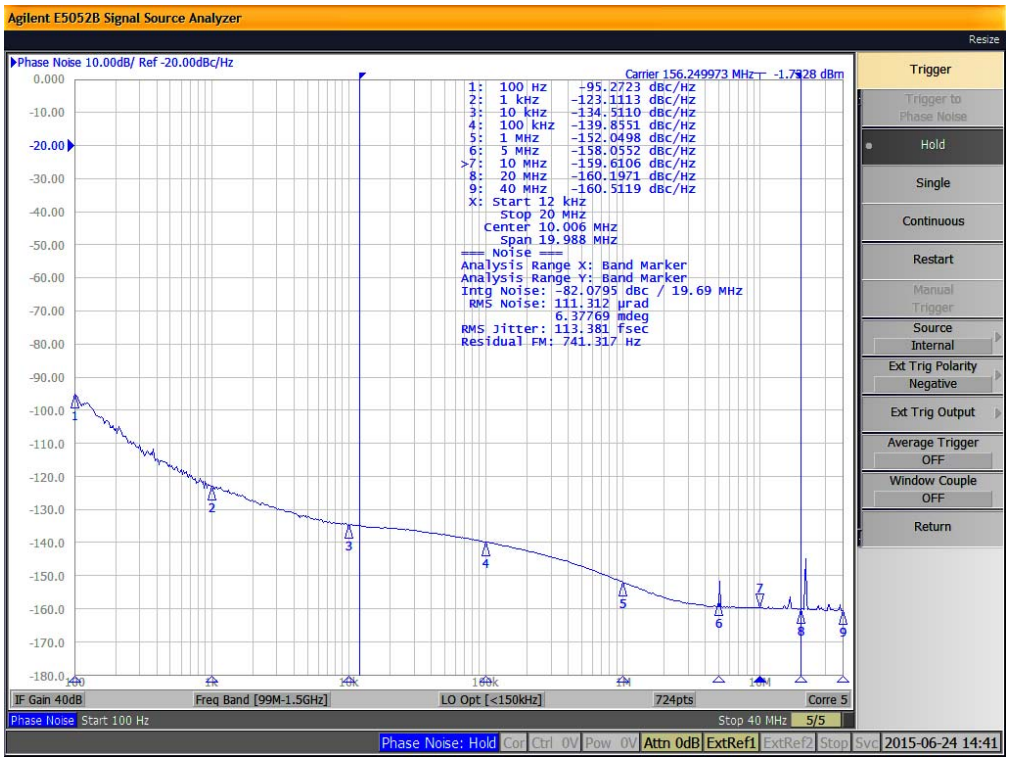


Figure 5. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS

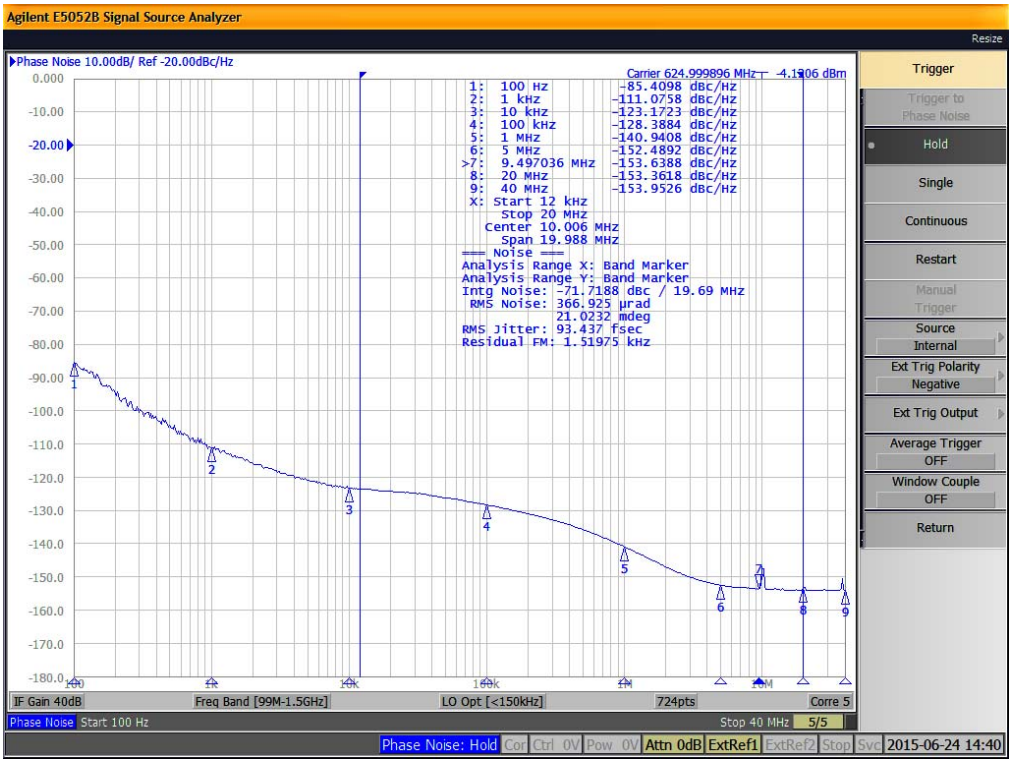


Figure 6. Input = 25 MHz; Output = 625 MHz, 2.5 V LVDS

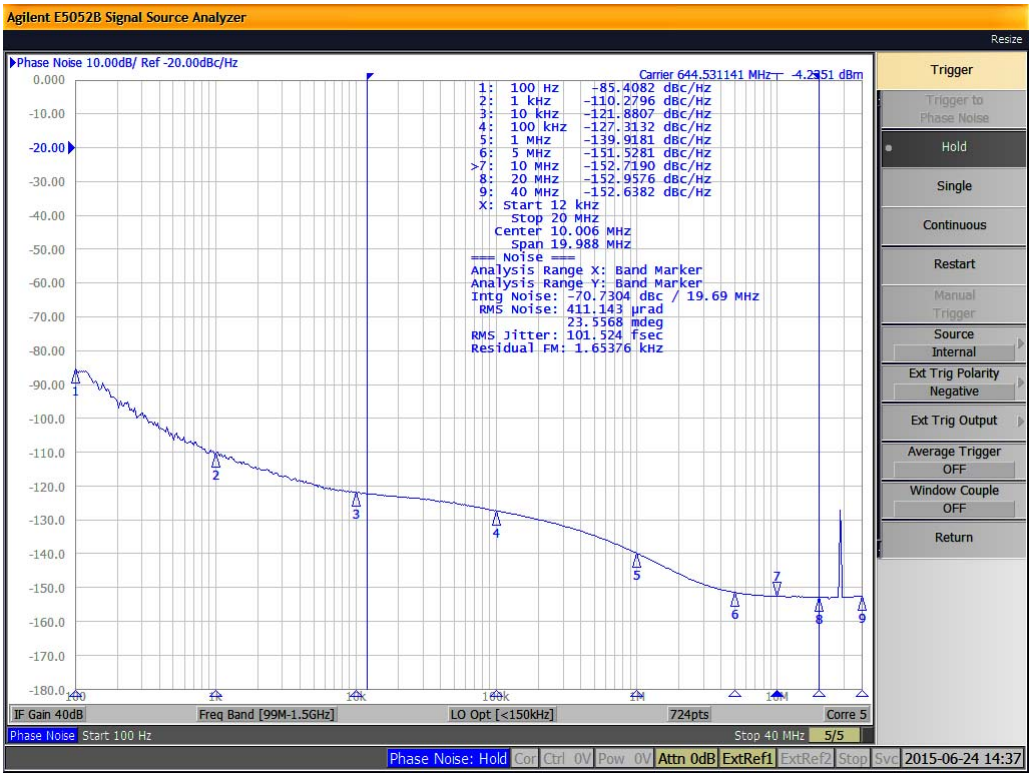


Figure 7. Input = 19.44 MHz; Output = 644.53125 MHz, 2.5 V LVDS

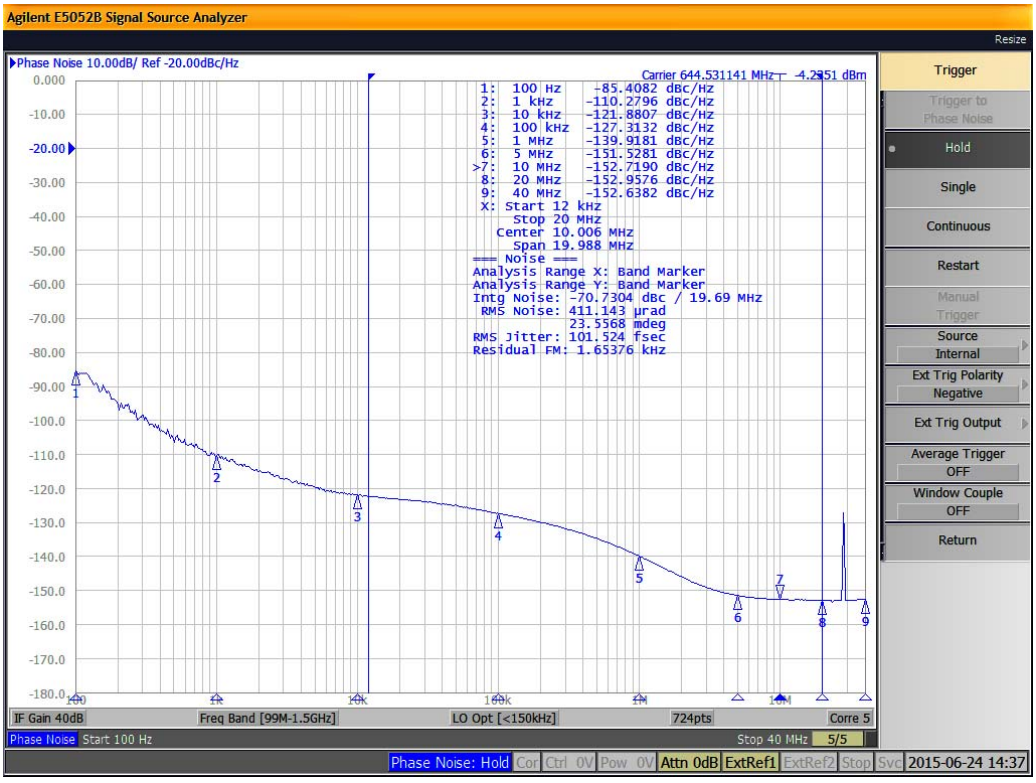


Figure 8. Input = 25 MHz; Output = 644.53125 MHz, 2.5 V LVDS

4. Detailed Block Diagram

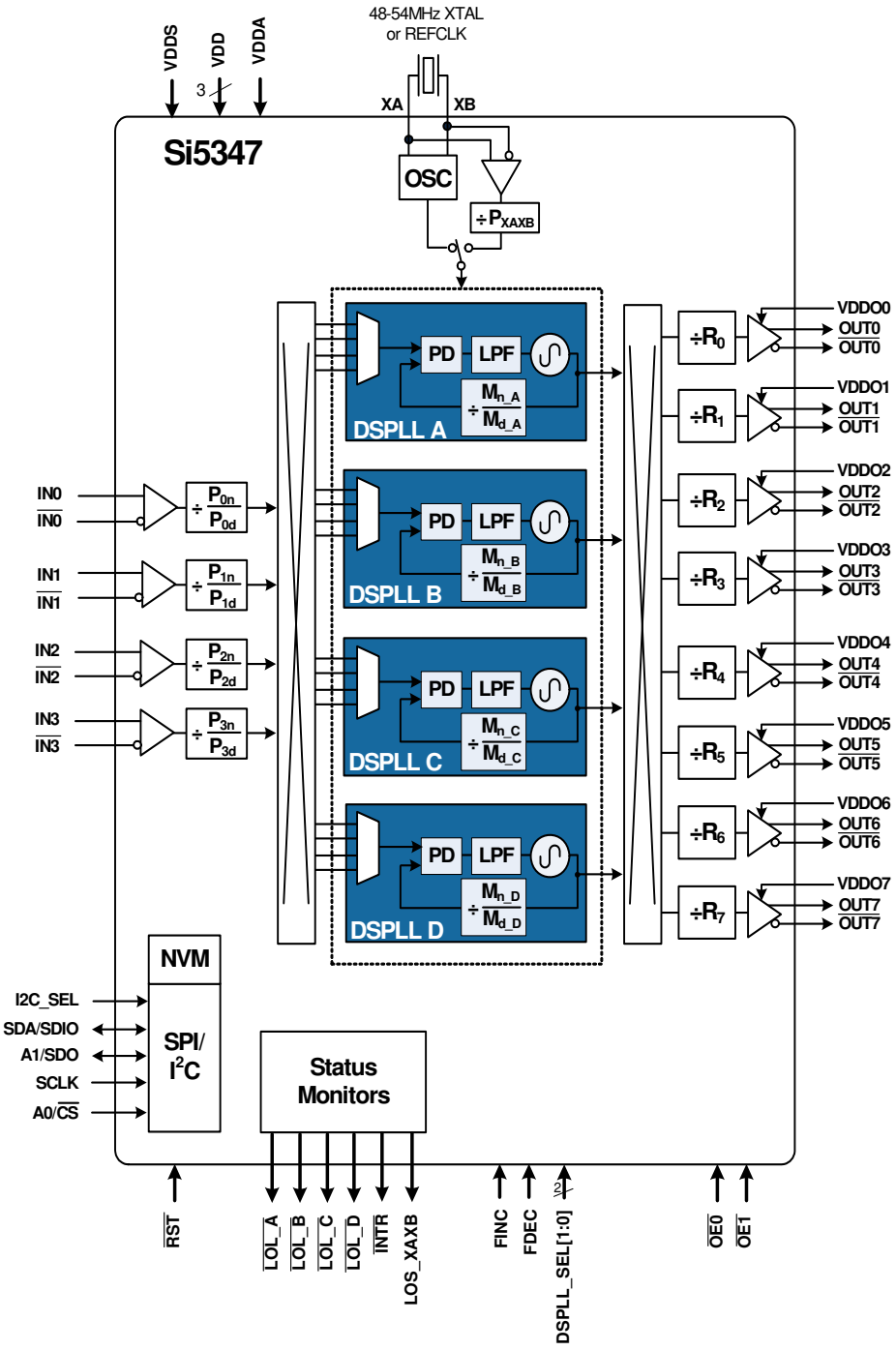


Figure 9. Si5347A/B Detailed Block Diagram

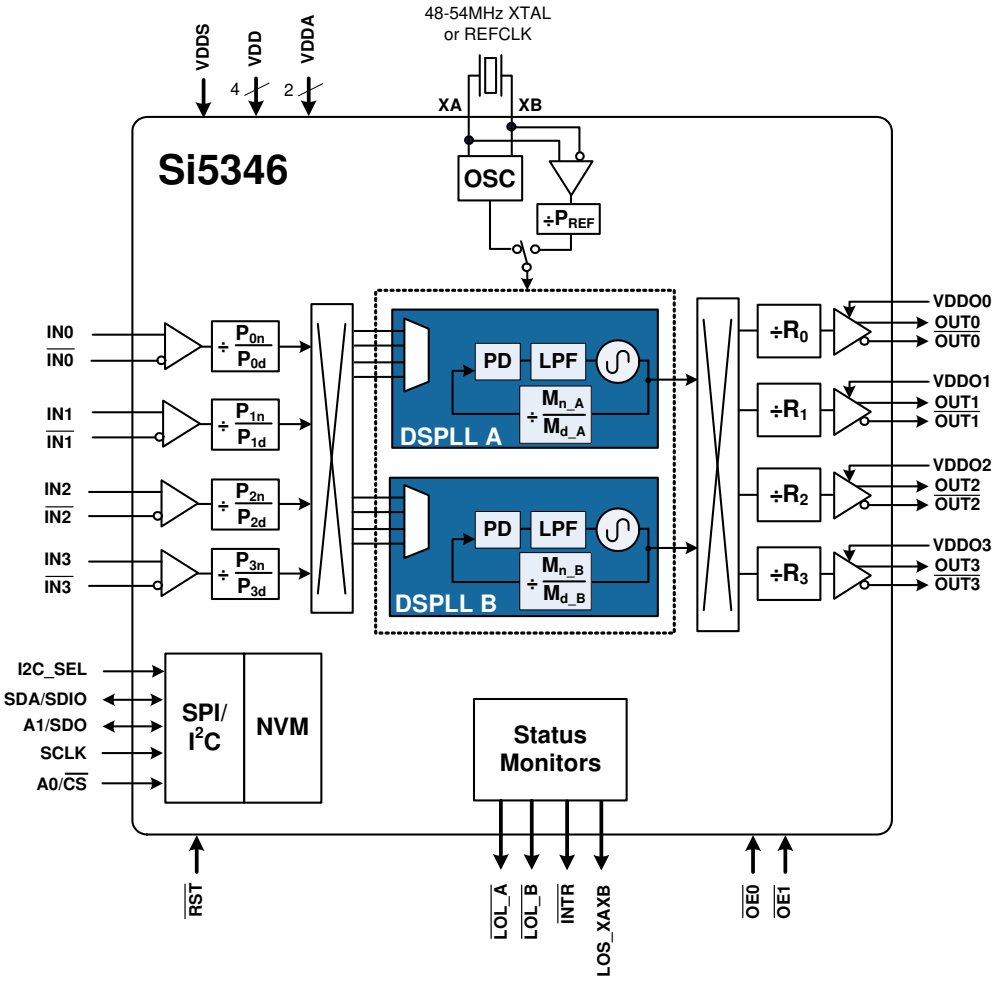


Figure 10. Si5346 Detailed Block Diagram