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Si5348 Rev D Data Sheet

Network Synchronizer for SyncE/ 1588 PTP Telecom Boundary (T-BC) and Slave (T-SC) Clocks

The Si5348 combines the industry's smallest footprint and lowest power network synchronizer clock with unmatched frequency synthesis flexibility and ultra-low jitter. The Si5348 is ideally suited for wireless backhaul, IP radio, small and macro cell wireless communications systems, and data center switches requiring both traditional and packet based network synchronization.

The three independent DSPLLs™ are individually configurable as a SyncE PLL, IEEE 1588 DCO or a general-purpose PLL for processor/FPGA clocking. The Si5348 can also be used in legacy SETS systems needing Stratum 3/3E compliance. The optional digitally controlled oscillator (DCO) mode provides precise timing adjustment to 1 ppt for 1588 (PTP) clock steering applications. The unique design of the Si5348 allows the TCXO/OCXO reference input to determine the device's frequency accuracy and stability. The Si5348 is programmable via a serial interface with in-circuit programmable non-volatile memory so it always powers up into a known configuration. Programming the Si5348 is easy with ClockBuilder Pro™ software. Factory pre-programmed devices are also available.

Applications:

- Synchronous Ethernet (SyncE) ITU-T G.8262 EEC Option 1 & 2
- Telecom Boundary Clock (T-BC) as defined by ITU-T G.8273.2
- IEEE 1588 (PTP) slave clock synchronization
- Stratum 3/3E, G.812, G.813 network synchronization

KEY FEATURES

- Three independent DSPLLs in a single monolithic IC supporting flexible SyncE/ IEEE 1588 and SETS architectures
- Ultra-low jitter of 100 fs
- Input frequency range:
  - External crystal: 48 to 54 MHz
  - REF clock: 5 to 250 MHz
  - Diff clock: 8 kHz to 750 MHz
  - LVCMOS clock: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: 1 PPS to 712.5 MHz
  - LVCMOS: 1 PPS to 250 MHz
- Meets the requirements of:
  - ITU-T G.8273.2 T-BC
  - ITU-T G.8262 (SyncE) EEC Options 1 & 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR-1244, GR-253 (Stratum-3/3E)
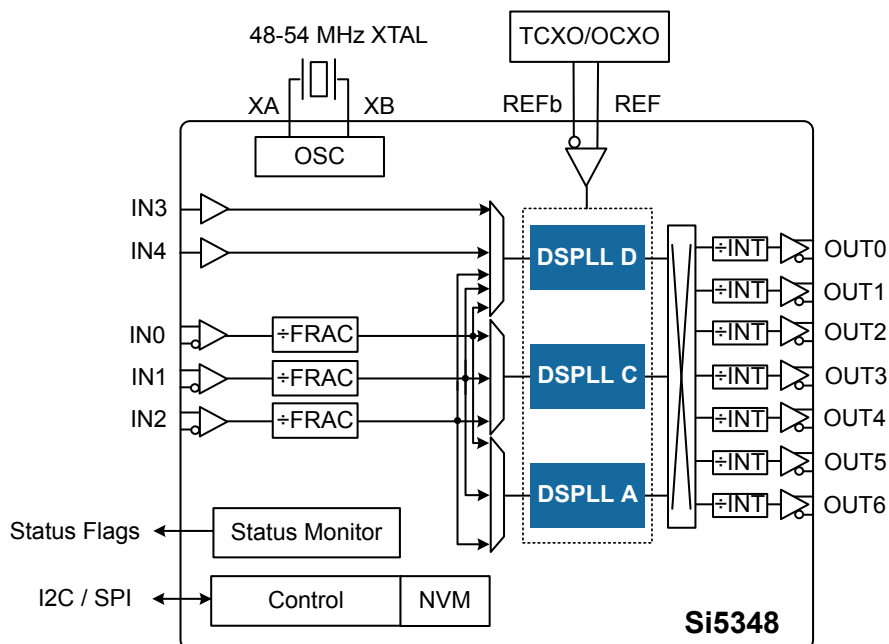
1. Feature List

The Si5348 features are listed below:

- Three independent DSPLLs in a single monolithic IC supporting flexible SyncE/IEEE 1588 and SETS architectures
- Ultra-Low Jitter
  - 100 fs typ (12 kHz to 20 MHz)
- Meets the requirements of:
  - ITU-T G.8273.2 T-BC
  - ITU-T G.8262 (SyncE) EEC Options 1 & 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR-1244, GR-253 (Stratum-3/3E)
- Each DSPLL generates any output frequency from any input frequency
- Input frequency range:
  - External crystal: 48-54 MHz
  - REF clock: 5-250 MHz
  - Diff clock: 8 kHz-750 MHz
  - LVCMOS clock: 8 kHz-250 MHz
- Output frequency range:
  - Differential: 1 PPS to 712.5 MHz
  - LVCMOS: 1 PPS to 250 MHz

- Pin or software controllable DCO on each DSPLL with typical resolution to 1 ppt/step
- TCXO/OCXO reference input determines DSPLL free-run/holdover accuracy and stability
- Programmable jitter attenuation bandwidth per DSPLL: 0.001 Hz to 4 kHz
- Highly configurable output drivers: LVDS, LVPECL, LVCMOS, HCSL, CML
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output supply pins: 3.3 V, 2.5 V, or 1.8 V
- Built-in power supply filtering
- Status monitoring: LOS, OOF, LOL
- Serial Interface: I^{2}C or SPI (3-wire or 4-wire)
- ClockBuilder^{TM} Pro software tool simplifies device configuration
- 5 input, 7 output, 64 QFN
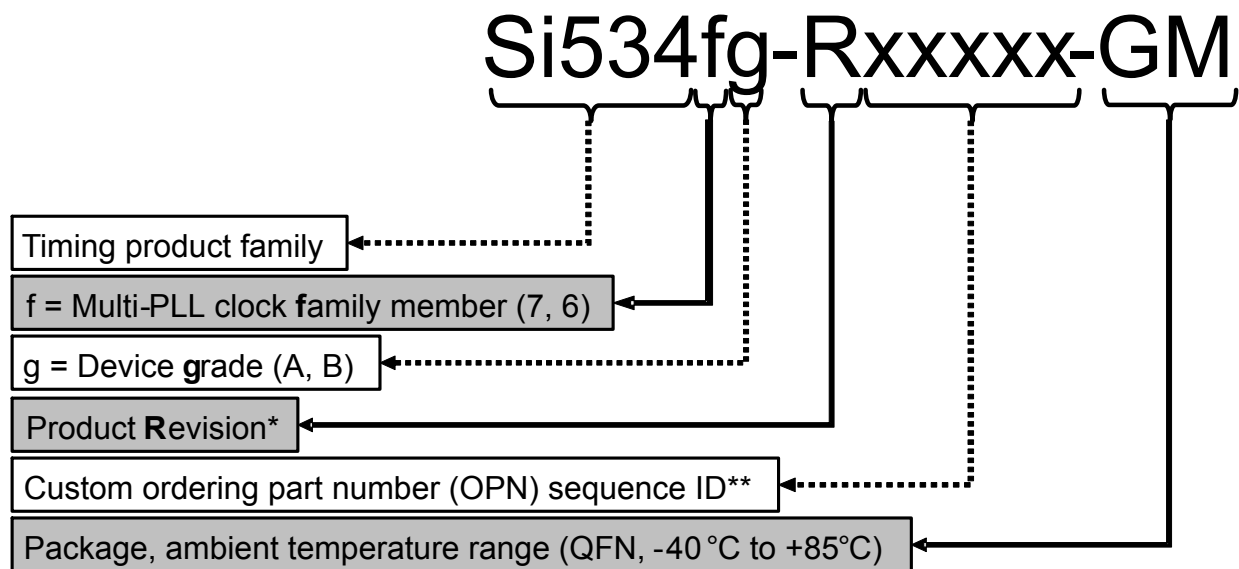- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Ordering Guide

Table 2.1. Si5348 Ordering Guide

Ordering Part Number	# of DSPLLs	Output Clock Frequency Range	Package	RoHS-6, Pb-Free	Temperature Range
Si5348A-D-GM [1, 2]	3	1 Hz to 712.5 MHz	64-Lead 9x9 QFN	Yes	–40 to 85 °C
Si5348B-D-GM [1, 2]		1 Hz to 350 MHz			
Si5348-D-EVB	—	—	Evaluation Board	—	—
SiOCXO1-EVB	—	12.800 MHz	OCXO Evaluation Board	—	—

Note:
1. Add an R at the end of the device part number to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by the ClockBuilder Pro software. Part number format is: Si5348A-Dxxxxx-GM, where "xxxxx" is a unique numerical sequence representing the pre-programmed configuration.

Si534fg-Rxxxxx-GM

Timing product family

f = Multi-PLL clock **f**amily member (7, 6)

g = Device **g**rade (A, B)

Product **R**evision*

Custom ordering part number (OPN) sequence ID**

Package, ambient temperature range (QFN, -40 °C to +85°C)

*See Ordering Guide table for current product revision
** 5 digits; assigned by ClockBuilder Pro

Figure 2.1. Ordering Part Number Fields

3. Functional Description

The Si5348 offers three DSPLLs that have identical performance and flexibility which can be independently configured and controlled through the serial interface. Each of the DSPLLs support locked, free-run, and holdover modes of operation with an optional DCO mode for IEEE 1588 applications. The device requires an external crystal and an external reference (TCXO or OCXO) to operate. The reference input (REF/REFb) determines the frequency accuracy and stability while in free-run and holdover modes. The external crystal completes the internal oscillator circuit (OSC) which is used by the DSPLL for intrinsic jitter performance. There are three main inputs (IN0 - IN2) for synchronizing the DSPLLs. Input selection can be manual or automatically controlled using an internal state machine. Two additional manually selected inputs are available to DSPLL D. Any of the output clocks (OUT0 to OUT6) can be configured to any of the DSPLLs using a flexible crosspoint connection. Output 6 is the only output that can be configured for a 1 Hz output to support 1 PPS.

3.1 Standards Compliance

Each of the DSPLLs meet the requirements of ITU-T G.8262 (SyncE), G.812, G.813, G.8273.2 (T-BC), in addition to Telcordia GR-1244 and GR-253 as shown in the compliance report. The DCO feature enables IEEE1588 (PTP) implementations in addition to hybrid SyncE + IEEE1588 (T-BC).

3.2 Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.3 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter and wander attenuation. Register configurable DSPLL loop bandwidth settings of 1 mHz to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

Table 3.1. Loop Bandwidth Requirements for North America

SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Loop Bandwidth
GR-253 Stratum 3E	G.812 Type III	—	0.001 Hz
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	<0.1 Hz
—	G.813 Option 1	G.8262 EEC Option 1	1 - 10 Hz

3.3.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The fastlock feature can be enabled or disabled independently for each of the DSPLLs.

3.4 Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in . The following sections describe each of these modes in greater detail.

3.4.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can either affect all or each DSPLL individually.
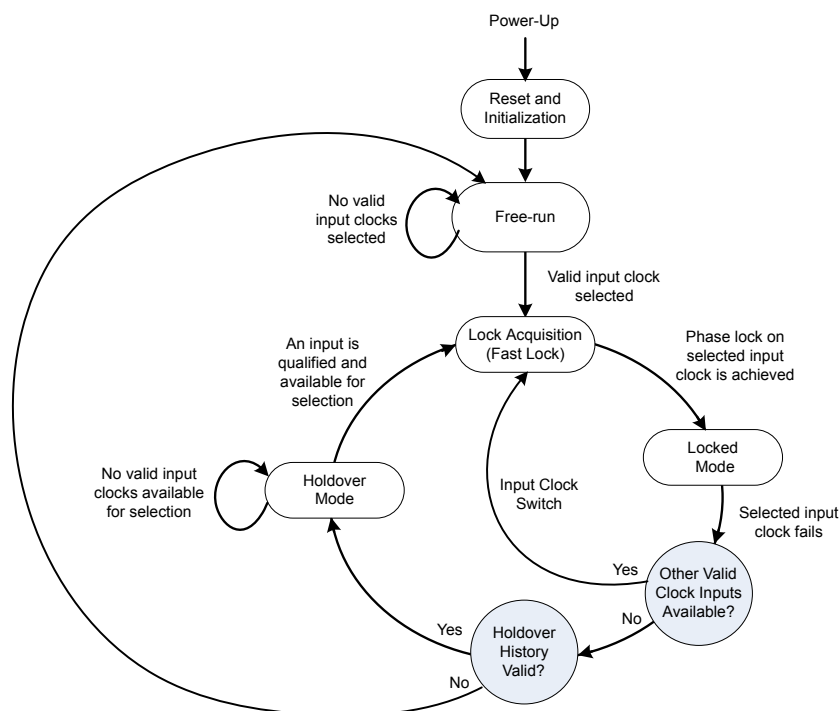

Figure 3.1. Modes of Operation

3.4.2 Free-run Mode

Once power is applied to the Si5348 and initialization is complete, all three DSPLLs will automatically enter freerun mode. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the clock source at the reference inputs (REF/REFb). A TCXO or OCXO is recommended for applications that need frequency accuracy and stability to meet the synchronization standards as shown in the following table:

Table 3.2. Free-run Accuracy for North American and European Synchronization Standards

| SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Free-run Accuracy
GR-253 Stratum 3E	G.812 Type III	—	±4.6 ppm
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	
—	G.813 Option 1	G.8262 EEC Option 1	

3.4.3 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

3.4.4 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own LOLb pin and status bit to indicate when lock is achieved. Refer to 3.8.6 LOL Detection for more details on the operation of the loss of lock circuit.

3.4.5 Holdover Mode

Any of the DSPLLs will automatically enter Holdover Mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.
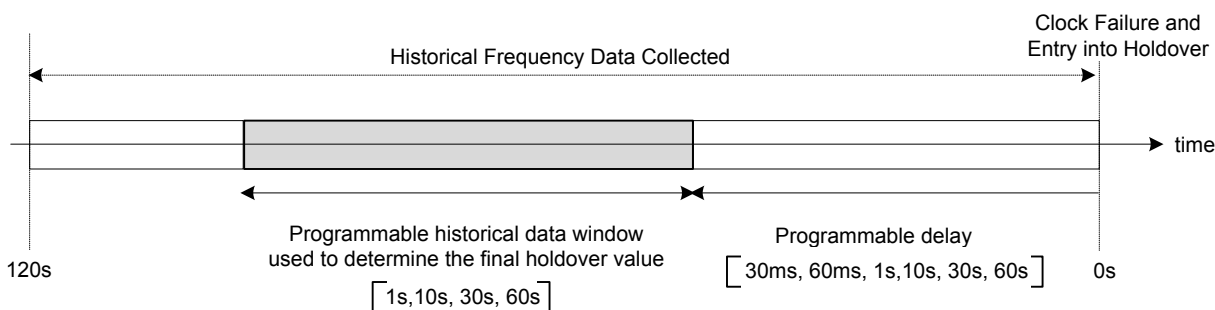
Figure 3.2. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF/REFb pins. If the clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching see 3.7.6 Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

3.5 Digitally-Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in pre-defined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in locked mode. The DCO mode is mainly used in IEEE1588 (PTP) applications where a clock needs to be generated based on recovered timestamps. In this case timestamps are recovered by the PHY/MAC. A processor containing servo software controls the DCO to close the timing loop between the master and slave nodes. The processor has the option of using the FINC/FDEC pin controls to update the DCO frequency or by controlling it through the serial interface.

3.5.1 Frequency Increment/Decrement Using Pin Controls (FINC, FDEC)

Controlling the output frequency with pin controls is available. This feature involves asserting the FINC or FDEC pins to step (increment or decrement) the DSPLL's output frequency. Both the step size and DCO selection (A, C, D) is made through the serial interface by writing to register bits.
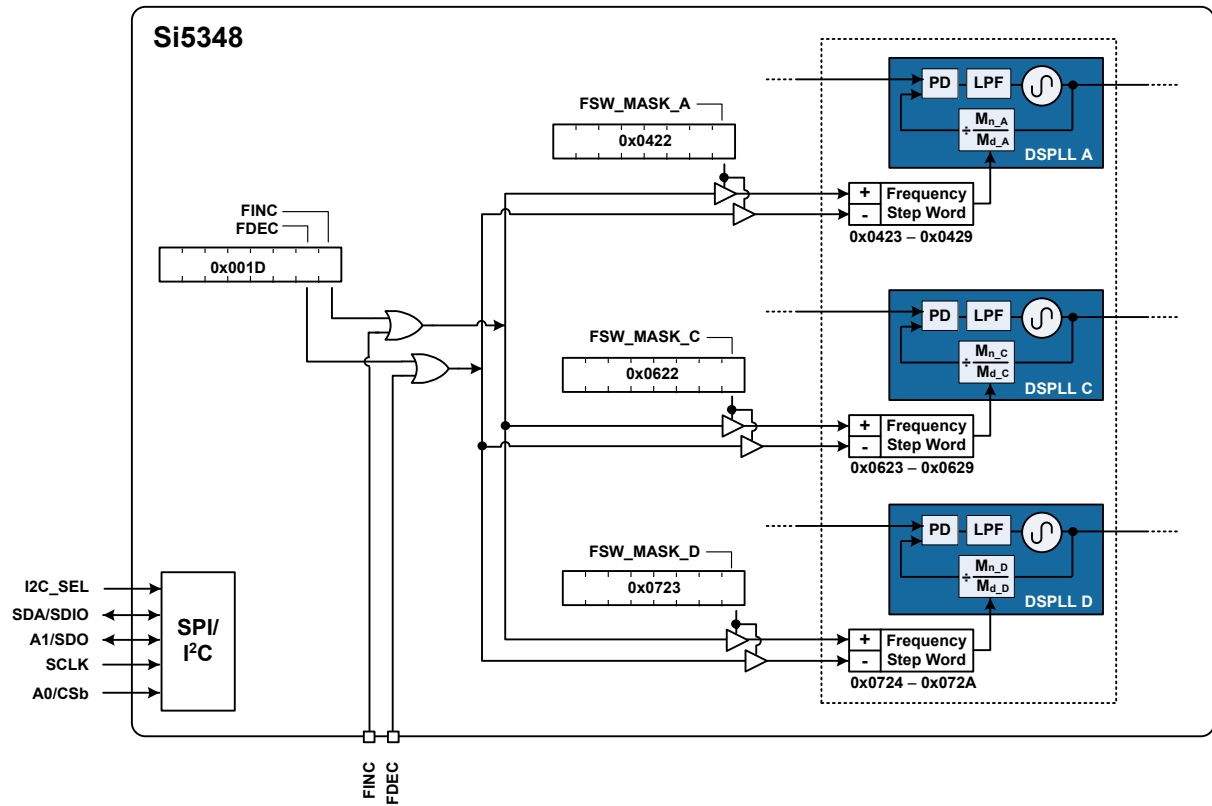
Figure 3.3. Controlling the DCO Mode By Pin Control

3.5.2 Frequency Increment/Decrement Using the Serial Interface

Controlling the DSPLL frequency through the serial interface is available. This feature involves asserting the FINC or FDEC bits to activate the frequency change defined by the frequency step word. A set of mask bits selects the DSPLL(s) that is affect by the frequency change.

3.6 External Reference (XA/XB, REF/REFb)

The external crystal at the XA/XB pins determines jitter performance of the output clocks, and the external reference clock at the REF/REFb pins determines the frequency accuracy, wander and stability during free-run or holdover modes. Jitter from the external clock on the REF/REFb pins will have little effect on the output jitter performance, depending upon the selected bandwidth.
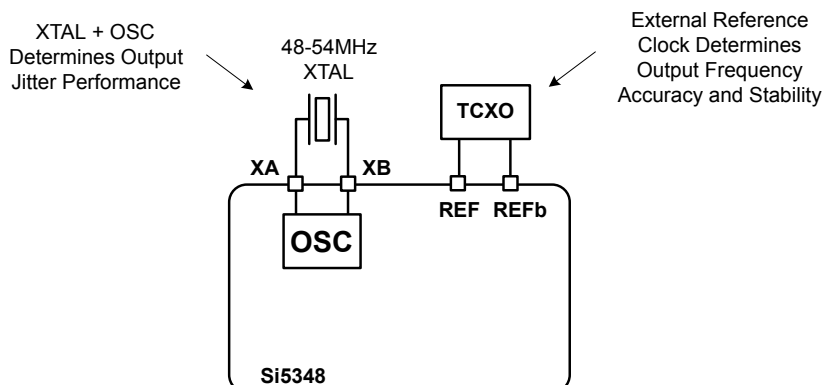

Figure 3.4. External Reference Connections

3.6.1 External Crystal (XA/XB)

The external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLLs. The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. The Si5348 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Although **not** recommended, the device can also accommodate an external clock at the XA/XB pins instead of a crystal. Selection between the external crystal or clock is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in this mode. Refer to Table 5.12 Crystal Specifications[1] on page 36 for reference clock requirements when using this mode. The Si5348 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.
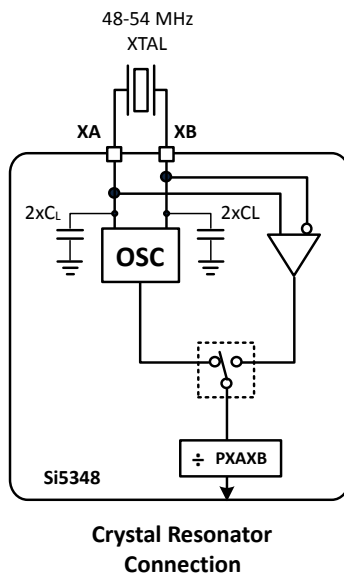

Figure 3.5. Crystal Resonator Connections

3.6.2 External Reference (REF/REFb)

The external reference at the REF/REFb pins is used to determine output frequency accuracy and stability during free-run and holdover modes. This reference is usually from a TCXO or OCXO and can be connected differentially or single-ended as shown in the figure below:
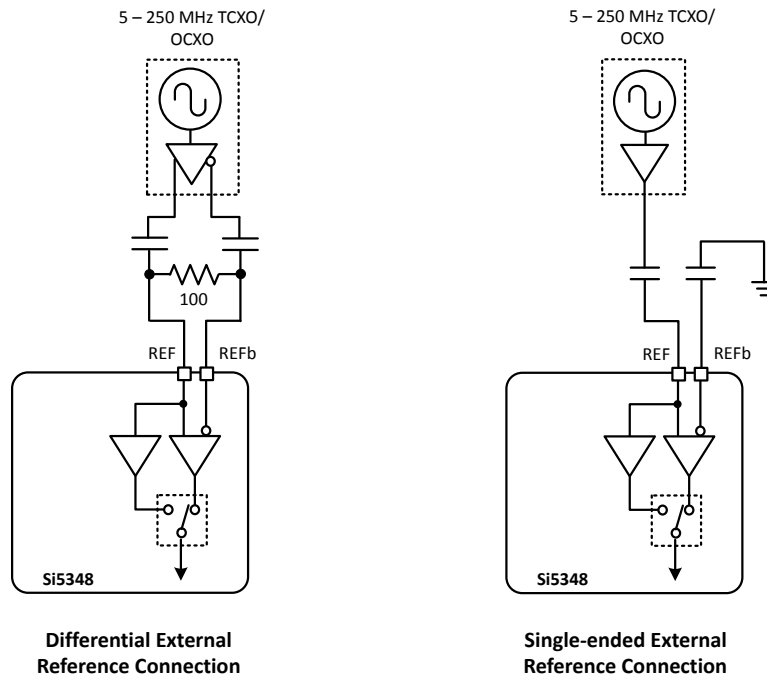

Differential External Reference Connection

Single-ended External Reference Connection

Figure 3.6. External Reference Connections

3.7 Inputs (IN0, IN1, IN2, IN3, IN4)

There are three inputs (IN0, IN1, and IN2) that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows inputs IN0-IN2 to connect to any of the DSPLLs as shown in the figure below. DSPLL D has two additional inputs (IN3-IN4) that can be manually selected. IN3 and IN4 are CMOS only inputs. If both IN3 and IN4 are used, they must be the same frequency.
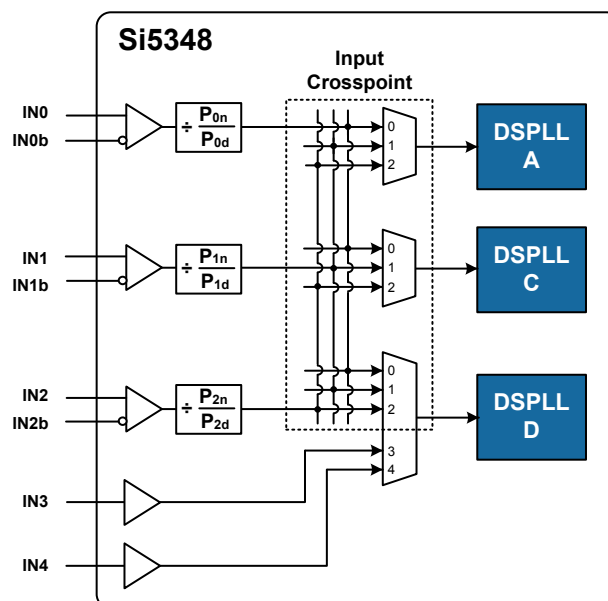

Figure 3.7. DSPLL Input Selection Crosspoint

3.7.1 Input Selection

Input selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine. Note that inputs IN3-IN4 can only be manually selected by DSPLL D.

3.7.2 Manual Input Selection

In manual mode the input selection is made by writing to a register. IN0-IN2 is available to DSPLL A and C, IN0-IN4 is available to DSPLL D. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode.

3.7.3 Automatic Input Selection

When configured in this mode, the DSPLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each DSPLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). Only inputs that do not assert both the LOS and OOF monitors can be selected for synchronization by the automatic state machine. The DSPLL(s) will enter either holdover or freerun mode if there are no valid inputs available. Note that automatic input selection only applies to IN0-IN2. If the Si5348 is locked to either IN3 or IN4 and the input clock fails, the Si5348 will not go into holdover.

3.7.4 Input Configuration and Terminations

Inputs IN0-IN2 can be configured as differential or single-ended LVCMOS. Inputs IN3-IN4 are single-ended only. The recommended input termination schemes are shown in the figure below. Standard 50% duty cycle signals must be ac-coupled, while low duty cycle Pulsed CMOS signals can be dc-coupled. Unused inputs can be disabled and left unconnected when not in use.
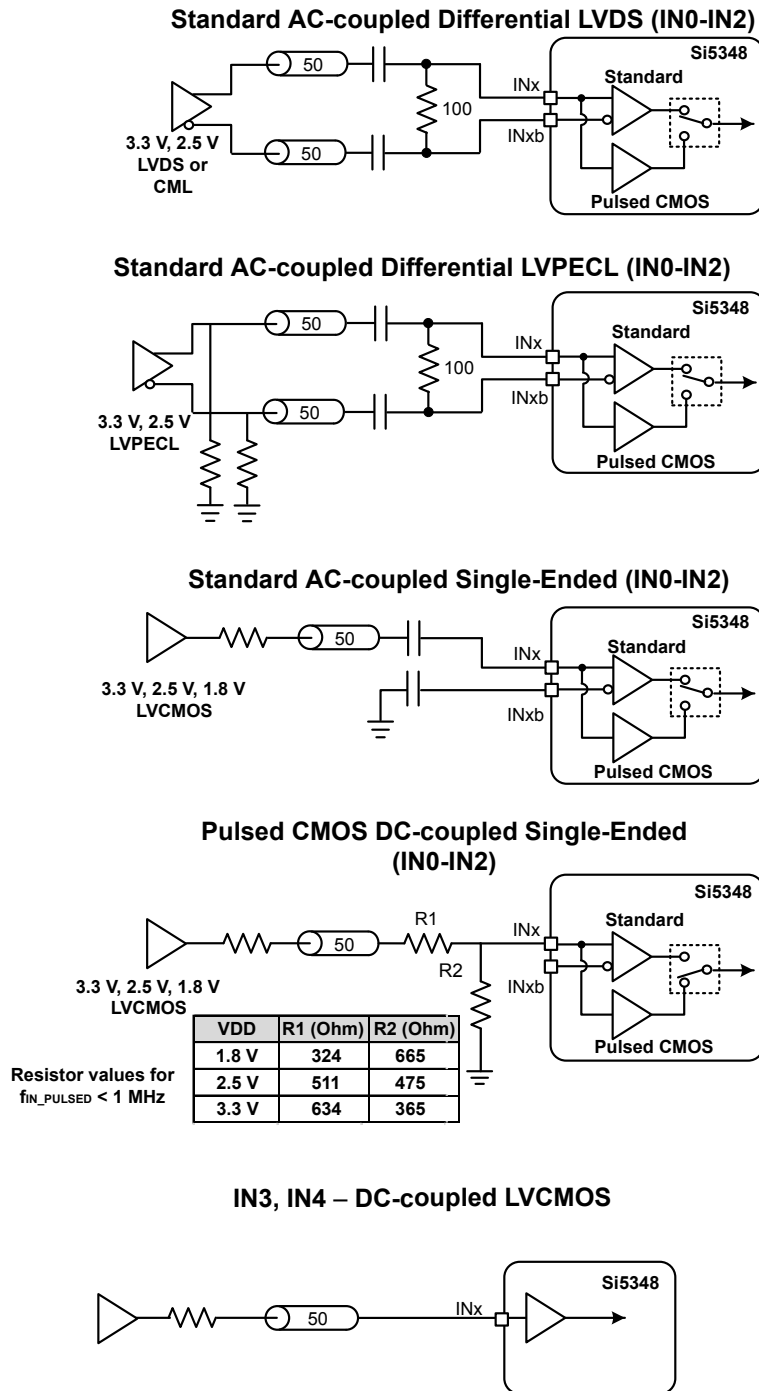
Standard AC-coupled Differential LVDS (IN0-IN2)

Standard AC-coupled Differential LVPECL (IN0-IN2)

Standard AC-coupled Single-Ended (IN0-IN2)

Pulsed CMOS DC-coupled Single-Ended (IN0-IN2)

VDD	R1 (Ohm)	R2 (Ohm)
1.8 V	324	665
2.5 V	511	475
3.3 V	634	365

Resistor values for f_{IN_PULSED} < 1 MHz

IN3, IN4 – DC-coupled LVCMOS

Figure 3.8. Termination of Differential and LVCMOS Input Signals

3.7.5 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that they have to be exactly at the same frequency, or at an integer frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz. Hitless switching can be enabled on a per DSPLL basis. Clock inputs 3 and 4 do not support hitless switching.

### 3.7.6 Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover, see 3.4.5 Holdover Mode.

3.7.7 Glitchless Input Switching

The DSPLLs have the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if it is enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition. All clock inputs, including 3 and 4, support glitchless input switching.

3.7.8 Synchronizing to Gapped Input Clocks

Each of the DSPLLs support locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter, so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in the figure below:

Gapped Input Clock

**100 MHz clock
1 missing period every 10**

Periodic Output Clock

90 MHz non-gapped clock
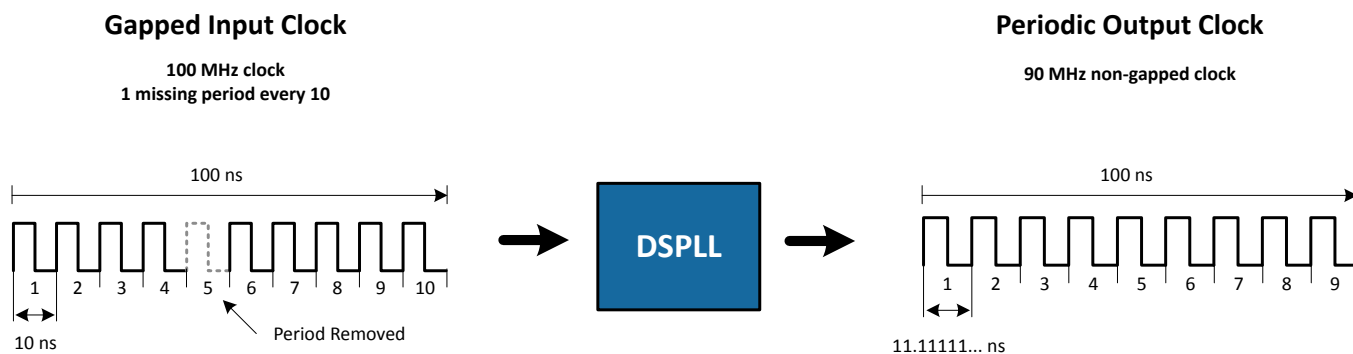
Figure 3.9. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 5.8 Performance Characteristics on page 31 when the switch occurs during a gap in either input clock.

3.8 Fault Monitoring

Three input clocks (IN0, IN1, IN2) and the reference input (REF/REFb) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has an LOL indicator, which is asserted when synchronization is lost with their selected input clock. Note that IN3 and IN4 are not monitored.
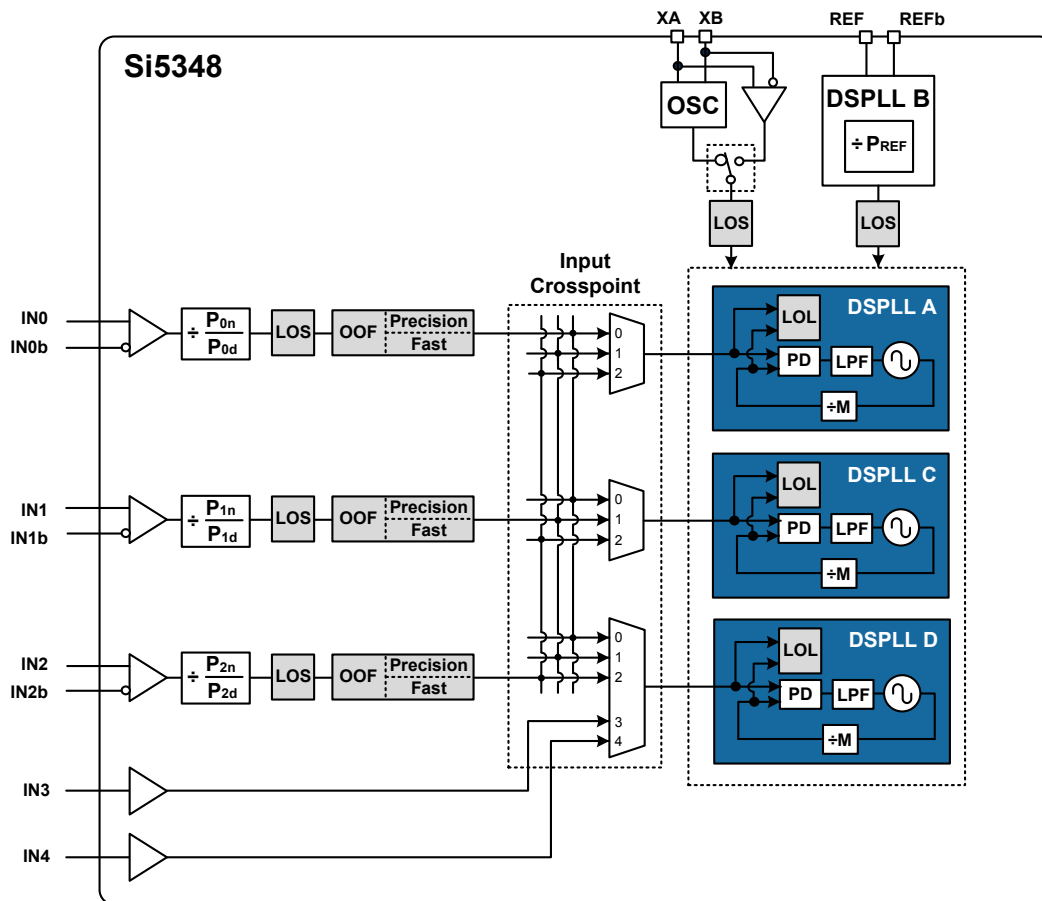

Figure 3.10. Si5348 Fault Monitors

3.8.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.
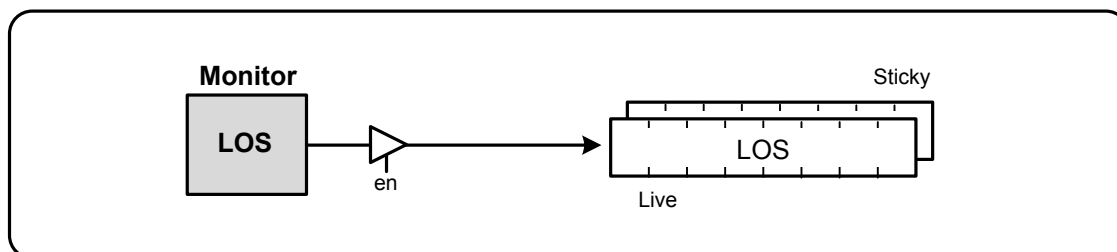

Figure 3.11. LOS Status Indicators

3.8.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.8.3 OOF Detection

Input clocks IN0, IN1, IN2 are monitored for frequency accuracy with respect to an OOF reference, which it considers as its "0_ppm" reference. Since a TCXO or OCXO will be connected to the REF input, most applications will declare the REF input to be the OOF reference. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.
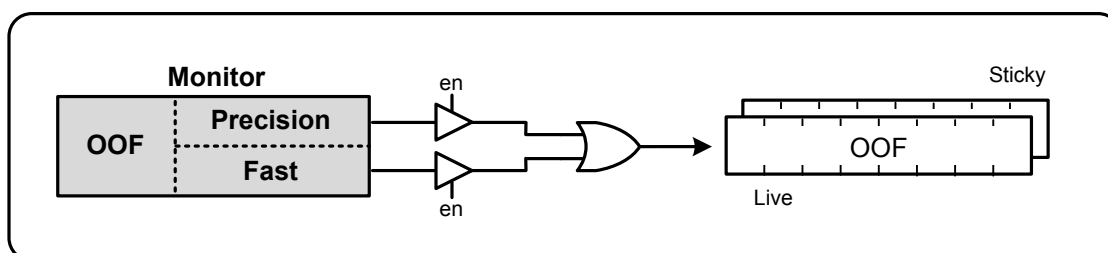
Figure 3.12. OOF Status Indicator

3.8.4 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range, which is register configurable up to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 – IN2) as the 0 ppm OOF reference instead of the REF/REFb pins is available. This option is register-configurable. XA/XB can also be used as the 0 ppm reference.
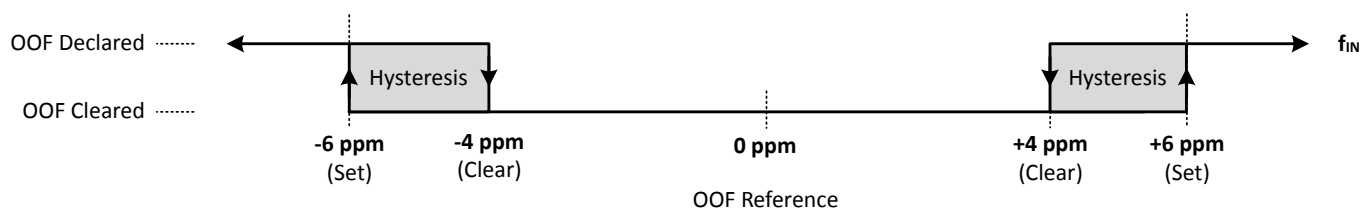
Figure 3.13. Example of Precise OOF Monitor Assertion and De-assertion Triggers

3.8.5 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

3.8.6 LOL Detection

There is an LOL monitor for each of the DSPLLs. The LOL monitor asserts the LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs (LOL_Ab, LOL_Cb, LOL_Db) and also for the reference. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.
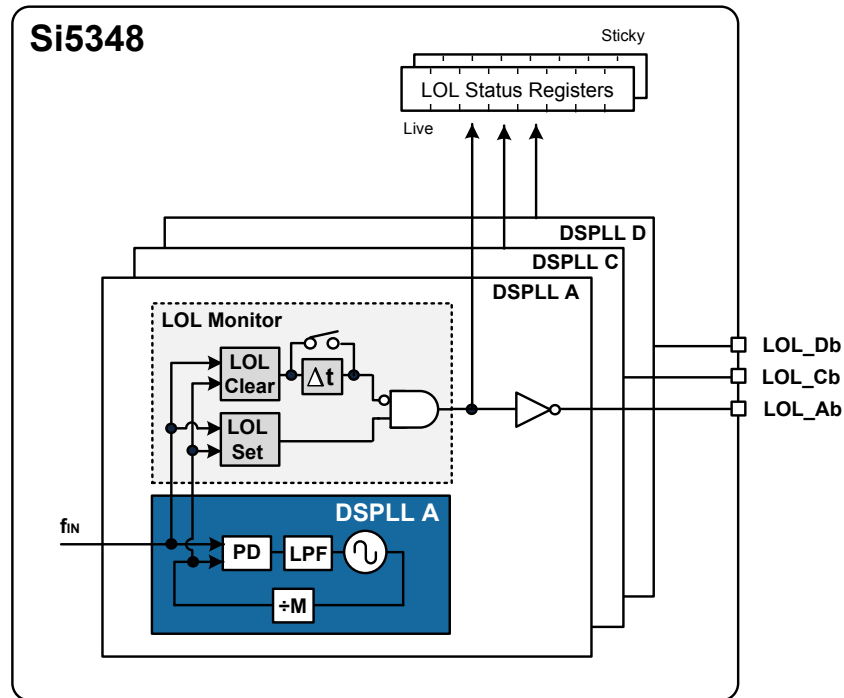

Figure 3.14. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity, which is register-configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 1 ppm frequency difference is shown in Figure 3.15 LOL Set and Clear Thresholds on page 14.
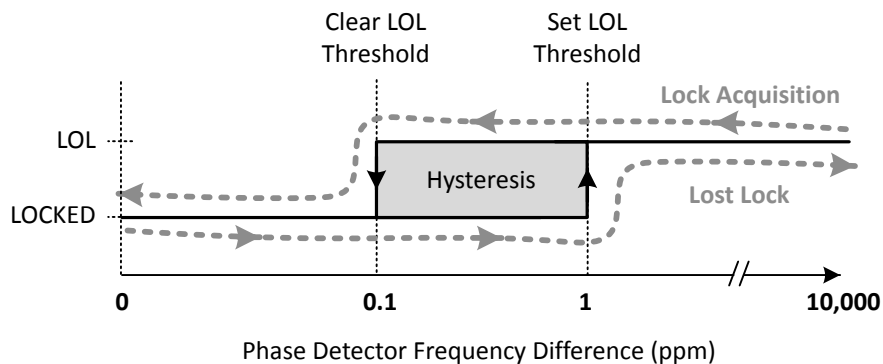

Figure 3.15. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilderPro utility.

3.8.7 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.
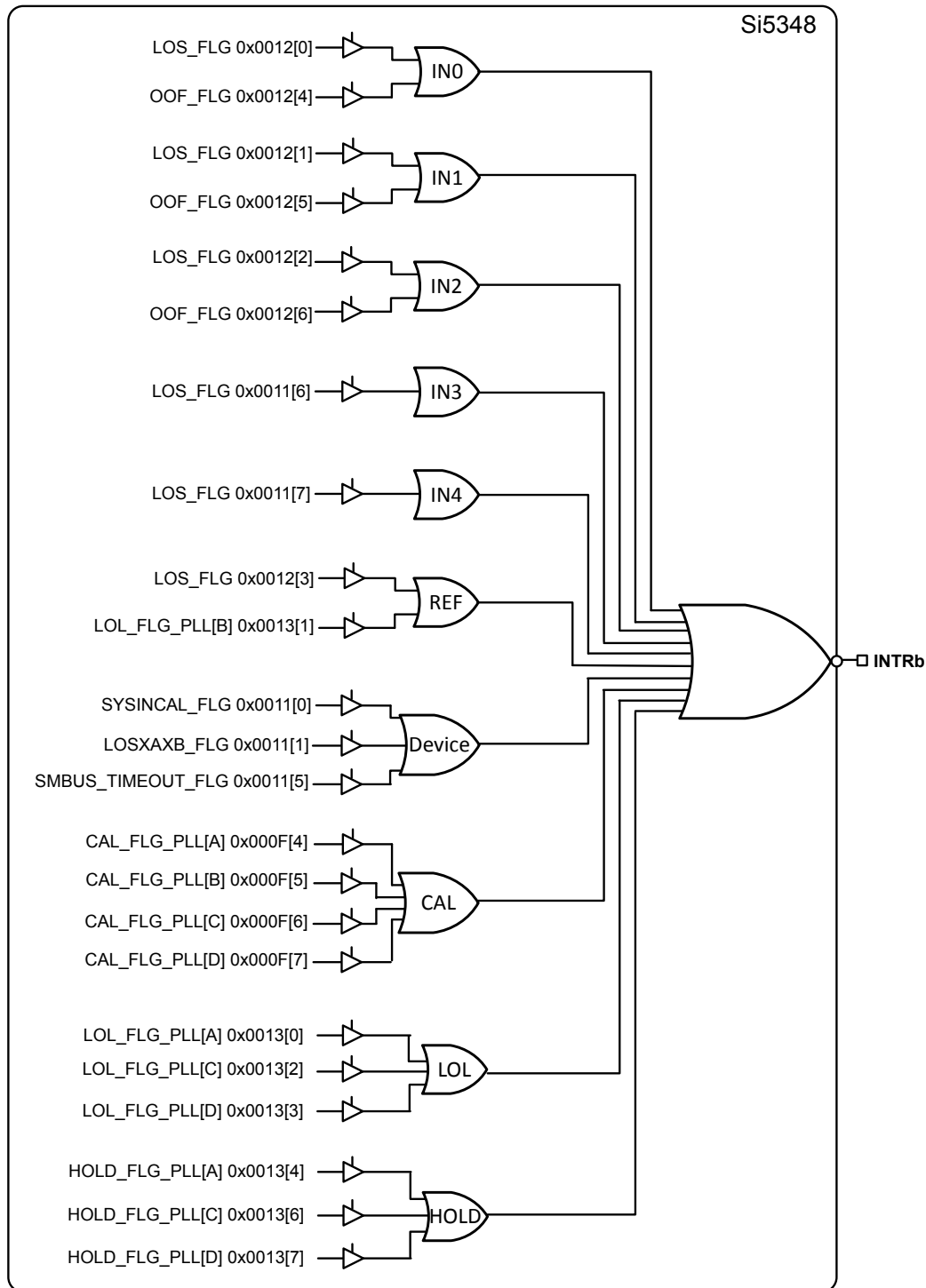
Figure 3.16. Interrupt Triggers and Masks

3.9 Outputs

The Si5348 supports seven differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 14 single-ended outputs, or a combination of differential and single-ended outputs.

3.9.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power-up.
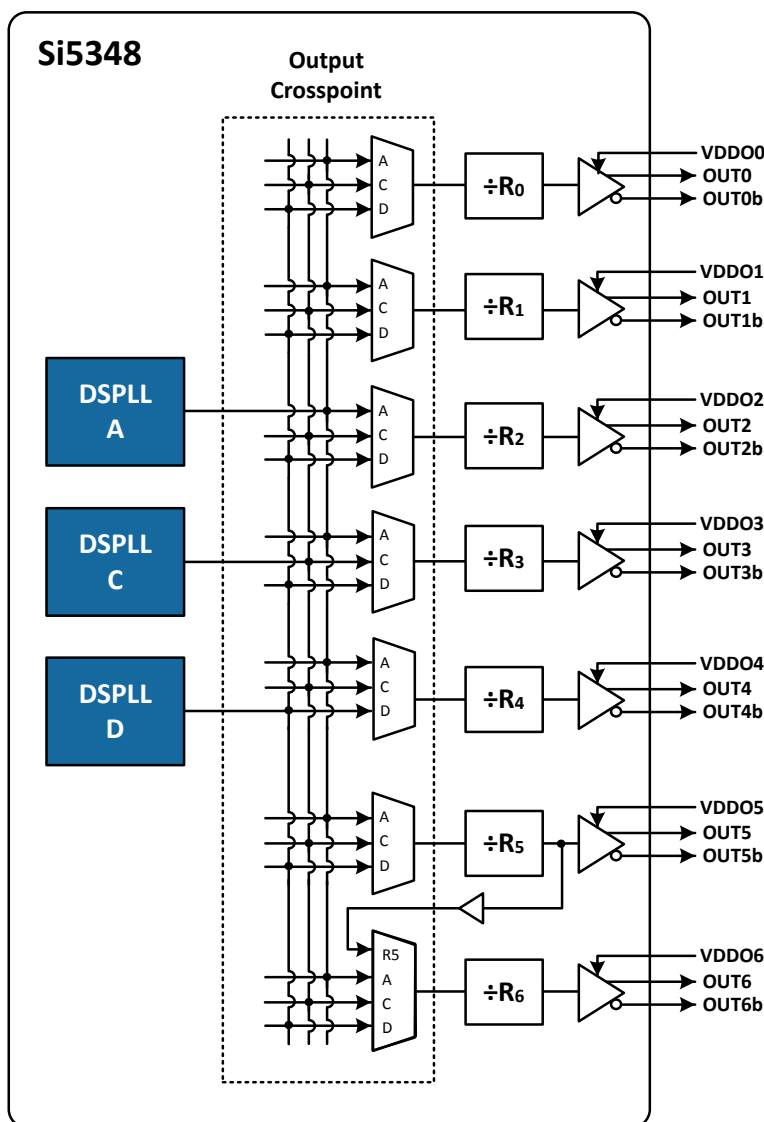

Figure 3.17. DSPLL to Output Driver Crosspoint

3.9.2 Support For 1 Hz Output

Output 6 of the Si5348 can be configured to generate a 1 Hz clock by cascading the R5 and R6 dividers. Output 5 is still usable in this case but is limited to a maximum frequency of 33.5 MHz. ClockBuilder Pro automatically determines the optimum configuration when generating a 1 Hz output (1 PPS).
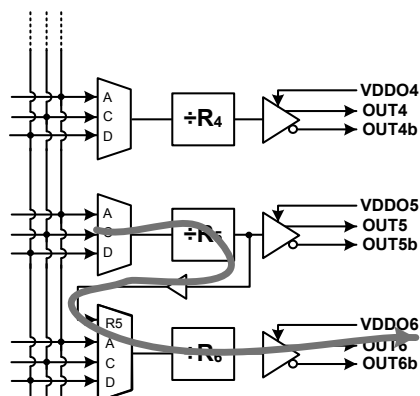

Figure 3.18. Generating a 1 Hz Output using the Si5348

3.9.3 Differential Output Terminations

Note: In this document, the terms LVDS and LVPECL refer to driver formats that are compatible with these signaling standards.

The differential output drivers support both ac-coupled and dc-coupled terminations, as shown in the figure below:
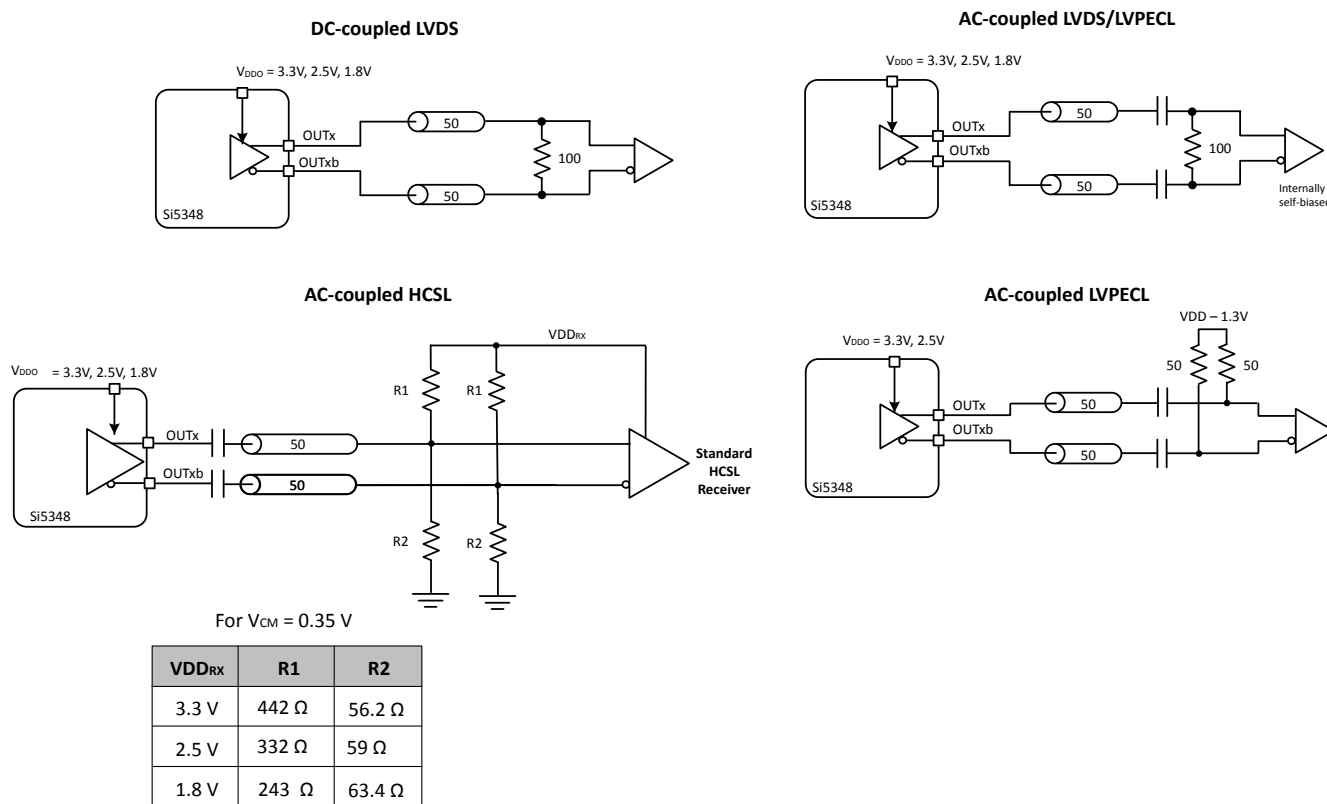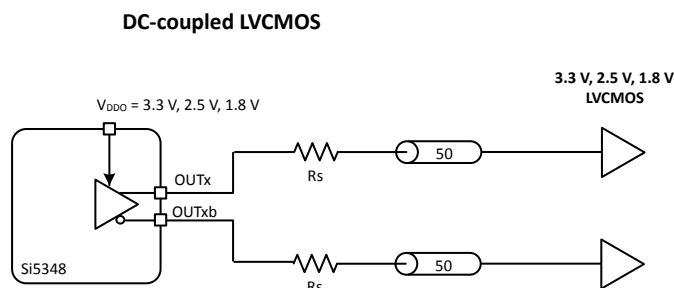

VDD$_{RX}$	R1	R2
3.3 V	442 Ω	56.2 Ω
2.5 V	332 Ω	59 Ω
1.8 V	243 Ω	63.4 Ω

Figure 3.19. Supported Differential Output Terminations

3.9.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled, as shown in the figure below.

DC-coupled LVCMOS

Figure 3.20. LVCMOS Output Terminations

3.9.5 Output Signal Format

The differential output amplitude and common mode voltage are both programmable and compatible with a wide variety of signal formats, including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 14 single-ended outputs or a combination of differential and single-ended outputs.

3.9.6 Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc-coupling the output drivers.

3.9.7 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below. Note that selecting a lower source impedance may result in higher output power consumption.

Table 3.3. Typical Output Impedance (Z_S)

VDDO	CMOS_DRIVE_Selection		
	OUTx_CMOS_DRV=1	OUTx_CMOS_DRV=2	OUTx_CMOS_DRV=3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

3.9.8 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

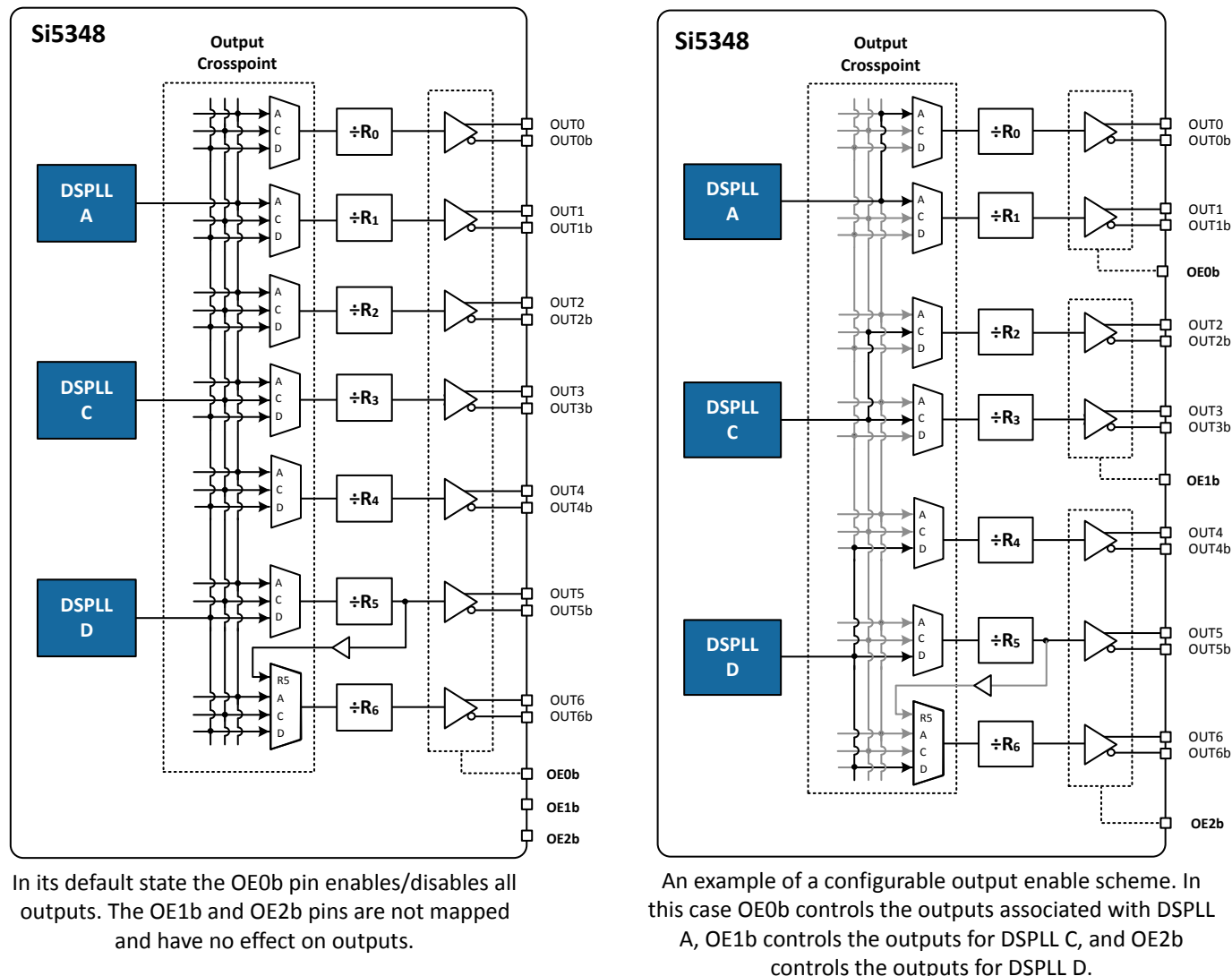### 3.9.9 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable, which enables complementary clock generation and/or inverted polarity with respect to other output drivers.

3.9.10 Output Enable/Disable

The Si5348 allows enabling/disabling outputs by pin or register control, or a combination of both. Three output enable pins are available (OE0b, OE1b, OE2b). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0b controls all of the outputs while OE1b and OE2b remain unmapped and has no effect until configured. The figure below shows an example of an output enable mapping scheme that is register configurable and can be stored in NVM as the default at power-up.

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the OEb pin(s) has them enabled. By default the output enable register settings are configured to allow the OEb pins to have full control.

In its default state the OE0b pin enables/disables all outputs. The OE1b and OE2b pins are not mapped and have no effect on outputs.

An example of a configurable output enable scheme. In this case OE0b controls the outputs associated with DSPLL A, OE1b controls the outputs for DSPLL C, and OE2b controls the outputs for DSPLL D.

Figure 3.21. Example of Configuring Output Enable Pins

3.9.11 Output Disable During LOL

By default a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.9.12 Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

3.9.13 Output Driver State When Disabled

The disabled state of an output driver is register configurable as disable low or high.

3.9.14 Synchronous/Asynchronous Output Disable

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

3.9.15 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.10 Power Management

Unused inputs, output drivers, and DSPLLs can be powered down when unused. Contact your local representative to access the Si5348 Reference Manual and ClockBuilder Pro configuration utility for details.

3.11 In-Circuit Programming

The Si5348 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Contact your local representative to access the Si5348 Reference Manual for a detailed procedure for writing registers to NVM.

3.12 Serial Interface

Configuration and operation of the Si5348 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire mode. Contact your local representative to access the Si5348 Reference Manual for details.

3.13 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-pre-programmed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will typically ship in about two weeks.

3.14 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-programmed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at www.si-labs.com, you will be notified whenever changes are made and what the impact of those changes are. This update process will ulti-mately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Si5348 Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Silicon Labs applications engineer for assis-tance. One example of this type of feature or custom setting is the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in the table below:

Table 3.4. Setting Overrides

Location	Name	Type	Target	Dec Value	Hex Value
0×0435[0]	FORCE_HOLD_PLLA	No NVM	N/A	1	0×1
0×0B48[4:0]	OOF_DIV_CLK_DIS	User	OPN and EVB	31	0×1F

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the figure below:
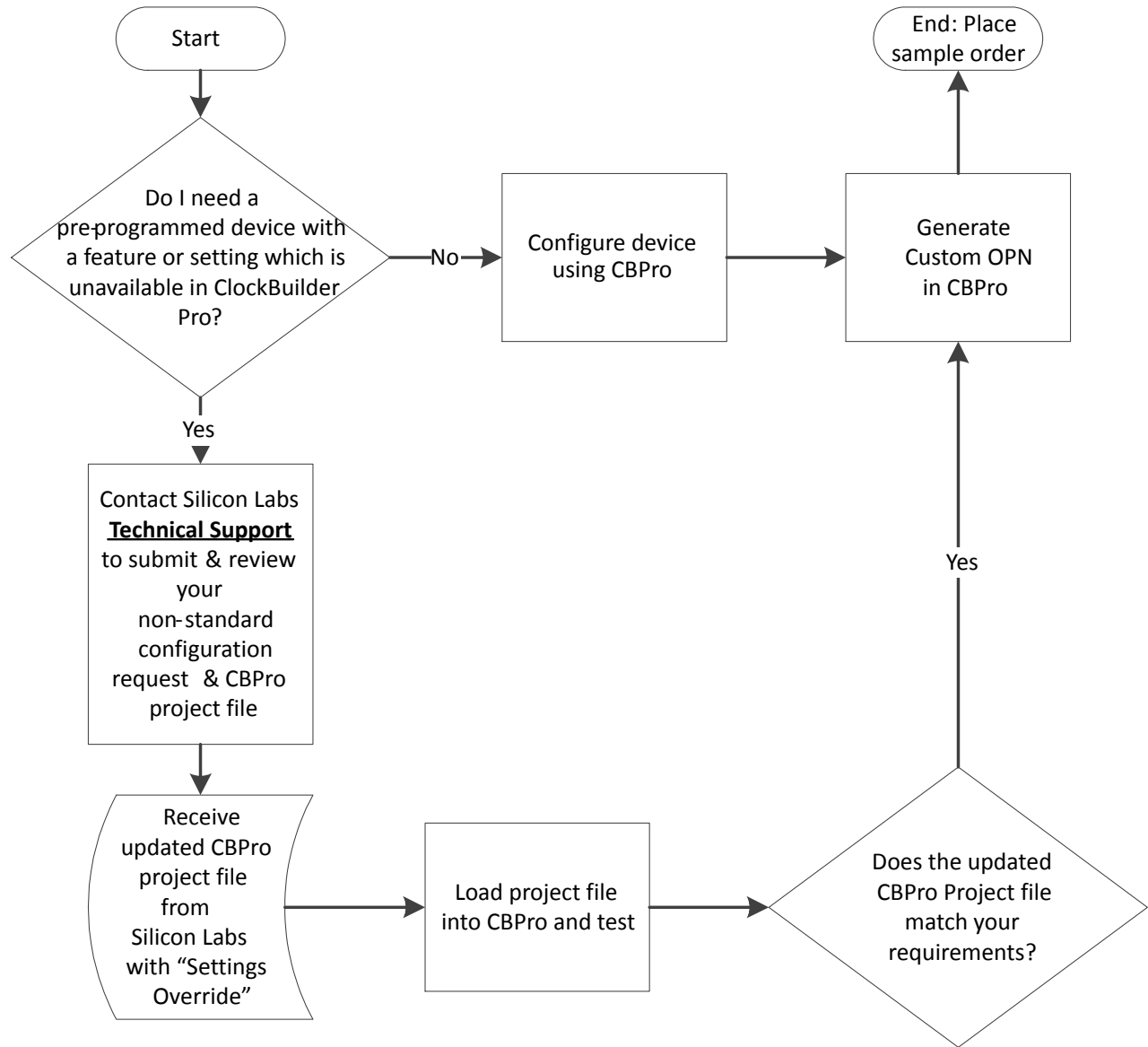
Figure 3.22. Process for Requesting Non-Standard CBPro Features

Note: Contact Silicon Labs Technical Support at www.silabs.com/support/Pages/default.aspx.

4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessed registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration and general device settings. Refer to the Si5348 Reference Manual for a complete list of register descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.