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# Si5367

# µP-Programmable Precision Clock Multiplier

## Features

- Not recommended for new designs. For alternatives, see the Si533x family of products.
- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 10 to 710 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 1.3 MHz)
- Four clock inputs with manual or automatically controlled switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm outputs
- $I^2C$ or SPI programmable settings
- On-chip voltage regulator for 1.8 V ±5%, 2.5 V ±10%, or 3.5 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant


**Ordering Information:**

See page 73.

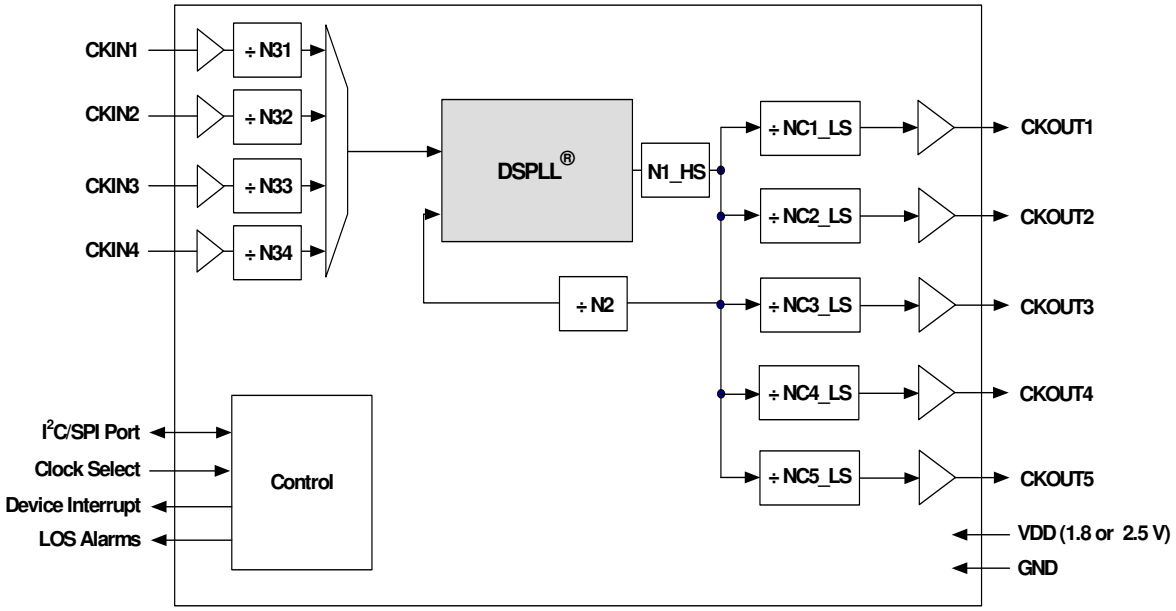
## Applications

- SONET/SDH OC-48/OC-192 STM-16/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Wireless base stations
- Data converter clocking
- xDSL
- SONET/SDH + PDH clock synthesis
- Test and measurement

## Description

The Si5367 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5367 accepts four clock inputs ranging from 10 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. The outputs are divided down separately from a common source. The Si5367 input clock frequency and clock multiplication ratio are programmable through an $I^2C$ or SPI interface. The Si5367 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.5 V supply, the Si5367 is ideal for providing clock multiplication in high performance timing applications.

## Functional Block Diagram



# TABLE OF CONTENTS


| Section | Page |
|---|---|
| **1. Electrical Specifications** | **4** |
| **2. Typical Application Schematics** | **15** |
| **3. Functional Description** | **17** |
| 3.1. Further Documentation | 17 |
| **4. Register Map** | **18** |
| **5. Register Descriptions** | **20** |
| **6. Pin Descriptions: Si5367** | **67** |
| **7. Ordering Guide** | **73** |
| **8. Package Outline: 100-Pin TQFP** | **74** |
| **9. PCB Land Pattern** | **75** |
| **10. Top Marking** | **77** |
| 10.1. Si5367 Top Marking | 77 |
| 10.2. Top Marking Explanation | 77 |
| **Document Change List** | **78** |
| **Contact Information** | **80** |

# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient Temperature | $T_A$ | | –40 | 25 | 85 | C |
| Supply Voltage during Normal Operation | $V_{DD}$ | 3.3 V Nominal | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V Nominal | 2.25 | 2.5 | 2.75 | V |
| | | 1.8 V Nominal | 1.71 | 1.8 | 1.89 | V |
| **Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ºC unless otherwise stated. | | | | | | |

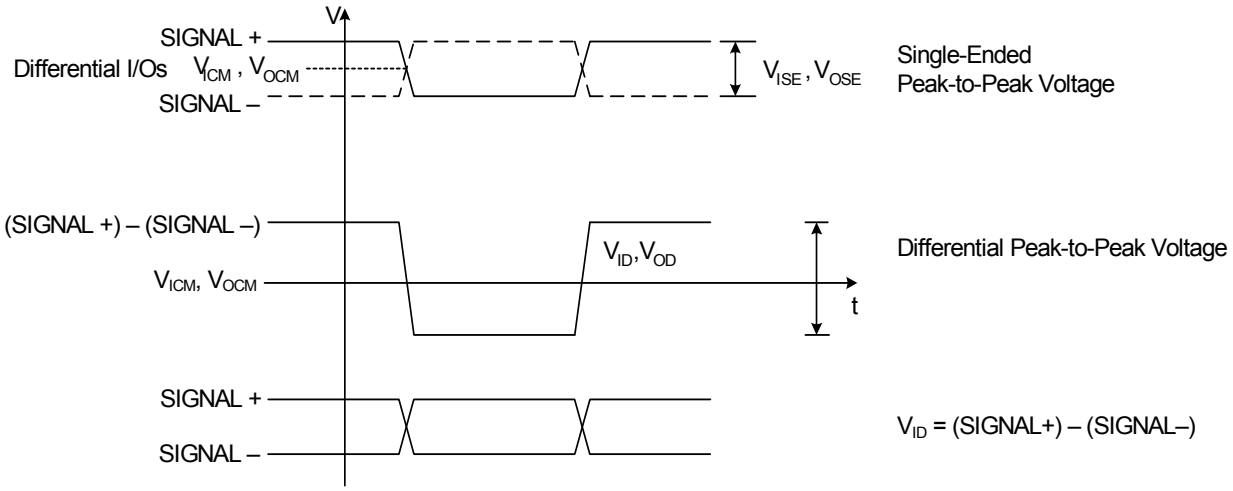



**Figure 1. Differential Voltage Characteristics**

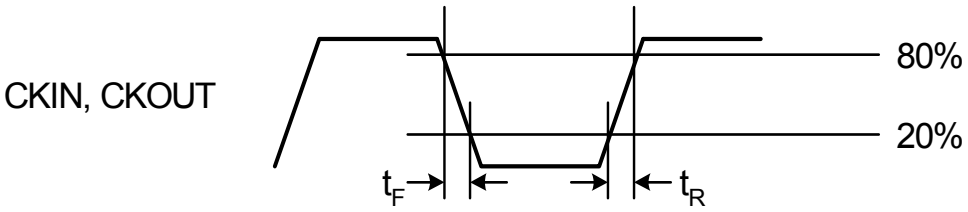



**Figure 2. Rise/Fall Time Characteristics**

## Table 2. DC Characteristics

($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current[1,2] | $I_{DD}$ | LVPECL Format<br>622.08 MHz Out<br>All CKOUTs Enabled | — | 394 | 435 | mA |
| | | LVPECL Format<br>622.08 MHz Out<br>1 CKOUT Enabled | — | 253 | 284 | mA |
| | | CMOS Format<br>19.44 MHz Out<br>All CKOUTs Enabled | — | 278 | 321 | mA |
| | | CMOS Format<br>19.44 MHz Out<br>1 CKOUT Enabled | — | 229 | 261 | mA |
| | | Disable Mode | — | 165 | — | mA |
| **CKINn Input Pins[3]** | | | | | | |
| Input Common Mode Voltage (Input Threshold Voltage) | $V_{ICM}$ | 1.8 V ± 5% | 0.9 | — | 1.4 | V |
| | | 2.5 V ± 10% | 1 | — | 1.7 | V |
| | | 3.3 V ± 10% | 1.1 | — | 1.95 | V |
| Input Resistance | $CKN_{RIN}$ | Single-ended | 20 | 40 | 60 | kΩ |
| Single-Ended Input Voltage Swing (See Absolute Specs) | $V_{ISE}$ | $f_{CKIN}$ < 212.5 MHz<br>See Figure 1. | 0.2 | — | — | $V_{PP}$ |
| | | $f_{CKIN}$ > 212.5 MHz<br>See Figure 1. | 0.25 | — | — | $V_{PP}$ |
| Differential Input Voltage Swing (See Absolute Specs) | $V_{ID}$ | $f_{CKIN}$ < 212.5 MHz<br>See Figure 1. | 0.2 | — | — | $V_{PP}$ |
| | | fCKIN > 212.5 MHz<br>See Figure 1. | 0.25 | — | — | $V_{PP}$ |
| **Output Clocks (CKOUTn)[4,5]** | | | | | | |

**Notes:**

1. Current draw is independent of supply voltage.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.
3. No under- or overshoot is allowed.
4. LVPECL outputs require nominal VDD ≥ 2.5 V.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Common Mode | $CKO_{VCM}$ | LVPECL 100 Ω load line-to-line | $V_{DD}$ –1.42 | — | $V_{DD}$ –1.25 | V |
| Differential Output Swing | $CKO_{VD}$ | LVPECL 100 Ω load line-to-line | 1.1 | — | 1.9 | $V_{PP}$ |
| Single Ended Output Swing | $CKO_{VSE}$ | LVPECL 100 Ω load line-to-line | 0.5 | — | 0.93 | $V_{PP}$ |
| Differential Output Voltage | $CKO_{VD}$ | CML 100 Ω load line-to-line | 350 | 425 | 500 | $mV_{PP}$ |
| Common Mode Output Voltage | $CKO_{VCM}$ | CML 100 Ω load line-to-line | — | $V_{DD}$–0.36 | — | V |
| Differential Output Voltage | $CKO_{VD}$ | LVDS 100 Ω load line-to-line | 500 | 700 | 900 | $mV_{PP}$ |
| | | Low Swing LVDS 100 Ω load line-to-line | 350 | 425 | 500 | $mV_{PP}$ |
| Common Mode Output Voltage | $CKO_{VCM}$ | LVDS 100 Ω load line-to-line | 1.125 | 1.2 | 1.275 | V |
| Differential Output Resistance | $CKO_{RD}$ | CML, LVPECL, LVDS | — | 200 | — | Ω |
| Output Voltage Low | $CKO_{VOLLH}$ | CMOS | — | — | 0.4 | V |
| Output Voltage High | $CKO_{VOHLH}$ | $V_{DD}$ = 1.71 V CMOS | 0.8 x $V_{DD}$ | — | — | V |

**Notes:**
1. Current draw is independent of supply voltage.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.
3. No under- or overshoot is allowed.
4. LVPECL outputs require nominal VDD ≥ 2.5 V.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Drive Current (CMOS driving into $CKO_{VOL}$ for output low or $CKO_{VOH}$ for output high. CKOUT+ and CKOUT– shorted externally) | $CKO_{IO}$ | ICMOS[1:0] = 11<br>$V_{DD}$ = 1.8 V | — | 7.5 | — | mA |
| | | ICMOS[1:0] = 10<br>$V_{DD}$ = 1.8 V | — | 5.5 | — | mA |
| | | ICMOS[1:0] = 01<br>$V_{DD}$ = 1.8 V | — | 3.5 | — | mA |
| | | ICMOS[1:0] = 00<br>$V_{DD}$ = 1.8 V | — | 1.75 | — | mA |
| | | ICMOS[1:0] = 11<br>$V_{DD}$ = 3.3 V | — | 32 | — | mA |
| | | ICMOS[1:0] = 10<br>$V_{DD}$ = 3.3 V | — | 24 | — | mA |
| | | ICMOS[1:0] = 01<br>$V_{DD}$ = 3.3 V | — | 16 | — | mA |
| | | ICMOS[1:0] = 00<br>$V_{DD}$ = 3.3 V | — | 8 | — | mA |
| **2-Level LVCMOS Input Pins** | | | | | | |
| Input Voltage Low | $V_{IL}$ | $V_{DD}$ = 1.71 V | — | — | 0.5 | V |
| | | $V_{DD}$ = 2.25 V | — | — | 0.7 | V |
| | | $V_{DD}$ = 2.97 V | — | — | 0.8 | V |
| Input Voltage High | $V_{IH}$ | $V_{DD}$ = 1.89 V | 1.4 | — | — | V |
| | | $V_{DD}$ = 2.25 V | 1.8 | — | — | V |
| | | $V_{DD}$ = 3.63 V | 2.5 | — | — | V |

**Notes:**
1. Current draw is independent of supply voltage.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.
3. No under- or overshoot is allowed.
4. LVPECL outputs require nominal VDD ≥ 2.5 V.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **3-Level Input Pins[6]** | | | | | | |
| Input Voltage Low | $V_{ILL}$ | | — | — | 0.15 x $V_{DD}$ | V |
| Input Voltage Mid | $V_{IMM}$ | | 0.45 x $V_{DD}$ | — | 0.55 x $V_{DD}$ | V |
| Input Voltage High | $V_{IHH}$ | | 0.85 x $V_{DD}$ | — | — | V |
| Input Low Current | $I_{ILL}$ | See Note 6 | –20 | — | — | µA |
| Input Mid Current | $I_{IMM}$ | See Note 6 | –2 | — | +2 | µA |
| Input High Current | $I_{IHH}$ | See Note 6 | — | — | 20 | µA |
| **LVCMOS Output Pins** | | | | | | |
| Output Voltage Low | $V_{OL}$ | IO = 2 mA<br>$V_{DD}$ = 1.71 V | — | — | 0.4 | V |
| Output Voltage Low | | IO = 2 mA<br>$V_{DD}$ = 2.97 V | — | — | 0.4 | V |
| Output Voltage High | $V_{OH}$ | IO = –2 mA<br>$V_{DD}$ = 1.71 V | $V_{DD}$ – 0.4 | — | — | V |
| Output Voltage High | | IO = –2 mA<br>$V_{DD}$ = 2.97 V | $V_{DD}$ – 0.4 | — | — | V |
| Disabled Leakage Current | $I_{OZ}$ | RSTb = 0 | –100 | — | 100 | µA |

**Notes:**
1. Current draw is independent of supply voltage.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.
3. No under- or overshoot is allowed.
4. LVPECL outputs require nominal VDD ≥ 2.5 V.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.

**Table 3. AC Characteristics**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CKINn Input Pins** | | | | | | |
| Input Frequency | $CKN_F$ | | 10 | — | 710 | MHz |
| Input Duty Cycle (Minimum Pulse Width) | $CKN_{DC}$ | Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks) | 40 | — | 60 | % |
| | | | 2 | — | — | ns |
| Input Capacitance | $CKN_{CIN}$ | | — | — | 3 | pF |
| Input Rise/Fall Time | $CKN_{TRF}$ | 20–80%<br>See Figure 2 | — | — | 11 | ns |
| **CKOUTn Output Pins**<br>(See ordering section for speed grade vs frequency limits) | | | | | | |
| Output Frequency (Output not configured for CMOS or Disabled) | $CKO_F$ | N1 ≥ 6 | 0.002 | — | 945 | MHz |
| | | N1 = 5 | 970 | — | 1134 | MHz |
| | | N1 = 4 | 1.213 | — | 1.4 | GHz |
| Maximum Output Frequency in CMOS Format | $CKO_F$ | | — | — | 212.5 | MHz |
| Output Rise/Fall (20–80 %) @ 622.08 MHz output | $CKO_{TRF}$ | Output not configured for CMOS or Disabled<br>See Figure 2 | — | 230 | 350 | ps |
| Output Rise/Fall (20–80%) @ 212.5 MHz output | $CKO_{TRF}$ | CMOS Output<br>$V_{DD}$ = 1.71<br>$C_{LOAD}$ = 5 pF | — | — | 8 | ns |
| Output Rise/Fall (20–80%) @ 212.5 MHz output | $CKO_{TRF}$ | CMOS Output<br>$V_{DD}$ = 2.97<br>$C_{LOAD}$ = 5 pF | — | — | 2 | ns |
| Output Duty Cycle Uncertainty @ 622.08 MHz | $CKO_{DC}$ | 100 Ω Load<br>Line-to-Line<br>Measured at 50% Point<br>(Not for CMOS) | — | — | +/-40 | ps |

**Table 3. AC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LVCMOS Input Pins** | | | | | | |
| Minimum Reset Pulse Width | $t_{RSTMN}$ | | 1 | — | — | µs |
| Reset to Microprocessor Access Ready | $t_{READY}$ | | — | — | 10 | ms |
| Input Capacitance | $C_{in}$ | | — | — | 3 | pF |
| **LVCMOS Output Pins** | | | | | | |
| Rise/Fall Times | $t_{RF}$ | $C_{LOAD}$ = 20 pF<br>See Figure 2 | — | 25 | — | ns |
| LOSn Trigger Window | $LOS_{TRIG}$ | From last CKINn ↑ to ↓ Internal detection of LOSn<br>N3 ≠ 1 | — | — | 4.5 x N3 | $T_{CKIN}$ |
| Time to Clear LOL after LOS Cleared | $t_{CLRLOL}$ | ↓LOS to ↓LOL<br>Fold = Fnew<br>Stable Xa/XB reference | — | 10 | — | ms |
| **Device Skew** | | | | | | |
| Output Clock Skew | $t_{SKEW}$ | ↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format<br>PHASEOFFSET = 0<br>CKOUT_ALWAYS_ON = 1<br>SQ_ICAL = 1 | — | — | 100 | ps |
| Phase Change due to Temperature Variation | $t_{TEMP}$ | Max phase changes from –40 to +85 °C | — | 300 | 500 | ps |

**Table 3. AC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PLL Performance (fin = fout = 622.08 MHz; BW = 120 Hz; LVPECL)** | | | | | | |
| Lock Time | $t_{LOCKMP}$ | Start of ICAL to ↓ of LOL | — | 35 | 1200 | ms |
| Closed Loop Jitter Peaking | $J_{PK}$ | | — | 0.05 | 0.1 | dB |
| Jitter Tolerance | $J_{TOL}$ | Jitter Frequency ≥ Loop Bandwidth | 5000/BW | — | — | ns pk-pk |
| Phase Noise fout = 622.08 MHz | $CKO_{PN}$ | 1 kHz Offset | — | –90 | — | dBc/Hz |
| | | 10 kHz Offset | — | –113 | — | dBc/Hz |
| | | 100 kHz Offset | — | –118 | — | dBc/Hz |
| | | 1 MHz Offset | — | –132 | — | dBc/Hz |
| Subharmonic Noise | $SP_{SUBH}$ | Phase Noise @ 100 kHz Offset | — | –88 | — | dBc |
| Spurious Noise | $SP_{SPUR}$ | Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz) | — | –93 | — | dBc |

**Table 4. Microprocessor Control**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$I^2C$ Bus Lines (SDA, SCL)** | | | | | | |
| Input Voltage Low | $VIL_{I2C}$ | | — | — | 0.25 x $V_{DD}$ | V |
| Input Voltage High | $VIH_{I2C}$ | | 0.7 x $V_{DD}$ | — | $V_{DD}$ | V |
| Hysteresis of Schmitt trigger inputs | $VHYS_{I2C}$ | $V_{DD}$ = 1.8V | 0.1 x $V_{DD}$ | — | — | V |
| | | $V_{DD}$ = 2.5 or 3.3 V | 0.05 x $V_{DD}$ | — | — | V |
| Output Voltage Low | $VOL_{I2C}$ | $V_{DD}$ = 1.8 V IO = 3 mA | — | — | 0.2 x $V_{DD}$ | V |
| | | $V_{DD}$ = 2.5 or 3.3 V IO = 3 mA | — | — | 0.4 | V |

**Table 4. Microprocessor Control (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SPI Specifications** | | | | | | |
| Duty Cycle, SCLK | $t_{DC}$ | SCLK = 10 MHz | 40 | — | 60 | % |
| Cycle Time, SCLK | $t_c$ | | 100 | — | — | ns |
| Rise Time, SCLK | $t_r$ | 20–80% | — | — | 25 | ns |
| Fall Time, SCLK | $t_f$ | 20–80% | — | — | 25 | ns |
| Low Time, SCLK | $t_{lsc}$ | 20–20% | 30 | — | — | ns |
| High Time, SCLK | $t_{hsc}$ | 80–80% | 30 | — | — | ns |
| Delay Time, SCLK Fall to SDO Active | $t_{d1}$ | | — | — | 25 | ns |
| Delay Time, SCLK Fall to SDO Transition | $t_{d2}$ | | — | — | 25 | ns |
| Delay Time, SS Rise to SDO Tri-state | $t_{d3}$ | | — | — | 25 | ns |
| Setup Time, SS to SCLK Fall | $t_{su1}$ | | 25 | — | — | ns |
| Hold Time, SS to SCLK Rise | $t_{h1}$ | | 20 | — | — | ns |
| Setup Time, SDI to SCLK Rise | $t_{su2}$ | | 25 | — | — | ns |
| Hold Time, SDI to SCLK Rise | $t_{h2}$ | | 20 | — | — | ns |
| Delay Time between Slave Selects | $t_{cs}$ | | 25 | — | — | ns |

### Table 5. Jitter Generation

| Parameter | Symbol | Test Condition* / Measurement Filter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Jitter Gen OC-192 | JGEN | 4–80 MHz | — | .23 | — | $ps_{rms}$ |
| | | 0.05–80 MHz | — | .47 | — | ps rms |
| Jitter Gen OC-48 | JGEN | 0.12–20 MHz | — | .48 | — | ps rms |

***Note:** Test conditions:

1. fIN = fOUT = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 877 kHz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. $V_{DD}$ = 2.5 V
7. $T_A$ = 85 °C

### Table 6. Thermal Characteristics

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still Air | 40 | C°/W |

### Table 7. Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | –0.5 to 3.8 | V |
| LVCMOS Input Voltage | $V_{DIG}$ | –0.3 to ($V_{DD}$ + 0.3) | V |
| CKINn Voltage Level Limits | $CKN_{VIN}$ | 0 to $V_{DD}$ | V |
| XA/XB Voltage Level Limits | $XA_{VIN}$ | 0 to 1.2 | V |
| Operating Junction Temperature | $T_{JCT}$ | –55 to 150 | C |
| Storage Temperature Range | $T_{STG}$ | –55 to 150 | C |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN– | | 2 | kV |
| ESD MM Tolerance; All pins except CKIN+/CKIN– | | 700 | V |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN– | | 750 | V |
| ESD MM Tolerance; CKIN+/CKIN– | | 100 | V |
| Latch-Up Tolerance | | JESD78 Compliant | |

**Note:** Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

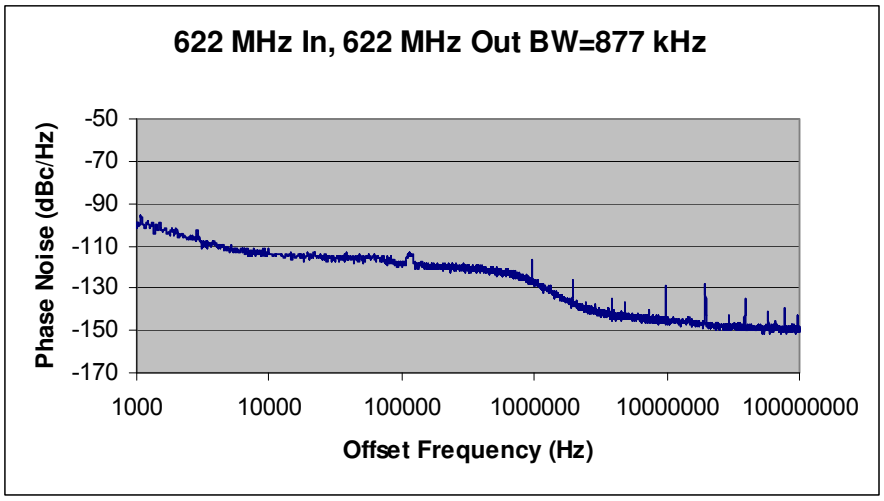
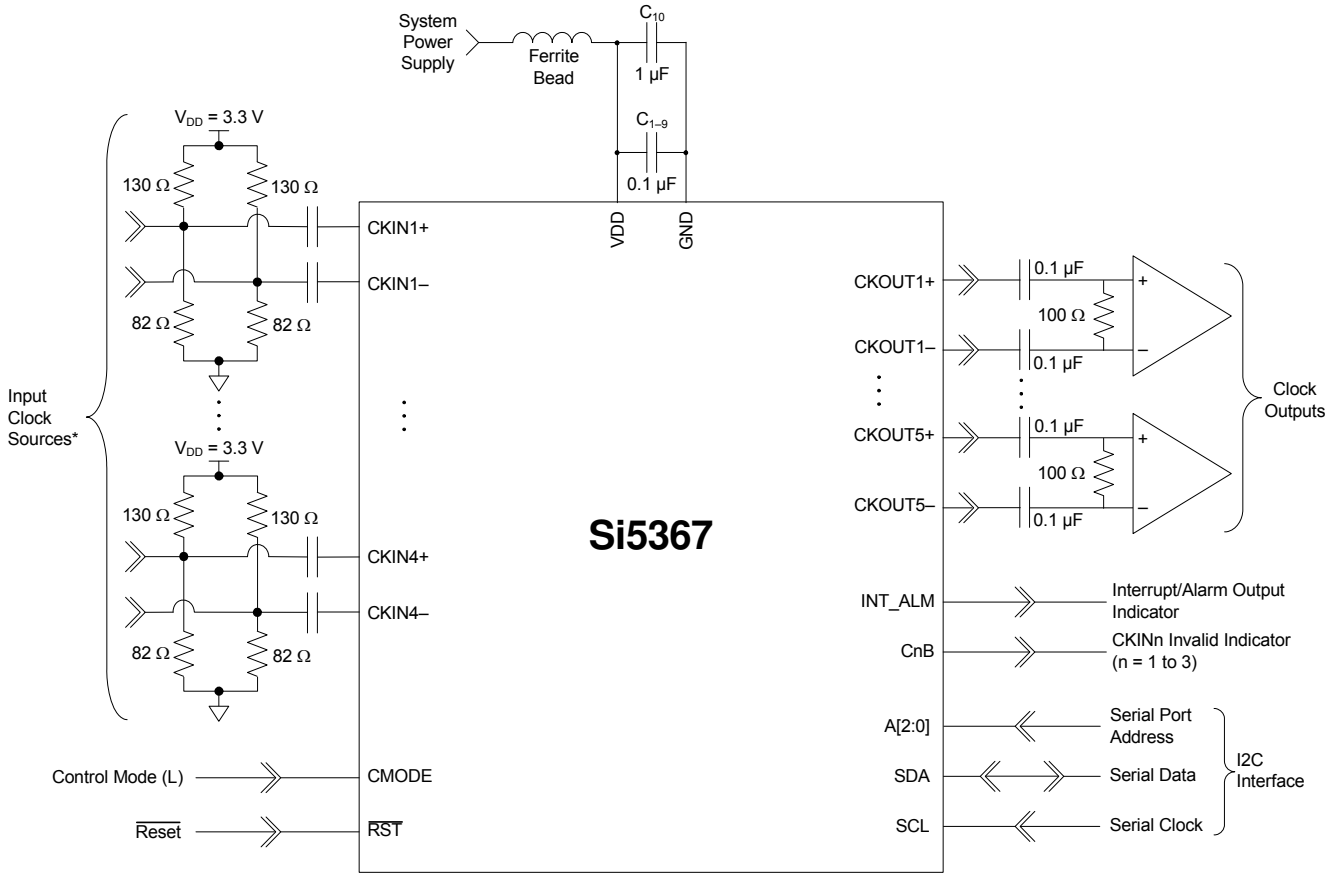



**Figure 3. Typical Phase Noise Plot**

### Table 8. Typical RMS Jitter Values

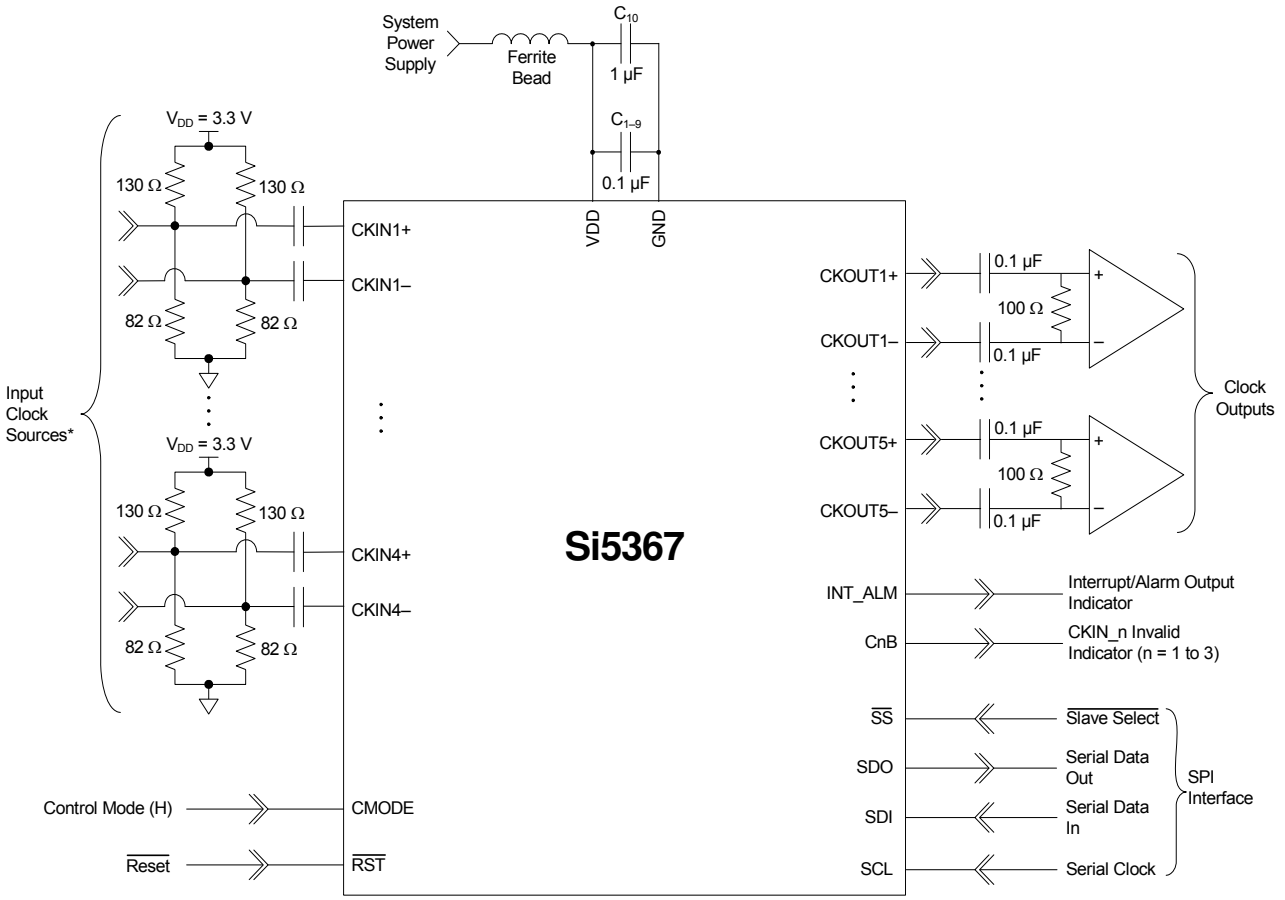
| Jitter Bandwidth | RMS Jitter (fs) |
|---|---|
| OC-48, 12 kHz to 20 MHz | 374 |
| OC-192, 20 kHz to 80 MHz | 388 |
| OC-192, 4 MHz to 80 MHz | 181 |
| OC-192, 50 kHz to 80 MHz | 377 |
| Broadband, 800 Hz to 80 MHz | 420 |

## 2. Typical Application Schematics




***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

**Figure 4. Si5367 Typical Application Circuit ($I^2C$ Control Mode)**




***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

**Figure 5. Si5367 Typical Application Circuit (SPI Control Mode)**

# 3. Functional Description

The Si5367 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5367 accepts four clock inputs ranging from 10 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for every input clock and output clock, so the Si5367 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5367 input clock frequency and clock multiplication ratio are programmable through an $I^2C$ or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5367 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5367 PLL loop bandwidth is digitally programmable and supports a range from 150 kHz to 1.3 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5367 monitors all input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on its inputs.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5367 has five differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. In addition, the phase of each output clock may be adjusted in relation to the other output clocks. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the DSPLL*sim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8 or 2.5 V supply.

## 3.1. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5367. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

## 4. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | | | CKOUT_ALWAYS_ON | | | | BYPASS_REG | |
| 1 | CK_PRIOR4 [1:0] | | CK_PRIOR3 [1:0] | | CK_PRIOR2 [1:0] | | CK_PRIOR1 [1:0] | |
| 2 | BWSEL_REG [3:0] | | | | | | | |
| 3 | CKSEL_REG [1:0] | | | SQ_ICAL | | | | |
| 4 | AUTOSEL_REG [1:0] | | | | | | | |
| 5 | ICMOS [1:0] | | SFOUT2_REG [2:0] | | | SFOUT1_REG [2:0] | | |
| 6 | | | SFOUT4_REG [2:0] | | | SFOUT3_REG [2:0] | | |
| 7 | | | SFOUT5_REG [2:0] | | | FOSREFSEL [2:0] | | |
| 8 | HLOG_4 [1:0] | | HLOG_3 [1:0] | | HLOG_2 [1:0] | | HLOG_1 [1:0] | |
| 9 | | | | | | | HLOG_5 [1:0] | |
| 10 | | | DSBL5_REG | | DSBL4_REG | DSBL3_REG | DSBL2_REG | DSBL1_REG |
| 11 | | | | | PD_CK4 | PD_CK3 | PD_CK2 | PD_CK1 |
| 19 | FOS_EN | FOS_THR [1:0] | | VALTIME [1:0] | | | | |
| 20 | | | | CK3_BAD_PIN | CK2_BAD_PIN | CK1_BAD_PIN | | INT_PIN |
| 21 | | | | CK4_ACTV_PIN | CK3_ACTV_PIN | CK2_ACTV_PIN | CK1_ACTV_PIN | CKSEL_PIN |
| 22 | | | | | CK_ACTV_POL | CK_BAD_POL | | INT_POL |
| 23 | | | | LOS4_MSK | LOS3_MSK | LOS2_MSK | LOS1_MSK | |
| 24 | | | | FOS4_MSK | FOS3_MSK | FOS2_MSK | FOS1_MSK | |
| 25 | N1_HS [2:0] | | | | NC1_LS [19:16] | | | |
| 26 | NC1_LS [15:8] | | | | | | | |
| 27 | NC1_LS [7:0] | | | | | | | |
| 28 | | | | | NC2_LS [19:16] | | | |
| 29 | NC2_LS [15:8] | | | | | | | |
| 30 | NC2_LS [7:0] | | | | | | | |
| 31 | | | | | NC3_LS [19:16] | | | |
| 32 | NC3_LS [15:8] | | | | | | | |
| 33 | NC3_LS [7:0] | | | | | | | |
| 34 | | | | | NC4_LS [19:16] | | | |
| 35 | NC4_LS [15:8] | | | | | | | |
| 36 | NC4_LS [7:0] | | | | | | | |
| 37 | | | | | NC5_LS [19:16] | | | |
| 38 | NC5_LS [15:8] | | | | | | | |

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 39 | NC5_LS [7:0] | | | | | | | |
| 40 | | | | | N2_LS [19:16] | | | |
| 41 | N2_LS [15:8] | | | | | | | |
| 42 | N2_LS [7:0] | | | | | | | |
| 43 | | | | | | N31_ [18:16] | | |
| 44 | N31_[15:8] | | | | | | | |
| 45 | N31_ [7:0] | | | | | | | |
| 46 | | | | | | N32_ [18:16] | | |
| 47 | N31_ [15:8] | | | | | | | |
| 48 | N32_[7:0] | | | | | | | |
| 49 | | | | | | N33_[18:16] | | |
| 50 | N33_[15:8] | | | | | | | |
| 51 | N33_[7:0] | | | | | | | |
| 52 | | | | | | N34_[18:16] | | |
| 53 | N34_[15:8] | | | | | | | |
| 54 | N34_[7:0] | | | | | | | |
| 55 | | | CLKIN2RATE_[2:0] | | | CLKIN1RATE[2:0] | | |
| 56 | | | CLKIN4RATE_[2:0] | | | CLKIN3RATE[2:0] | | |
| 128 | | | | | CK4_ACTV_REG | CK3_ACTV_REG | CK2_ACTV_REG | CK1_ACTV_REG |
| 129 | | | | LOS4_INT | LOS3_INT | LOS2_INT | LOS1_INT | |
| 130 | | | | FOS4_INT | FOS3_INT | FOS2_INT | FOS1_INT | |
| 131 | | | | LOS4_FLG | LOS3_FLG | LOS2_FLG | LOS1_FLG | |
| 132 | | | FOS4_FLG | FOS3_FLG | FOS2_FLG | FOS1_FLG | | |
| 134 | PARTNUM_RO [11:4] | | | | | | | |
| 135 | PARTNUM_RO [3:0] | | | | REVID_RO [3:0] | | | |
| 136 | RST_REG | ICAL | | | | | | |
| 138 | | | | | LOS4_EN [1:1] | LOS3_EN [1:1] | LOS2_EN [1:1] | LOS1_EN [1:1] |
| 139 | LOS4_EN [0:0] | LOS3_EN [0:0] | LOS2_EN [0:0] | LOS1_EN [0:0] | FOS4_EN | FOS3_EN | FOS2_EN | FOS1_EN |
| 140 | INDEPENDENTSKEW1 [7:0] | | | | | | | |
| 141 | INDEPENDENTSKEW2 [7:0] | | | | | | | |
| 142 | INDEPENDENTSKEW3 [7:0] | | | | | | | |
| 143 | INDEPENDENTSKEW4 [7:0] | | | | | | | |
| 144 | INDEPENDENTSKEW5 [7:0] | | | | | | | |

# 5. Register Descriptions

**Register 0.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | CKOUT_ALWAYS_ON | | | | BYPASS_REG | |
| Type | R | R | R/W | R | R | R | R/W | R |

Reset value = 0001 0100

| Bit | Name | Function |
|---|---|---|
| 7:6 | Reserved | |
| 5 | CKOUT_ALWAYS_ON | **CKOUT Always On.**<br>This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9.<br>0: Squelch output until part is calibrated (ICAL).<br>1: Provide an output. Note: The frequency may be significantly off until the part is calibrated. |
| 4:2 | Reserved | |
| 1 | BYPASS_REG | **Bypass Register.**<br>This bit enables or disables the PLL bypass mode. Use is only valid when the part is in digital hold or before the first ICAL.<br>0: Normal operation<br>1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL. Bypass mode does not support CMOS clock outputs. |
| 0 | Reserved | |

**Register 1.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | CK_PRIOR4 [1:0] | | CK_PRIOR3 [1:0] | | CK_PRIOR2 [1:0] | | CK_PRIOR1 [1:0] | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value = 1110 0100

| Bit | Name | Function |
|---|---|---|
| 7:6 | CK_PRIOR4 [1:0] | Selects which of the input clocks will be 4th priority in the autoselection state machine.<br>00: CKIN1 is 4th priority<br>01: CKIN2 is 4th priority<br>10: CKIN3 is 4th priority<br>11: CKIN4 is 4th priority |
| 5:4 | CK_PRIOR3 [1:0] | Selects which of the input clocks will be 3rd priority in the autoselection state machine.<br>00: CKIN1 is 3rd priority<br>01: CKIN2 is 3rd priority<br>10: CKIN3 is 3rd priority<br>11: CKIN4 is 3rd priority |
| 3:2 | CK_PRIOR2 [1:0] | **CK_PRIOR 2.**<br>Selects which of the input clocks will be 2nd priority in the autoselection state machine.<br>00: CKIN1 is 2nd priority<br>01: CKIN2 is 2nd priority<br>10: CKIN3 is 2nd priority<br>11: CKIN4 is 2nd priority |
| 1:0 | CK_PRIOR1 [1:0] | **CK_PRIOR 1.**<br>Selects which of the input clocks will be 1st priority in the autoselection state machine.<br>00: CKIN1 is 1st priority<br>01: CKIN2 is 1st priority<br>10: CKIN3 is 1st priority<br>11: CKIN4 is 1st priority |

**Register 2.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | BWSEL_REG [3:0] | | | | | | | |
| Type | R/W | | | | R | R | R | R |

Reset value = 0100 0010

| Bit | Name | Function |
|---|---|---|
| 7:4 | BWSEL_REG [3:0] | **BWSEL_REG.**<br>Selects nominal f3dB bandwidth for PLL. See the DSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect. |
| 3:0 | Reserved | |

**Register 3.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | CKSEL_REG [1:0] | | | SQ_ICAL | | | | |
| Type | R/W | | R | R/W | R | R | R | R |

Reset value = 0000 0101

| Bit | Name | Function |
|---|---|---|
| 7:6 | CKSEL_REG [1:0] | **CKSEL_REG.**<br>If the device is operating in manual register-based clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1, the CKSEL[1:0] input pins continue to control clock selection and CKSEL_REG is of no consequence.<br>00: CKIN_1 selected.<br>01: CKIN_2 selected.<br>10: CKIN_3 selected.<br>11: CKIN_4 selected. |
| 5 | Reserved | |
| 4 | SQ_ICAL | **SQ_ICAL.**<br>This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9.<br>0: Output clocks enabled during ICAL.<br>1: Output clocks disabled during ICAL. |
| 3:0 | Reserved | |

**Register 4.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | AUTOSEL_REG [1:0] | | | | | | | |
| Type | R/W | | R | R | R | R | R | R |

Reset value = 0001 0010

| Bit | Name | Function |
|---|---|---|
| 7:6 | AUTOSEL_REG [1:0] | **AUTOSEL_REG [1:0].**<br>Selects method of input clock selection to be used.<br>00: Manual (either register or pin controlled. See CKSEL_PIN).<br>01: Automatic Non-Revertive<br>10: Automatic Revertive<br>11: Reserved |
| 5:0 | Reserved | |

**Register 5.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | ICMOS [1:0] | | SFOUT2_REG [2:0] | | | SFOUT1_REG [2:0] | | |
| Type | R/W | | R/W | | | R/W | | |

Reset value = 1110 1101

| Bit | Name | Function |
|---|---|---|
| 7:6 | ICMOS [1:0] | **ICMOS [1:0].**<br>When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT–.<br>00: 8 mA/2 mA<br>01: 16 mA/4 mA<br>10: 24 mA/6 mA<br>11: 32 mA (3.3 V operation)/8 mA (1.8 V operation) |
| 5:3 | SFOUT2_REG [2:0] | **SFOUT2_REG [2:0].**<br>Controls output signal format and disable for CKOUT2 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.<br>000: Reserved<br>001: Disable<br>010: CMOS (Bypass mode not supported.)<br>011: Low swing LVDS<br>100: Reserved<br>101: LVPECL<br>110: CML<br>111: LVDS |
| 2:0 | SFOUT1_REG [2:0] | **SFOUT1_REG [2:0].**<br>Controls output signal format and disable for CKOUT1 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.<br>000: Reserved<br>001: Disable<br>010: CMOS (Bypass mode not supported.)<br>011: Low swing LVDS<br>100: Reserved<br>101: LVPECL<br>110: CML<br>111: LVDS |

**Register 6.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | SFOUT4_REG [2:0] | | | SFOUT3_REG [2:0] | | |
| Type | R | R | R/W | | | R/W | | |

Reset value = 0010 1100

| Bit | Name | Function |
|---|---|---|
| 7:6 | Reserved | |
| 5:3 | SFOUT4_REG [2:0] | **SFOUT4_REG [2:0].**<br>Controls output signal format and disable for CKOUT4 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.<br><br>000: Reserved<br>001: Disable<br>010: CMOS (Bypass mode not supported.)<br>011: Low swing LVDS<br>100: Reserved<br>101: LVPECL<br>110: CML<br>111: LVDS |
| 2:0 | SFOUT3_REG [2:0] | **SFOUT3_REG [2:0].**<br>Controls output signal format and disable for CKOUT3 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.<br><br>000: Reserved<br>001: Disable<br>010: CMOS (Bypass mode not supported.)<br>011: Low swing LVDS<br>100: Reserved<br>101: LVPECL<br>110: CML<br>111: LVDS |