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# ANY-FREQUENCY PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

## Features

- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 300 fs rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (4 Hz to 525 Hz)
- Meets OC-192 GR-253-CORE jitter specifications
- Four clock inputs with manual or automatically controlled hitless switching and phase build-out
- Supports holdover and freerun modes of operation
- SONET frame sync switching and regeneration
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (253/226, 239/237, 255/238, 255/237, 255/236)
- LOL, LOS, FOS alarm outputs
- Digitally-controlled output phase adjust
- $I^2C$ or SPI programmable settings
- On-chip voltage regulator for 1.8 V ±5%, 2.5 V ±10%, or 3.3 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant


**Ordering Information:**
See page 78.

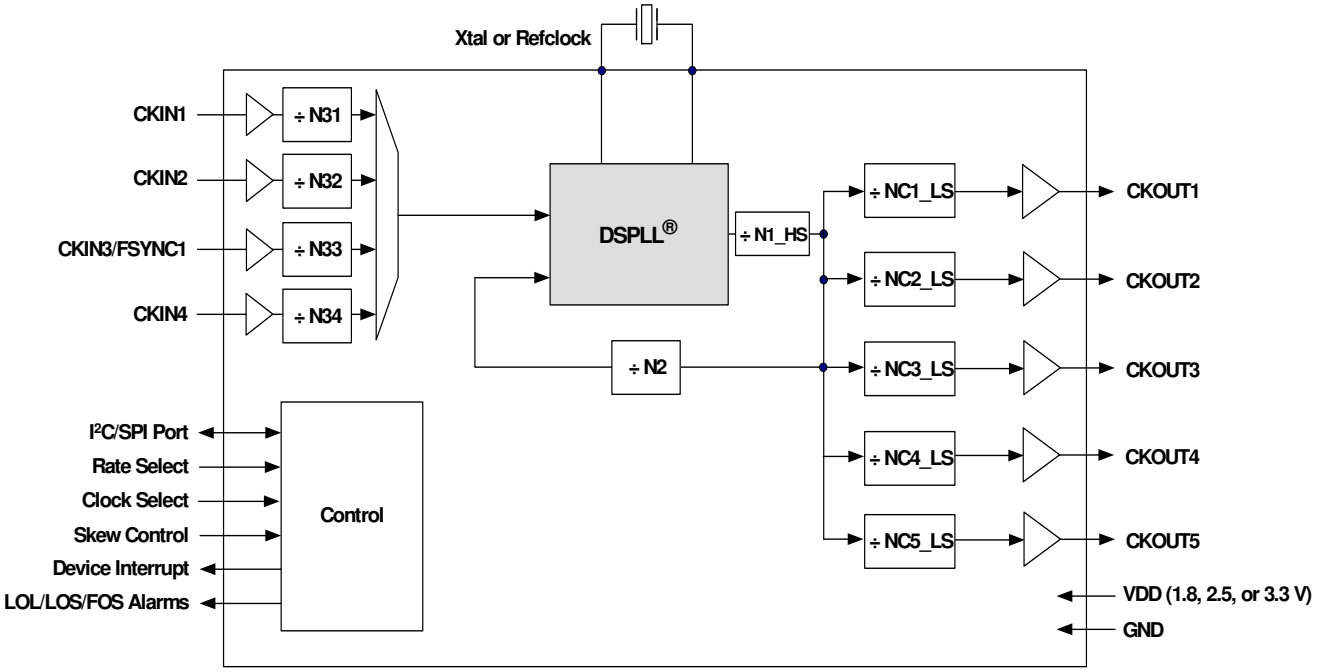
## Applications

- SONET/SDH OC-48/STM-16/OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10G FC line cards
- ITU G.709 and custom FEC line cards
- Wireless repeaters/wireless backhaul
- Data converter clocking
- OTN/WDM Muxponder, MSPP, ROADM line cards
- SONET/SDH + PDH clock synthesis
- Test and measurement
- Synchronous Ethernet
- Broadcast video

## Description

The Si5369 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps rms jitter performance. The Si5369 accepts four clock inputs ranging from 2 kHz to 710 MHz and generates five clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. The outputs are divided down separately from a common source. The Si5369 input clock frequency and clock multiplication ratio are programmable through an $I^2C$ or SPI interface. The Si5369 is based on Silicon Laboratories' third-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5 ,or 3.3 V supply, the Si5369 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

## Functional Block Diagram



# TABLE OF CONTENTS

# 1. Electrical Specifications

**Table 1. Recommended Operating Conditions[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient Temperature | $T_A$ | | -40 | 25 | 85 | C |
| Supply Voltage during Normal Operation | $V_{DD}$ | 3.3 V Nominal[2] | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V Nominal | 2.25 | 2.5 | 2.75 | V |
| | | 1.8 V Nominal | 1.71 | 1.8 | 1.89 | V |

**Notes:**
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ºC unless otherwise stated.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

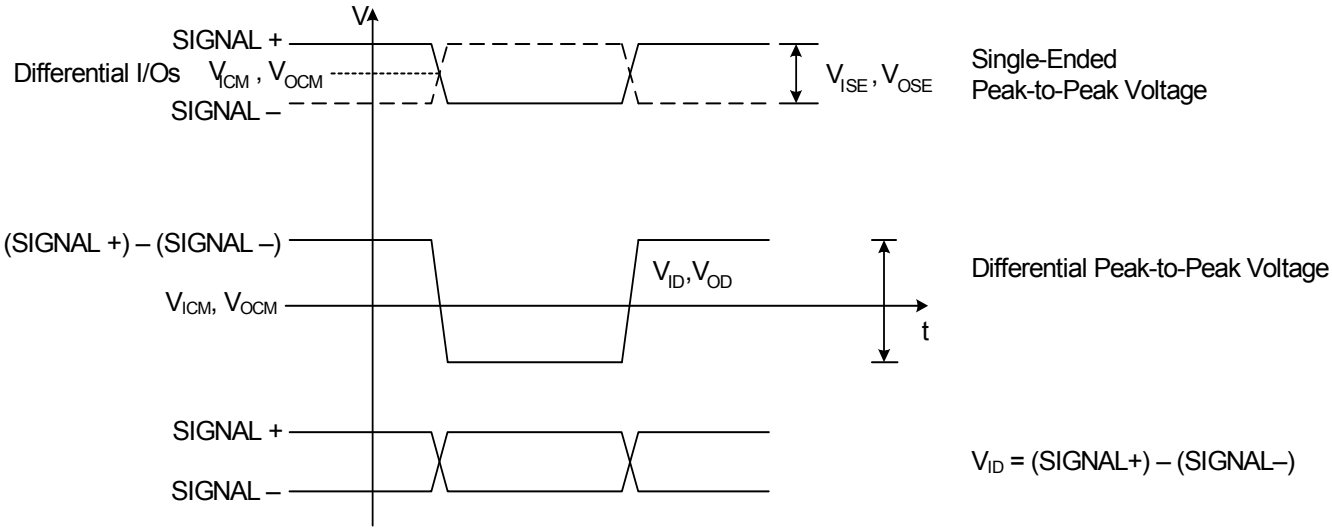



**Figure 1. Differential Voltage Characteristics**

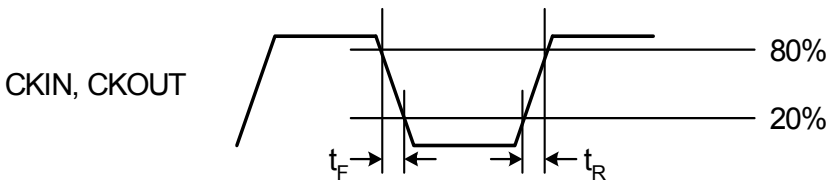



**Figure 2. Rise/Fall Time Characteristics**

## Table 2. DC Characteristics

($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current[1,6] | $I_{DD}$ | LVPECL Format<br>622.08 MHz Out<br>All CKOUTs Enabled | — | 394 | 435 | mA |
| | | LVPECL Format<br>622.08 MHz Out<br>1 CKOUT Enabled | — | 253 | 284 | mA |
| | | CMOS Format<br>19.44 MHz Out<br>All CKOUTs Enabled | — | 278 | 400 | mA |
| | | CMOS Format<br>19.44 MHz Out<br>1 CKOUT Enabled | — | 229 | 261 | mA |
| | | Disable Mode | — | 165 | — | mA |
| **CKINn Input Pins[2]** | | | | | | |
| Input Common Mode Voltage (Input Threshold Voltage) | $V_{ICM}$ | 1.8 V ± 5% | 0.9 | — | 1.4 | V |
| | | 2.5 V ± 10% | 1 | — | 1.7 | V |
| | | 3.3 V ± 10% | 1.1 | — | 1.95 | V |
| Input Resistance | $CKN_{RIN}$ | Single-ended | 20 | 40 | 60 | kΩ |
| Single-Ended Input Voltage Swing (See Absolute Specs) | $V_{ISE}$ | $f_{CKIN}$ < 212.5 MHz<br>See Figure 1. | 0.2 | — | — | $V_{PP}$ |
| | | $f_{CKIN}$ > 212.5 MHz<br>See Figure 1. | 0.25 | — | — | $V_{PP}$ |
| Differential Input Voltage Swing (See Absolute Specs) | $V_{ID}$ | $f_{CKIN}$ < 212.5 MHz<br>See Figure 1. | 0.2 | — | — | $V_{PP}$ |
| | | fCKIN > 212.5 MHz<br>See Figure 1. | 0.25 | — | — | $V_{PP}$ |

**Notes:**

1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Output Clocks (CKOUTn)[3,5,6]** | | | | | | |
| Common Mode | $CKO_{VCM}$ | LVPECL 100 Ω load line-to-line | $V_{DD}$ –1.42 | — | $V_{DD}$ –1.25 | V |
| Differential Output Swing | $CKO_{VD}$ | LVPECL 100 Ω load line-to-line | 1.1 | — | 1.9 | $V_{PP}$ |
| Single Ended Output Swing | $CKO_{VSE}$ | LVPECL 100 Ω load line-to-line | 0.5 | — | 0.93 | $V_{PP}$ |
| Differential Output Voltage | $CKO_{VD}$ | CML 100 Ω load line-to-line | 350 | 425 | 500 | $mV_{PP}$ |
| Common Mode Output Voltage | $CKO_{VCM}$ | CML 100 Ω load line-to-line | — | $V_{DD}$–0.36 | — | V |
| Differential Output Voltage | $CKO_{VD}$ | LVDS 100 Ω load line-to-line | 500 | 700 | 900 | $mV_{PP}$ |
| | | Low Swing LVDS 100 Ω load line-to-line | 350 | 425 | 500 | $mV_{PP}$ |
| Common Mode Output Voltage | $CKO_{VCM}$ | LVDS 100 Ω load line-to-line | 1.125 | 1.2 | 1.275 | V |
| Differential Output Resistance | $CKO_{RD}$ | CML, LVPECL, LVDS | — | 200 | — | Ω |
| Output Voltage Low | $CKO_{VOLLH}$ | CMOS | — | — | 0.4 | V |
| Output Voltage High | $CKO_{VOHLH}$ | $V_{DD}$ = 1.71 V CMOS | 0.8 x $V_{DD}$ | — | — | V |

**Notes:**
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Drive Current (CMOS driving into $CKO_{VOL}$ for output low or $CKO_{VOH}$ for output high. CKOUT+ and CKOUT– shorted externally) | $CKO_{IO}$ | ICMOS[1:0] = 11<br>$V_{DD}$ = 1.8 V | — | 7.5 | — | mA |
| | | ICMOS[1:0] = 10<br>$V_{DD}$ = 1.8 V | — | 5.5 | — | mA |
| | | ICMOS[1:0] = 01<br>$V_{DD}$ = 1.8 V | — | 3.5 | — | mA |
| | | ICMOS[1:0] = 00<br>$V_{DD}$ = 1.8 V | — | 1.75 | — | mA |
| | | ICMOS[1:0] = 11<br>$V_{DD}$ = 3.3 V | — | 32 | — | mA |
| | | ICMOS[1:0] = 10<br>$V_{DD}$ = 3.3 V | — | 24 | — | mA |
| | | ICMOS[1:0] = 01<br>$V_{DD}$ = 3.3 V | — | 16 | — | mA |
| | | ICMOS[1:0] = 00<br>$V_{DD}$ = 3.3 V | — | 8 | — | mA |
| **2-Level LVCMOS Input Pins** | | | | | | |
| Input Voltage Low | $V_{IL}$ | $V_{DD}$ = 1.71 V | — | — | 0.5 | V |
| | | $V_{DD}$ = 2.25 V | — | — | 0.7 | V |
| | | $V_{DD}$ = 2.97 V | — | — | 0.8 | V |
| Input Voltage High | $V_{IH}$ | $V_{DD}$ = 1.89 V | 1.4 | — | — | V |
| | | $V_{DD}$ = 2.25 V | 1.8 | — | — | V |
| | | $V_{DD}$ = 3.63 V | 2.5 | — | — | V |

**Notes:**
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

**Table 2. DC Characteristics (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **3-Level Input Pins[4]** | | | | | | |
| Input Voltage Low | $V_{ILL}$ | | — | — | 0.15 x $V_{DD}$ | V |
| Input Voltage Mid | $V_{IMM}$ | | 0.45 x $V_{DD}$ | — | 0.55 x $V_{DD}$ | V |
| Input Voltage High | $V_{IHH}$ | | 0.85 x $V_{DD}$ | — | — | V |
| Input Low Current | $I_{ILL}$ | See Note 4 | –20 | — | — | µA |
| Input Mid Current | $I_{IMM}$ | See Note 4 | –2 | — | +2 | µA |
| Input High Current | $I_{IHH}$ | See Note 4 | — | — | 20 | µA |
| **LVCMOS Output Pins** | | | | | | |
| Output Voltage Low | $V_{OL}$ | IO = 2 mA<br>$V_{DD}$ = 1.71 V | — | — | 0.4 | V |
| Output Voltage Low | | IO = 2 mA<br>$V_{DD}$ = 2.97 V | — | — | 0.4 | V |
| Output Voltage High | $V_{OH}$ | IO = –2 mA<br>$V_{DD}$ = 1.71 V | $V_{DD}$ –0.4 | — | — | V |
| Output Voltage High | | IO = –2 mA<br>$V_{DD}$ = 2.97 V | $V_{DD}$ –0.4 | — | — | V |

**Notes:**
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

## Table 3. AC Specifications

($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Single-Ended Reference Clock Input Pin XA (XB with cap to GND)** | | | | | | |
| Input Resistance | $XA_{RIN}$ | RATE[1:0] = LM, MH, ac coupled | — | 12 | — | kΩ |
| Input Voltage Swing | $XA_{VPP}$ | RATE[1:0] = LM, MH, ac coupled | 0.5 | — | 1.2 | $V_{PP}$ |
| **Differential Reference Clock Input Pins (XA/XB)** | | | | | | |
| Input Voltage Swing | $XA/XB_{VPP}$ | RATE[1:0] = LM, MH | 0.5 | — | 2.4 | $V_{PP}$ |
| **CKINn Input Pins** | | | | | | |
| Input Frequency | $CKN_F$ | | 0.002 | — | 710 | MHz |
| Input Duty Cycle (Minimum Pulse Width) | $CKN_{DC}$ | Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks) | 40 | — | 60 | % |
| | | | 2 | — | — | ns |
| Input Capacitance | $CKN_{CIN}$ | | — | — | 3 | pF |
| Input Rise/Fall Time | $CKN_{TRF}$ | 20–80% See Figure 2 | — | — | 11 | ns |
| **CKOUTn Output Pins** (See ordering section for speed grade vs frequency limits) | | | | | | |
| Output Frequency (Output not configured for CMOS or Disabled) | $CKO_F$ | N1 ≥ 6 | 0.002 | — | 945 | MHz |
| | | N1 = 5 | 970 | — | 1134 | MHz |
| | | N1 = 4 | 1.213 | — | 1.4 | GHz |
| Maximum Output Frequency in CMOS Format | $CKO_F$ | | — | — | 212.5 | MHz |
| Output Rise/Fall (20–80 %) @ 622.08 MHz output | $CKO_{TRF}$ | Output not configured for CMOS or Disabled See Figure 2 | — | 230 | 350 | ps |

**Notes:**

1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan and the XAXB reference frequency. Please visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.

**Table 3. AC Specifications (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise/Fall (20–80%) @ 212.5 MHz output | $CKO_{TRF}$ | CMOS Output $V_{DD}$ = 1.71 $C_{LOAD}$ = 5 pF | — | — | 8 | ns |
| Output Rise/Fall (20–80%) @ 212.5 MHz output | $CKO_{TRF}$ | CMOS Output $V_{DD}$ = 2.97 $C_{LOAD}$ = 5 pF | — | — | 2 | ns |
| Output Duty Cycle Uncertainty @ 622.08 MHz | $CKO_{DC}$ | 100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS) | — | — | ±40 | ps |
| **LVCMOS Input Pins** | | | | | | |
| Minimum Reset Pulse Width | $t_{RSTMN}$ | | 1 | — | | µs |
| Reset to Microprocessor Access Ready | $t_{READY}$ | | — | — | 10 | ms |
| Input Capacitance | $C_{in}$ | | — | — | 3 | pF |
| **LVCMOS Output Pins** | | | | | | |
| Rise/Fall Times | $t_{RF}$ | $C_{LOAD}$ = 20pf See Figure 2 | — | 25 | — | ns |
| LOSn Trigger Window | $LOS_{TRIG}$ | From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1 | — | — | 4.5 x N3 | $T_{CKIN}$ |
| Time to Clear LOL after LOS Cleared | $t_{CLRLOL}$ | ↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference | — | 10 | — | ms |
| **Device Skew** | | | | | | |
| Output Clock Skew | $t_{SKEW}$ | ↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format PHASEOFFSET = 0 CKOUT_ALWAYS_ON = 1 SQ_ICAL = 1 | — | — | 100 | ps |

**Notes:**
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan and the XAXB reference frequency. Please visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.

**Table 3. AC Specifications (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Phase Change due to Temperature Variation[1] | $t_{TEMP}$ | Max phase changes from –40 to +85 °C | — | 300 | 500 | ps |
| **PLL Performance (fin = fout = 622.08 MHz; BW = 7 Hz; LVPECL, XAXB = 114.285 MHz)** | | | | | | |
| Lock Time[2] | $t_{LOCKMP}$ | Start of ICAL to ↓ of LOL | — | 0.8 | 1.0 | s |
| Settle Time[2] | $t_{SETTLE}$ | Start of ICAL to $F_{OUT}$ within 5 ppm of final value | — | 4.2 | 5.0 | s |
| Output Clock Phase Change | $t_{P\_STEP}$ | After clock switch f3 ≥ 128 kHz | — | 200 | — | ps |
| Closed Loop Jitter Peaking | $J_{PK}$ | | — | 0.05 | 0.1 | dB |
| Jitter Tolerance | $J_{TOL}$ | Jitter Frequency ≥ Loop Bandwidth | 5000/BW | — | — | ns pk-pk |
| Phase Noise fout = 622.08 MHz | $CKO_{PN}$ | 100 Hz Offset | — | –95 | — | dBc/Hz |
| | | 1 kHz Offset | — | –110 | — | dBc/Hz |
| | | 10 kHz Offset | — | –117 | — | dBc/Hz |
| | | 100 kHz Offset | — | –118 | — | dBc/Hz |
| | | 1 MHz Offset | — | –131 | — | dBc/Hz |
| Spurious Noise | $SP_{SPUR}$ | Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz) | — | –67 | — | dBc |

**Notes:**
1. Input to output phase skew after an ICAL is not controlled and can assume any value.
2. Lock and settle time performance is dependent on the frequency plan and the XAXB reference frequency. Please visit the Silicon Labs Technical Support web page at: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx to submit a technical support request regarding the lock time of your frequency plan.

**Table 4. Microprocessor Control**

($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$I^2C$ Bus Lines (SDA, SCL)** | | | | | | |
| Input Voltage Low | $VIL_{I2C}$ | | — | — | 0.25 x $V_{DD}$ | V |
| Input Voltage High | $VIH_{I2C}$ | | 0.7 x $V_{DD}$ | — | $V_{DD}$ | V |
| Hysteresis of Schmitt trigger inputs | $VHYS_{I2C}$ | $V_{DD}$ = 1.8 V | 0.1 x $V_{DD}$ | — | — | V |
| | | $V_{DD}$ = 2.5 or 3.3 V | 0.05 x $V_{DD}$ | — | — | V |
| Output Voltage Low | $VOL_{I2C}$ | $V_{DD}$ = 1.8 V<br>IO = 3 mA | — | — | 0.2 x $V_{DD}$ | V |
| | | $V_{DD}$ = 2.5 or 3.3 V<br>IO = 3 mA | — | — | 0.4 | V |

**Table 4. Microprocessor Control (Continued)**
($V_{DD}$ = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SPI Specifications** | | | | | | |
| Duty Cycle, SCLK | $t_{DC}$ | SCLK = 10 MHz | 40 | — | 60 | % |
| Cycle Time, SCLK | $t_c$ | | 100 | — | — | ns |
| Rise Time, SCLK | $t_r$ | 20–80% | — | — | 25 | ns |
| Fall Time, SCLK | $t_f$ | 20–80% | — | — | 25 | ns |
| Low Time, SCLK | $t_{lsc}$ | 20–20% | 30 | — | — | ns |
| High Time, SCLK | $t_{hsc}$ | 80–80% | 30 | — | — | ns |
| Delay Time, SCLK Fall to SDO Active | $t_{d1}$ | | — | — | 25 | ns |
| Delay Time, SCLK Fall to SDO Transition | $t_{d2}$ | | — | — | 25 | ns |
| Delay Time, SS Rise to SDO Tri-state | $t_{d3}$ | | — | — | 25 | ns |
| Setup Time, SS to SCLK Fall | $t_{su1}$ | | 25 | — | — | ns |
| Hold Time, SS to SCLK Rise | $t_{h1}$ | | 20 | — | — | ns |
| Setup Time, SDI to SCLK Rise | $t_{su2}$ | | 25 | — | — | ns |
| Hold Time, SDI to SCLK Rise | $t_{h2}$ | | 20 | — | — | ns |
| Delay Time between Slave Selects | $t_{cs}$ | | 25 | — | — | ns |

**Table 5. Jitter Generation**

| Parameter | Symbol | Test Condition* | | Min | Typ | Max | GR-253-Specification | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Measurement Filter | DSPLL BW[2] | | | | | |
| Jitter Gen OC-192 | JGEN | 0.02–80 MHz | 120 Hz | — | 4.2 | — | 30 | $ps_{PP}$ |
| | | | | — | .27 | — | N/A | $ps_{rms}$ |
| | | 4–80 MHz | 120 Hz | — | 3.7 | — | 10 | $ps_{PP}$ |
| | | | | — | .14 | — | N/A | $ps_{rms}$ |
| | | 0.05–80 MHz | 120 Hz | — | 4.4 | — | 10 | $ps_{PP}$ |
| | | | | — | .26 | — | 1.0 | $ps_{rms}$ |
| Jitter Gen OC-48 | JGEN | 0.12–20 MHz | 120 Hz | — | 3.5 | — | 40.2 | $ps_{PP}$ |
| | | | | — | .27 | — | 4.02 | $ps_{rms}$ |

***Note:** Test conditions:

1. fIN = fOUT = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 120 Hz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. $V_{DD}$ = 2.5 V
7. $T_A$ = 85 °C
8. Jitter integration bands include low-pass (-20 dB/dec) and high-pas (-60 dB/dec) roll-offs per Telecordia GR-253-CORE.

### Table 6. Thermal Characteristics

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still Air | 31 | C°/W |

### Table 7. Absolute Maximum Ratings*

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | | –0.5 | — | 3.8 | V |
| LVCMOS Input Voltage | $V_{DIG}$ | | –0.3 | — | $V_{DD}$+0.3 | V |
| CKINn Voltage Level Limits | $CKN_{VIN}$ | | 0 | — | $V_{DD}$ | V |
| XA/XB Voltage Level Limits | $XA_{VIN}$ | | 0 | — | 1.2 | V |
| Operating Junction Temperature | $T_{JCT}$ | | –55 | — | 150 | ºC |
| Storage Temperature Range | $T_{STG}$ | | –55 | — | 150 | ºC |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN– | | | 2 | — | — | kV |
| ESD MM Tolerance; All pins except CKIN+/CKIN– | | | 150 | — | — | V |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN– | | | 700 | — | — | V |
| ESD MM Tolerance; CKIN+/CKIN– | | | 100 | — | — | V |
| Latch-up Tolerance | | | JESD78 Compliant | | | |

***Note:** Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

## 2. Typical Phase Noise Performance

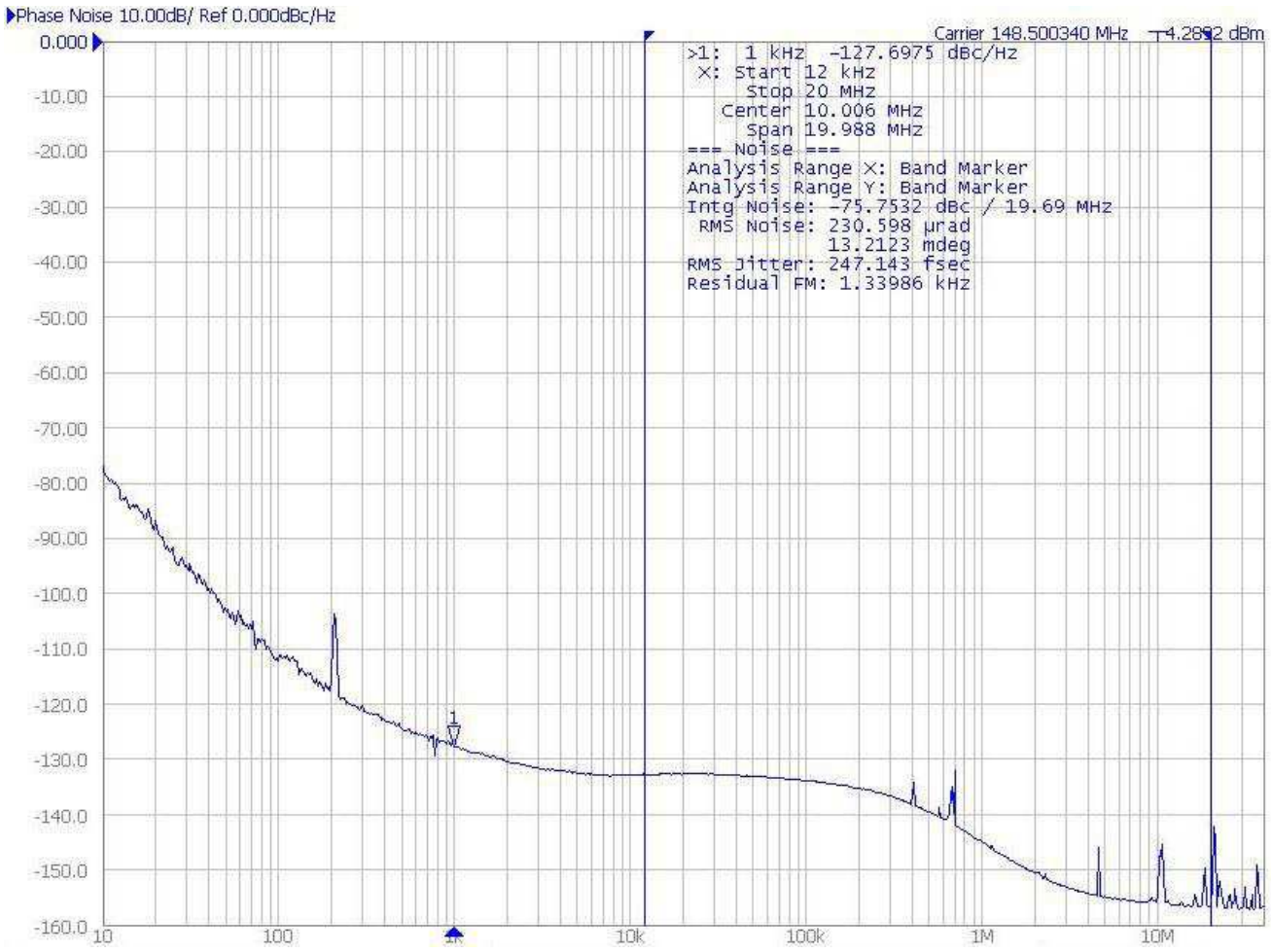



**Figure 3. Broadcast Video***

***Note:** Phase noise plot RMS jitter value used brick wall integration.

| Jitter Bandwidth | Jitter (peak-peak) | Jitter (RMS) |
|---|---|---|
| 10 Hz to 20 MHz | 5.24 ps | 484 |
| **Note:** Number of samples: 8.91E9 | | |

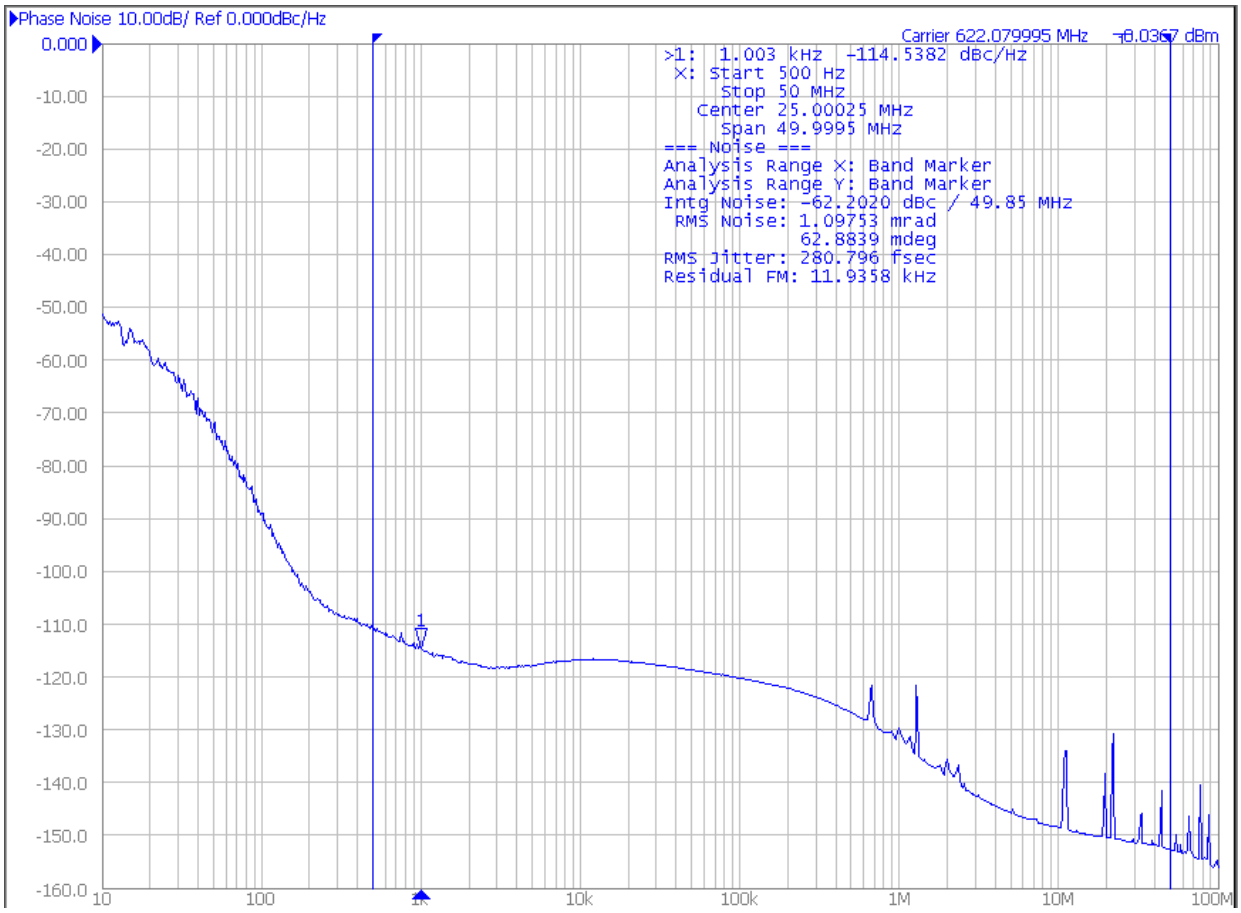



**Figure 4. OTN/SONET/SDH Phase Noise***

***Note:** Phase noise plot RMS jitter value uses brick wall integration.

| Jitter Bandwidth | Jitter, RMS |
|---|---|
| SONET_OC48, 12 kHz to 20 MHz | 266 fs |
| SONET_OC192_A, 20 kHz to 80 MHz | 283 fs |
| SONET_OC192_B, 4 MHz to 80 MHz | 155 fs |
| SONET_OC192_C, 50 kHz to 80 MHz | 275 fs |
| Brick Wall_800 Hz to 80 MHz | 287 fs |
| **Note:** Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE. | |

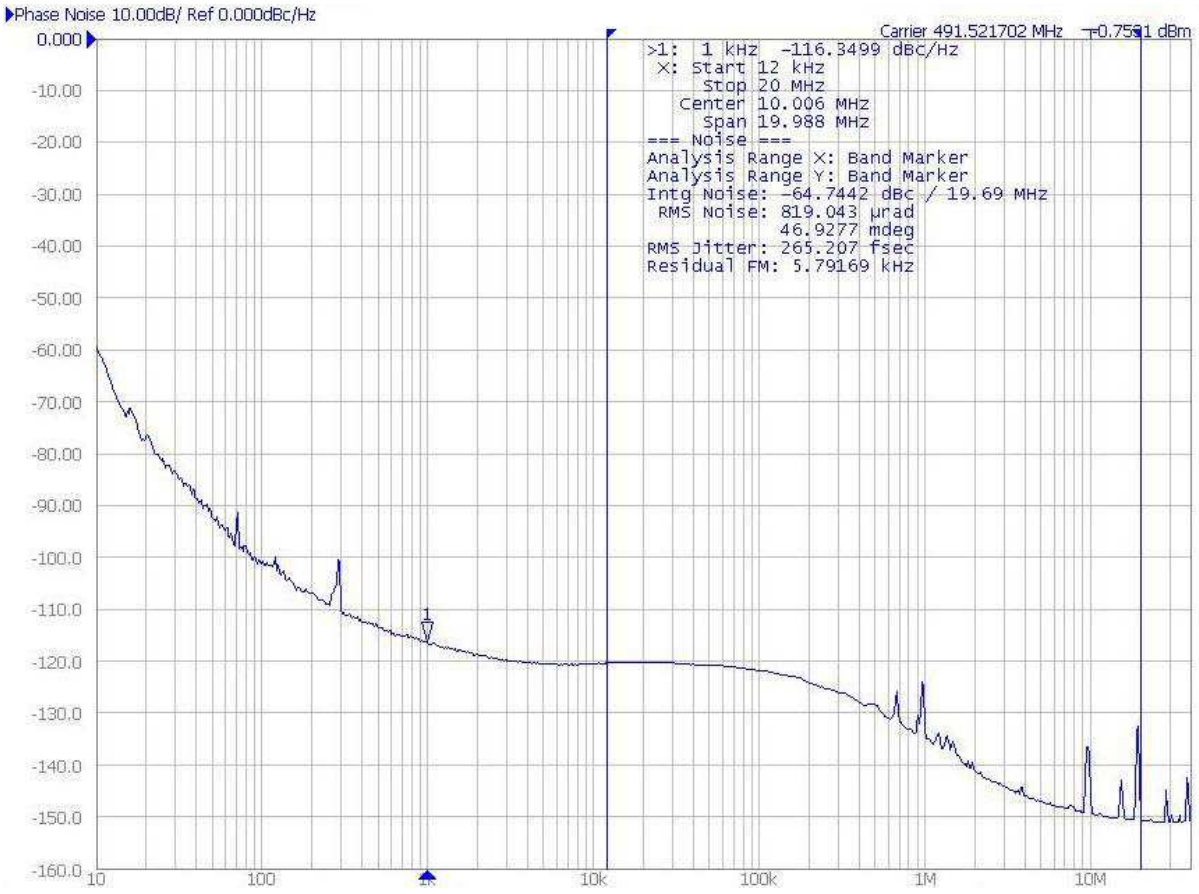



**Figure 5. Wireless Base Station Phase Noise***

***Note:** Phase noise plot RMS jitter value uses brick wall integration.

| Jitter Bandwidth | Jitter (peak-peak) | Jitter (RMS) |
|---|---|---|
| 10 Hz to 20 MHz | 7.28 ps | 581 |
| **Note:** Number of samples: 8.91E9 | | |

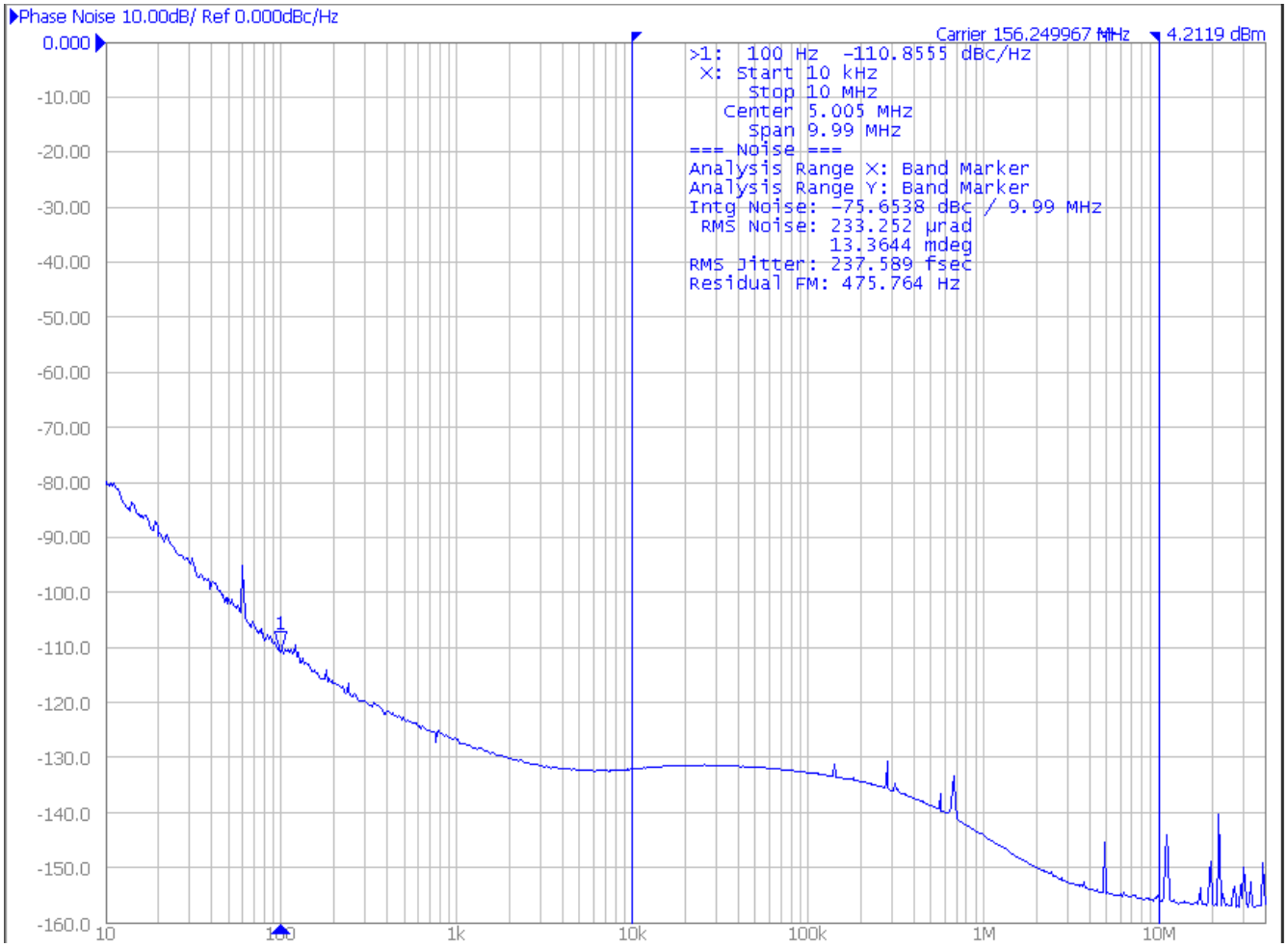
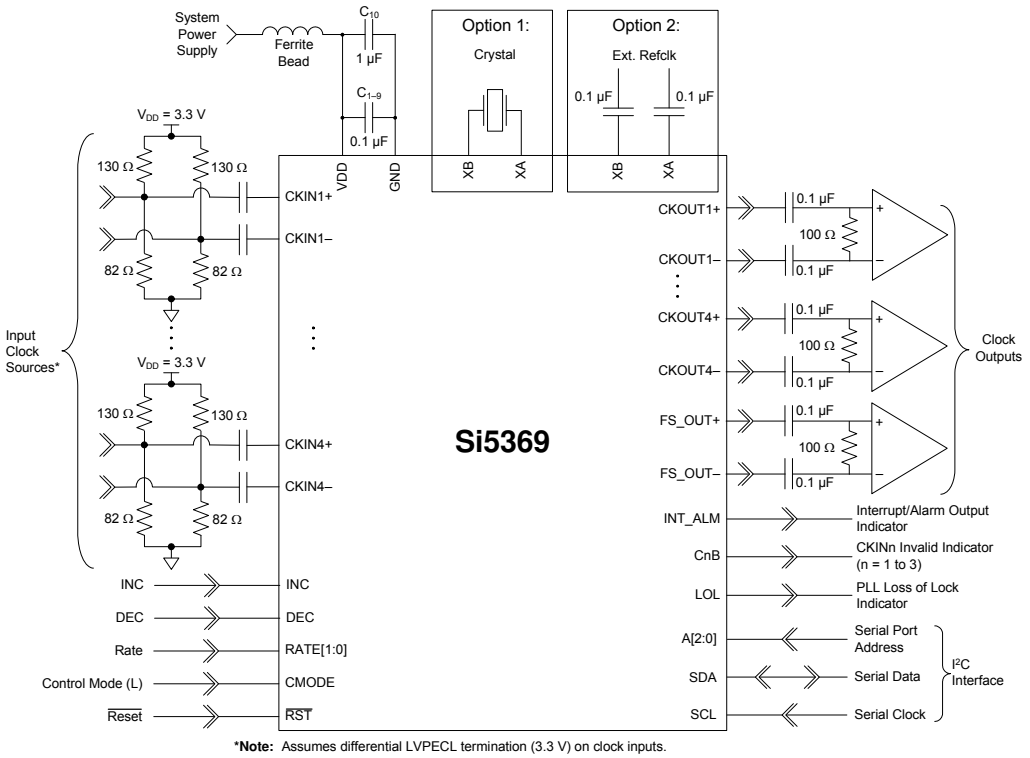



**Figure 6. 10 GbE Phase Noise***

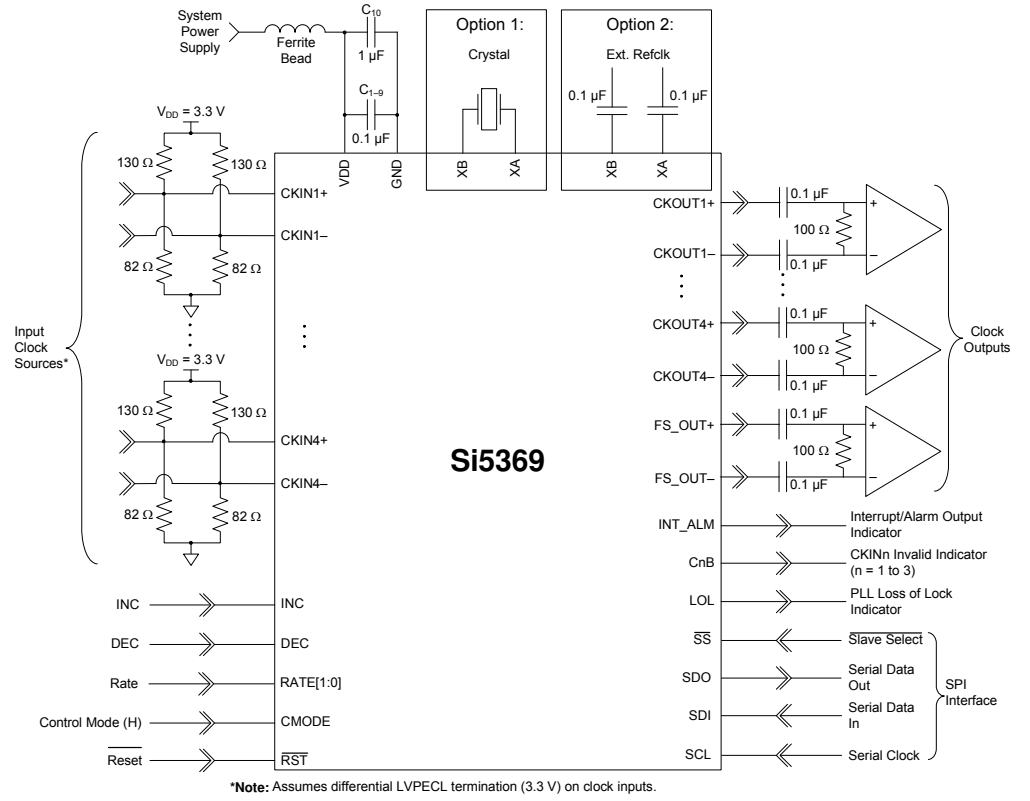
***Note:** Phase noise plot RMS jitter value uses brick wall integration.

| Jitter Bandwidth | Jitter (RMS) |
|---|---|
| 10 kHz to 10 MHz | 238 fs |




***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

**Figure 7. Si5369 Typical Application Circuit (I²C Control Mode)**




***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

**Figure 8. Si5369 Typical Application Circuit (SPI Control Mode)**

# 3. Functional Description

The Si5369 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps rms jitter performance. The Si5369 accepts four clock inputs ranging from 2 kHz to 710 MHz and generates five clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for every input clock and output clock, so the Si5369 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5369 input clock frequency and clock multiplication ratio are programmable through an $I^2C$ or SPI interface. Optionally, the fifth clock output can be configured as a 2 to 512 kHz SONET/SDH frame synchronization output that is phase aligned with one of the high-speed output clocks. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5369 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5369 PLL loop bandwidth is digitally programmable and supports a range from 4 to 525 Hz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5369 supports hitless switching between input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual, automatic revertive and non-revertive input clock switching options are available. The Si5369 monitors the four input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on any of the four input clocks. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. The Si5369 monitors the frequency of CKIN1, CKIN2, CKIN3, and CKIN4 with respect to a selected reference frequency and generates a frequency offset alarm (FOS) if the threshold is exceeded. This FOS feature is available for SONET applications in which both the monitored frequency on CKIN1, CKIN3, and CKIN4 and the reference frequency are integer multiples of 19.44 MHz. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported.

The Si5369 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5369 has five differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the DSPLL*sim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

## 3.1. External Reference

An external clock or a low-cost 114.285 MHz 3rd overtone crystal is typically used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to operate. Silicon Laboratories recommends using a high-quality crystal. Specific recommendations may be found in the Family Reference Manual. An external clock from a high-quality OCXO or TCXO can also be used as a reference for the device.

If there is a need to use a reference oscillator instead of a crystal, Silicon Labs does not recommend using MEMS based oscillators. Instead, Silicon Labs recommends the Si530EB121M109DG, which is a very low jitter/wander, LVPECL, 2.5 V crystal oscillator. The very low loop BW of the Si5369 means that it can be susceptible to XAXB reference sources that have high wander. Experience has shown that in spite of having low jitter, some MEMs oscillators have high wander, and these devices should be avoided. Contact Silicon Labs for details.

In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold, will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

### 3.2. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5369. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, frequency planning, and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

## 4. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | | FREE_RUN | CKOUT_ ALWAYS_ ON | | | | BYPASS_ REG | |
| 1 | CK_PRIOR4 [1:0] | | CK_PRIOR3 [1:0] | | CK_PRIOR2 [1:0] | | CK_PRIOR1 [1:0] | |
| 2 | BWSEL_REG [3:0] | | | | | | | |
| 3 | CKSEL_REG [1:0] | | DHOLD | SQ_ICAL | | | | |
| 4 | AUTOSEL_REG [1:0] | | | HIST_DEL [4:0] | | | | |
| 5 | ICMOS [1:0] | | SFOUT2_REG [2:0] | | | SFOUT1_REG [2:0] | | |
| 6 | | | SFOUT4_REG [2:0] | | | SFOUT3_REG [2:0] | | |
| 7 | | | SFOUT5_REG [2:0] | | | FOSREFSEL [2:0] | | |
| 8 | HLOG_4 [1:0] | | HLOG_3 [1:0] | | HLOG_2 [1:0] | | HLOG_1 [1:0] | |
| 9 | HIST_AVG [4:0] | | | | | | HLOG_5 [1:0] | |
| 10 | | | DSBL5_ REG | | DSBL4_ REG | DSBL3_ REG | DSBL2_ REG | DSBL1_ REG |
| 11 | | | | | PD_CK4 | PD_CK3 | PD_CK2 | PD_CK1 |
| 19 | FOS_EN | FOS_THR [1:0] | | VALTIME [1:0] | | LOCKT [2:0] | | |
| 20 | | | ALR- MOUT_PIN | CK3_BAD_ PIN | CK2_BAD_ PIN | CK1_BAD_ PIN | LOL_PIN | INT_PIN |
| 21 | | | | CK4_ACT- V_PIN | CK3_ACT- V_PIN | CK2_ACT- V_PIN | CK1_ACT- V_PIN | CKSEL_PIN |
| 22 | | | | | CK_ACTV_ POL | CK_BAD_ POL | LOL_POL | INT_POL |
| 23 | | | | LOS4_MSK | LOS3_MSK | LOS2_MSK | LOS1_MSK | LOSX_MSK |
| 24 | | | | FOS4_MSK | FOS3_MSK | FOS2_MSK | FOS1_MSK | LOL_MSK |
| 25 | N1_HS [2:0] | | | | NC1_LS [19:16] | | | |
| 26 | NC1_LS [15:8] | | | | | | | |
| 27 | NC1_LS [7:0] | | | | | | | |
| 28 | | | | | NC2_LS [19:16] | | | |
| 29 | NC2_LS [15:8] | | | | | | | |
| 30 | NC2_LS [7:0] | | | | | | | |
| 31 | | | | | NC3_LS [19:16] | | | |

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 32 | NC3_LS [15:8] | | | | | | | |
| 33 | NC3_LS [7:0] | | | | | | | |
| 34 | | | | | NC4_LS [19:16] | | | |
| 35 | NC4_LS [15:8] | | | | | | | |
| 36 | NC4_LS [7:0] | | | | | | | |
| 37 | | | | | NC5_LS [19:16] | | | |
| 38 | NC5_LS [15:8] | | | | | | | |
| 39 | NC5_LS [7:0] | | | | | | | |
| 40 | N2_HS [2:0] | | | | N2_LS [19:16] | | | |
| 41 | N2_LS [15:8] | | | | | | | |
| 42 | N2_LS [7:0] | | | | | | | |
| 43 | | | | | | N31_ [18:16] | | |
| 44 | N31_[15:8] | | | | | | | |
| 45 | N31_ [7:0] | | | | | | | |
| 46 | | | | | | N32_ [18:16] | | |
| 47 | N31_ [15:8] | | | | | | | |
| 48 | N32_[7:0] | | | | | | | |
| 49 | | | | | | N33_[18:16] | | |
| 50 | N33_[15:8] | | | | | | | |
| 51 | N33_[7:0] | | | | | | | |
| 52 | | | | | | N34_[18:16] | | |
| 53 | N34_[15:8] | | | | | | | |
| 54 | N34_[7:0] | | | | | | | |
| 55 | | | CLKIN2RATE_[2:0] | | | CLKIN1RATE[2:0] | | |
| 56 | | | CLKIN4RATE_[2:0] | | | CLKIN3RATE[2:0] | | |
| 128 | | | | | CK4_ACT-V_REG | CK3_ACT-V_REG | CK2_ACT-V_REG | CK1_ACT-V_REG |
| 129 | | | | LOS4_INT | LOS3_INT | LOS2_INT | LOS1_INT | LOSX_INT |
| 130 | | DIGHOLD-VALID | | FOS4_INT | FOS3_INT | FOS2_INT | FOS1_INT | LOL_INT |
| 131 | | | | LOS4_FLG | LOS3_FLG | LOS2_FLG | LOS1_FLG | LOSX_FLG |

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 132 | | | FOS4_FLG | FOS3_FLG | FOS2_FLG | FOS1_FLG | LOL_FLG | |
| 134 | PARTNUM_RO [11:4] | | | | | | | |
| 135 | PARTNUM_RO [3:0] | | | | REVID_RO [3:0] | | | |
| 136 | RST_REG | ICAL | | | | | | |
| 137 | | | | | | | | FASTLOCK |
| 138 | | | | | LOS4_EN [1:1] | LOS3_EN [1:1] | LOS2_EN [1:1] | LOS1_EN [1:1] |
| 139 | LOS4_EN [0:0] | LOS3_EN [0:0] | LOS2_EN [0:0] | LOS1_EN [0:0] | FOS4_EN | FOS3_EN | FOS2_EN | FOS1_EN |
| 140 | INDEPENDENTSKEW1 [7:0] | | | | | | | |
| 141 | INDEPENDENTSKEW2 [7:0] | | | | | | | |
| 142 | INDEPENDENTSKEW3 [7:0] | | | | | | | |
| 143 | INDEPENDENTSKEW4 [7:0] | | | | | | | |
| 144 | INDEPENDENTSKEW5 [7:0] | | | | | | | |

# 5. Register Descriptions

**Register 0.**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | | FREE_RUN | CKOUT_ALWAYS_ON | | | | BYPASS_REG | |
| Type | R | R/W | R/W | R | R | R | R/W | R |

Reset value = 0001 0100

| Bit | Name | Function |
|---|---|---|
| 7 | Reserved | |
| 6 | FREE_RUN | **Free Run.**<br>Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its external reference.<br>0: Disable Free Run<br>1: Enable |
| 5 | CKOUT_ALWAYS_ON | **CKOUT Always On.**<br>This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 8.<br>0: Squelch output until part is calibrated (ICAL).<br>1: Provide an output. Note: The frequency may be significantly off until the part is calibrated. |
| 4:2 | Reserved | |
| 1 | BYPASS_REG | **Bypass Register.**<br>This bit enables or disables the PLL bypass mode. Use is only valid when the part is in digital hold or before the first ICAL.<br>0: Normal operation<br>1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL. |
| 0 | Reserved | |