



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 12	0.027 at $V_{GS} = - 4.5$ V	- 8.1
	0.0335 at $V_{GS} = - 2.5$ V	- 7.3
	0.045 at $V_{GS} = - 1.8$ V	- 6.3

FEATURES

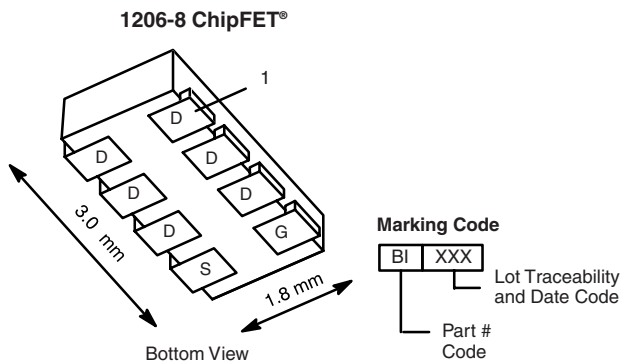
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- Low $R_{DS(on)}$ and Excellent Power Handling in Compact Footprint



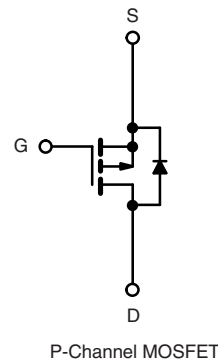
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Battery and Load Switch for Portable Devices



Ordering Information: Si5473DC-T1-E3 (Lead (Pb)-free)
Si5473DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	- 8.1	- 5.9	A
		- 5.9	- 4.3	
Pulsed Drain Current	I_{DM}	± 20		
Continuous Source Current ^a	I_S	- 2.1	- 1.1	
Maximum Power Dissipation ^a	P_D	2.5	1.3	W
		1.3	0.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	40	50	$^\circ\text{C/W}$
		80	95	
Maximum Junction-to-Foot (Drain)	R_{thJF}	15	20	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted

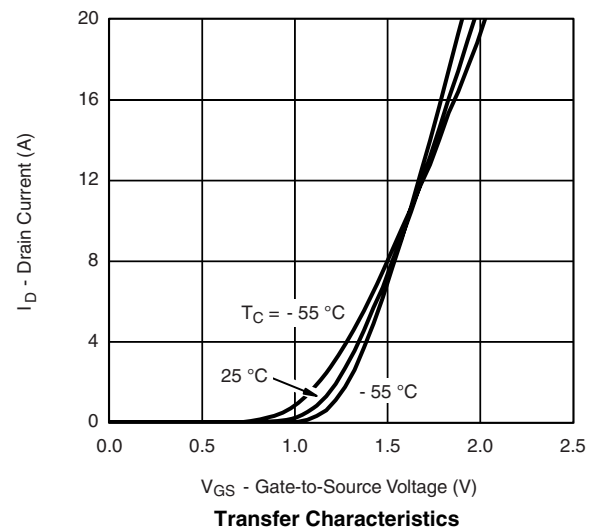
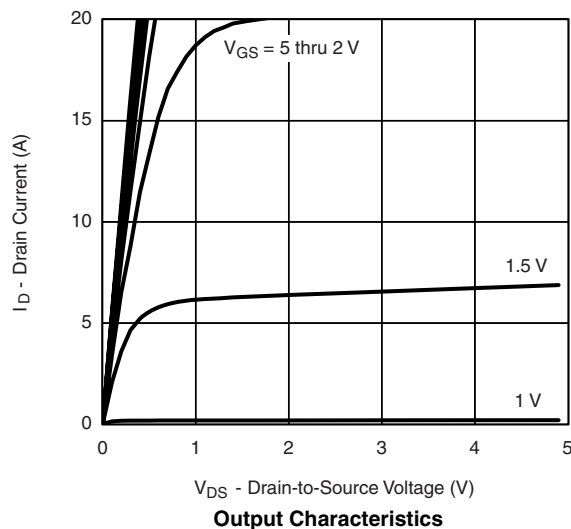
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-0.40		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -9.6\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -9.6\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -5.9\text{ A}$		0.022	0.027	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -5.3\text{ A}$		0.028	0.0335	
		$V_{GS} = -1.8\text{ V}$, $I_D = -2.2\text{ A}$		0.036	0.045	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5\text{ V}$, $I_D = -5.9\text{ A}$		20		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.1\text{ A}$, $V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -5.9\text{ A}$		21	32	nC
Gate-Source Charge	Q_{gs}			3.1		
Gate-Drain Charge	Q_{gd}			6.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}$, $R_L = 6\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_G = 6\text{ }\Omega$		25	40	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			145	220	
Fall Time	t_f			90	135	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.1\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$		70	105	

Notes:

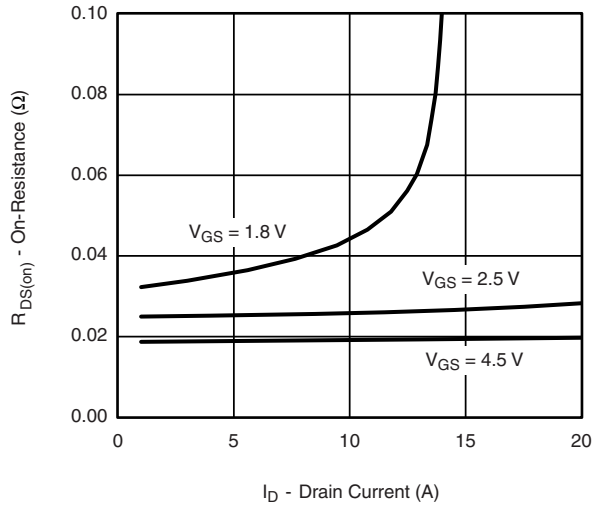
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

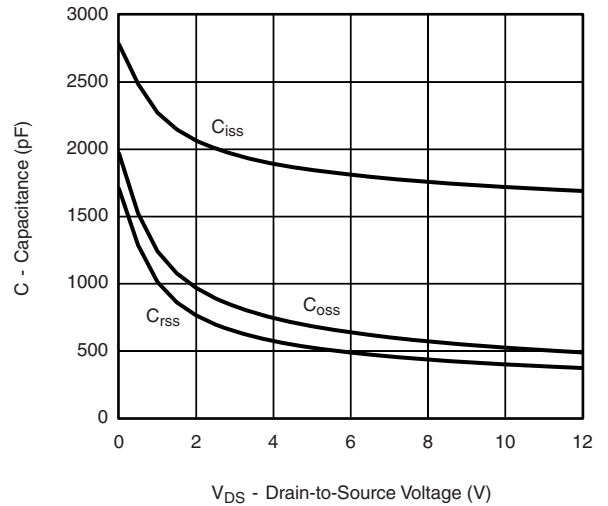
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

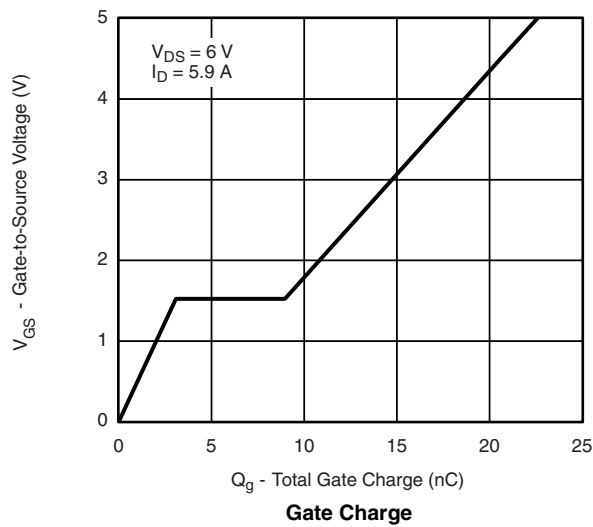
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



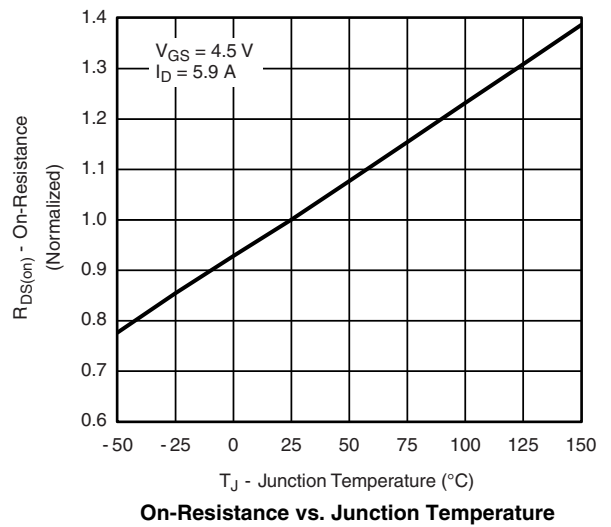
On-Resistance vs. Drain Current



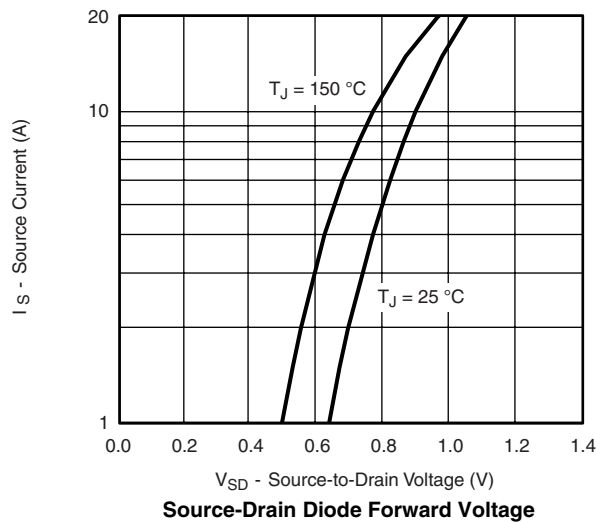
Capacitance



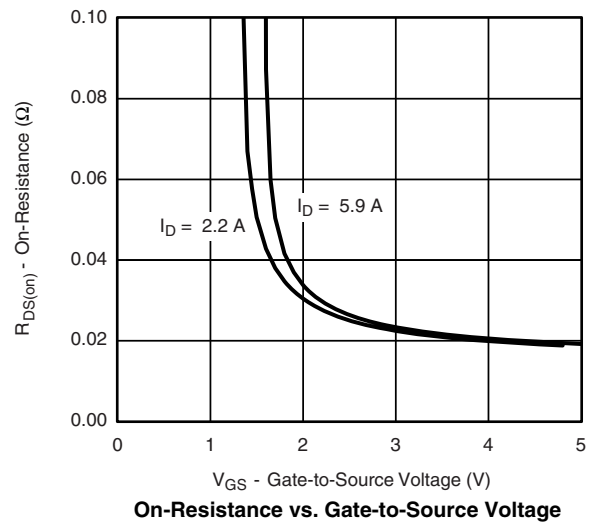
Gate Charge



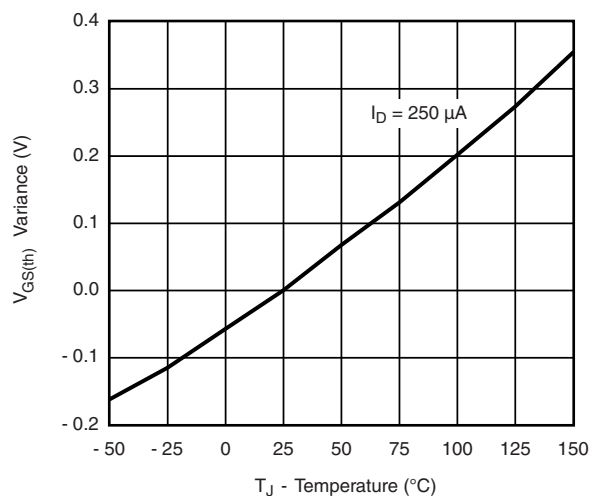
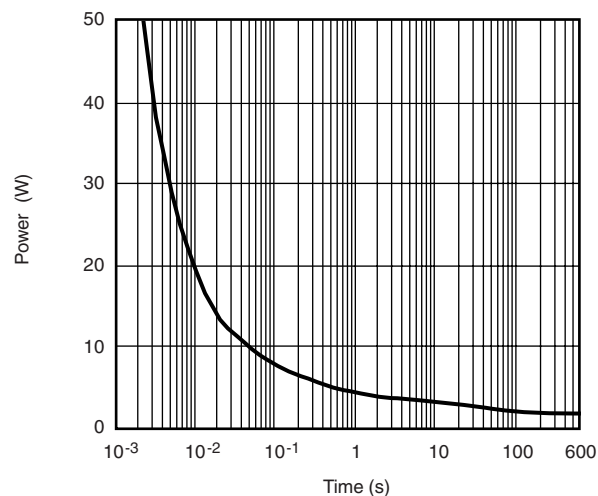
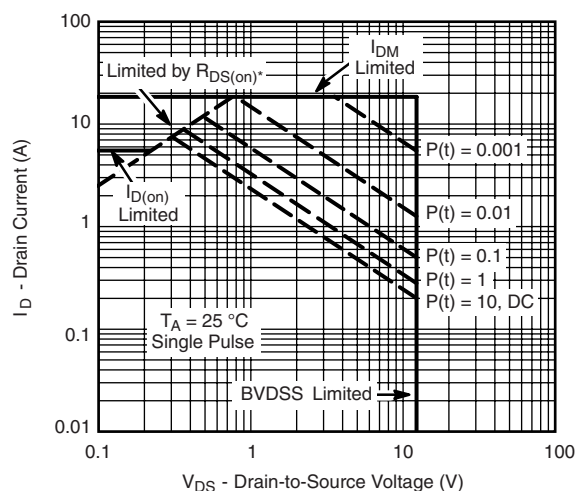
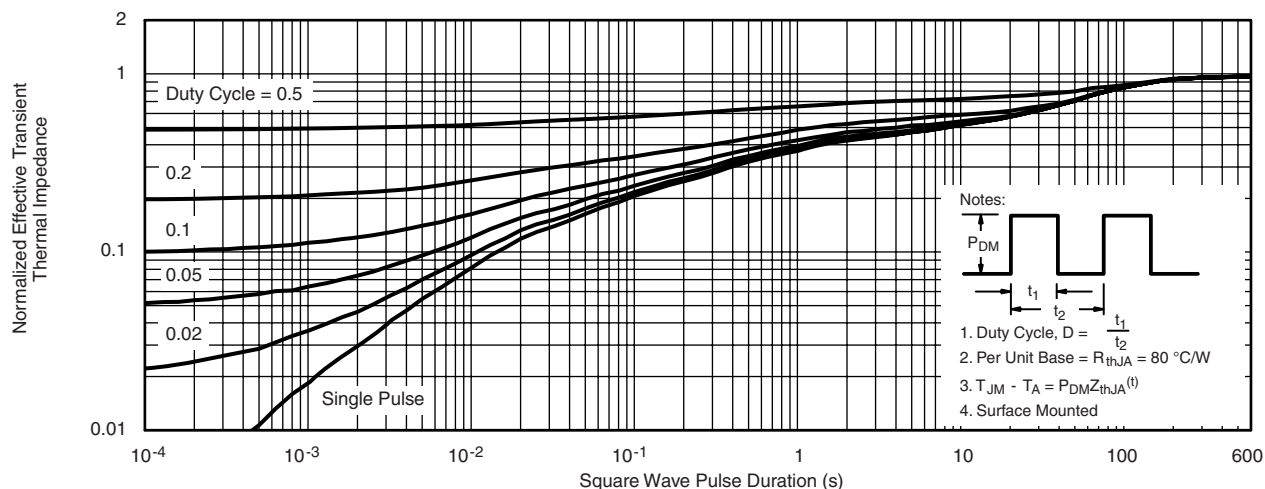
On-Resistance vs. Junction Temperature



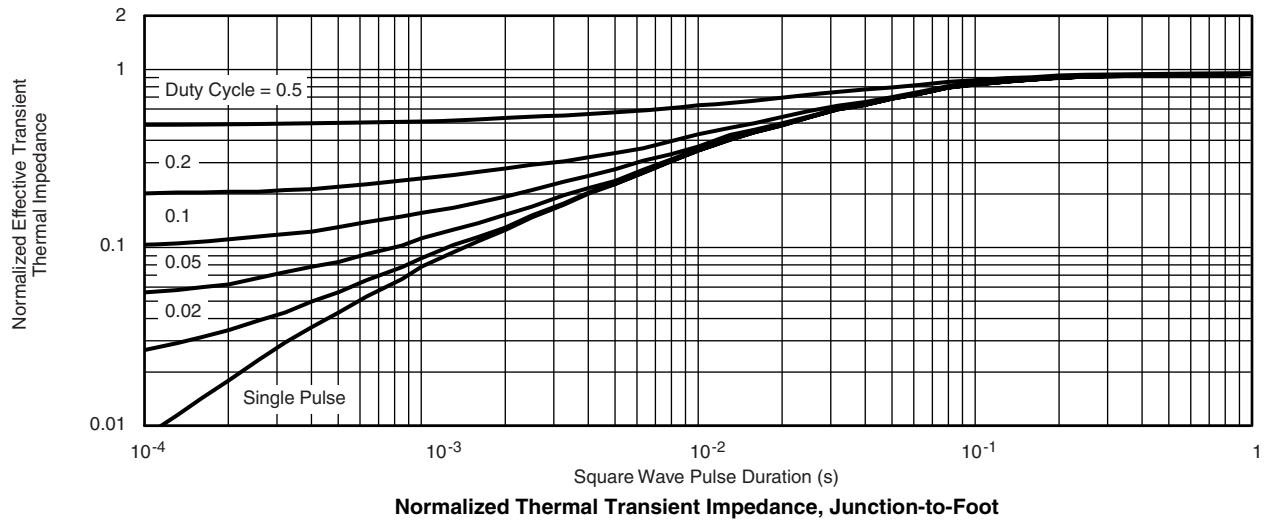
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Threshold Voltage****Single Pulse Power*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area****Normalized Thermal Transient Impedance, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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