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Dual P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 8	0.070 at $V_{GS} = - 4.5$ V	- 4.6
	0.108 at $V_{GS} = - 2.5$ V	- 3.7
	0.162 at $V_{GS} = - 1.8$ V	- 3.0

FEATURES

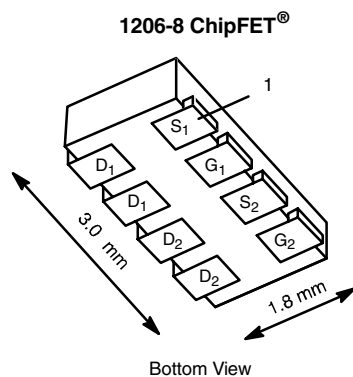
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Low Thermal Resistance
- 40 % Smaller Footprint than TSOP-6
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

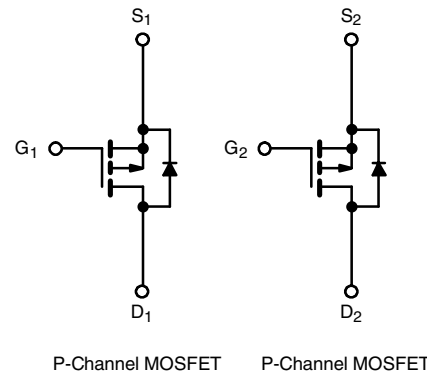
- Load Switch or PA Switch for Portable Devices



Marking Code



Ordering Information: Si5915DC-T1-E3 (Lead (Pb)-free)
Si5915DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	- 8		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	- 4.6	- 3.4	A
		$T_A = 85$ °C	- 3.3	- 2.5	
Pulsed Drain Current	I_{DM}	- 10		A	
Continuous Source Current (Diode Conduction) ^a	I_S	- 1.8	- 0.9		
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	2.1	1.1	W
		$T_A = 85$ °C	1.1	0.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ s	50	60	°C/W
		Steady State	90	110	
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- See reliability manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -6.4\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -6.4\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-10			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$		0.058	0.070	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -2.7\text{ A}$		0.090	0.108	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.131	0.162	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5\text{ V}, I_D = -3.4\text{ A}$		8		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -0.9\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$		5.9	9	nC
Gate-Source Charge	Q_{gs}		1.3			
Gate-Drain Charge	Q_{gd}		1.4			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$		20	30	ns
Rise Time	t_r		70	110		
Turn-Off Delay Time	$t_{d(off)}$		35	55		
Fall Time	t_f		35	55		
Source-Drain Reverse Recovery Time	t_{rr}		$I_F = -0.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		30	

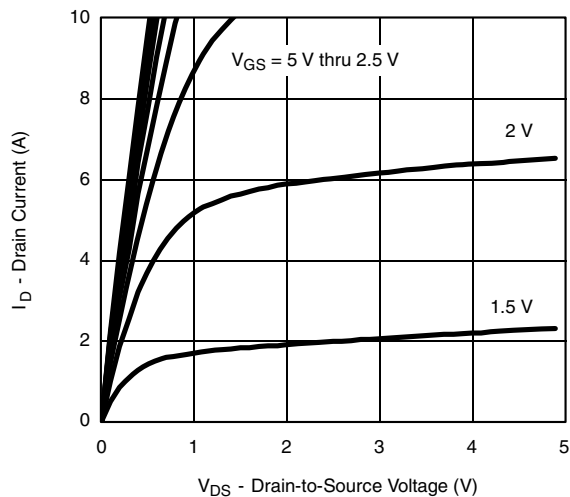
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

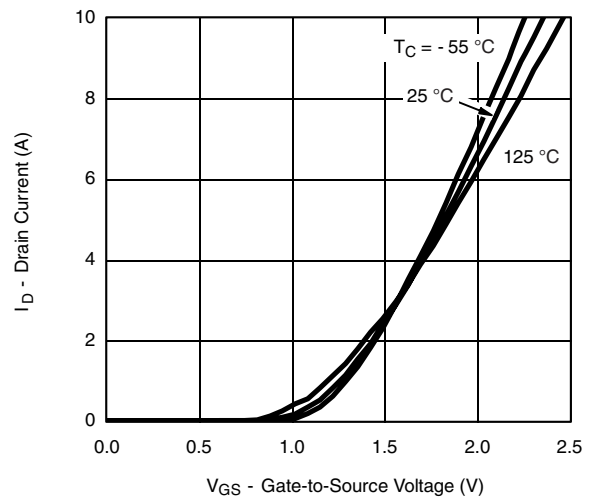
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

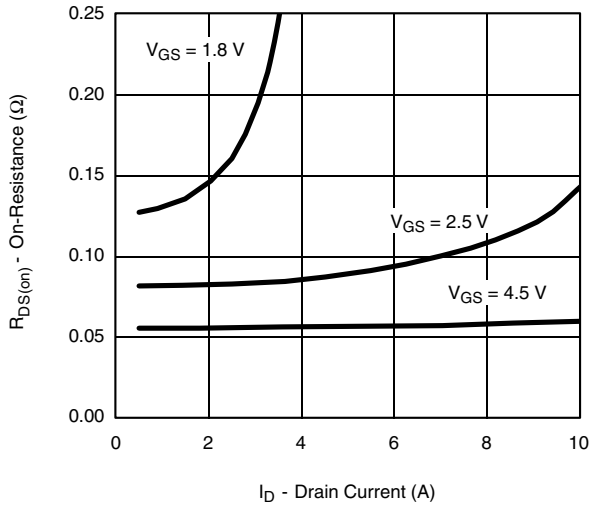


Output Characteristics

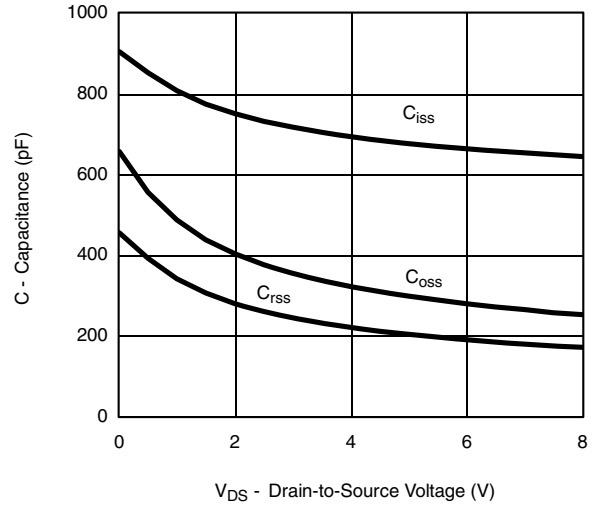


Transfer Characteristics

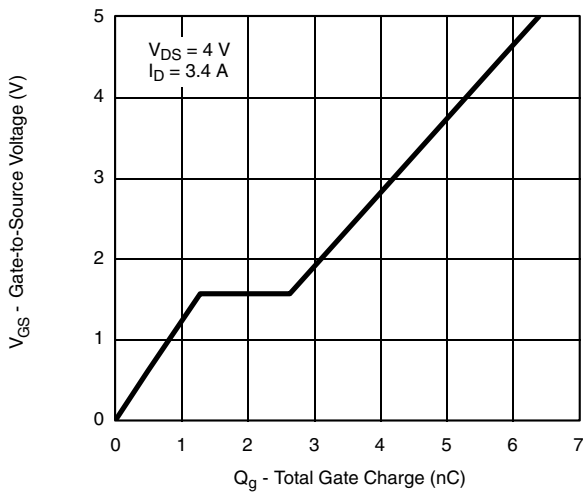
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



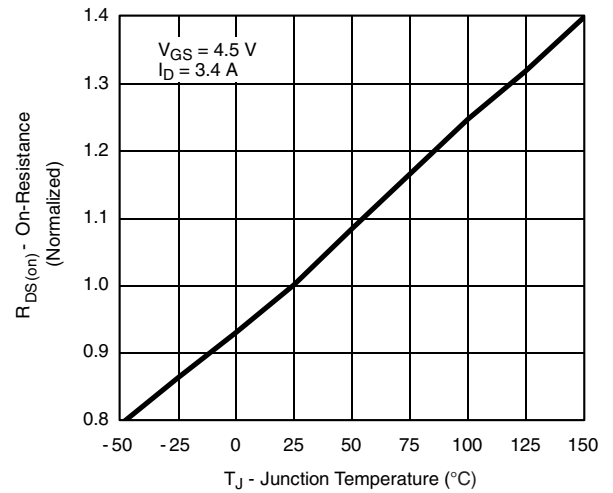
On-Resistance vs. Drain Current



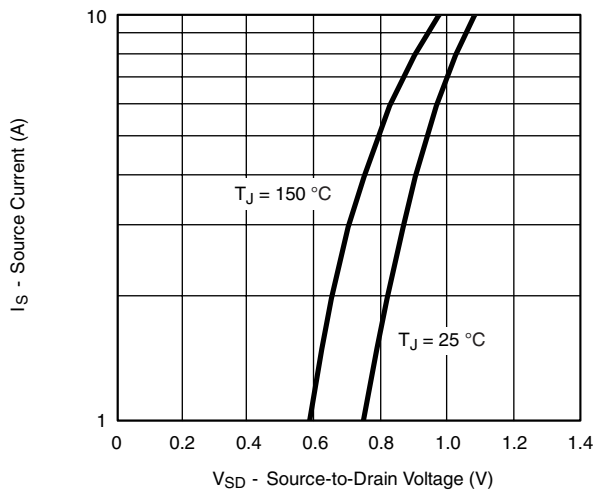
Capacitance



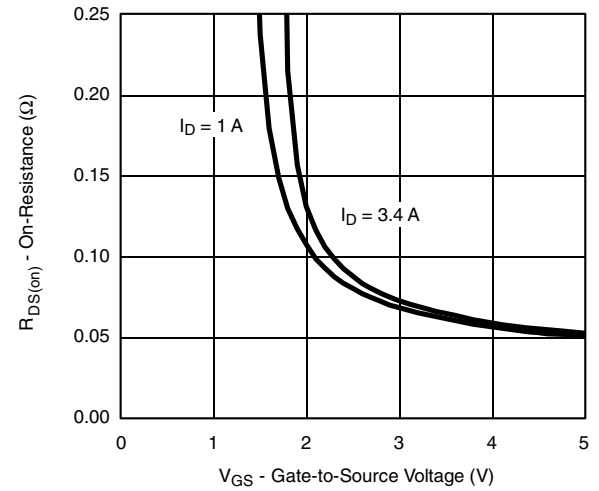
Gate Charge



On-Resistance vs. Junction Temperature

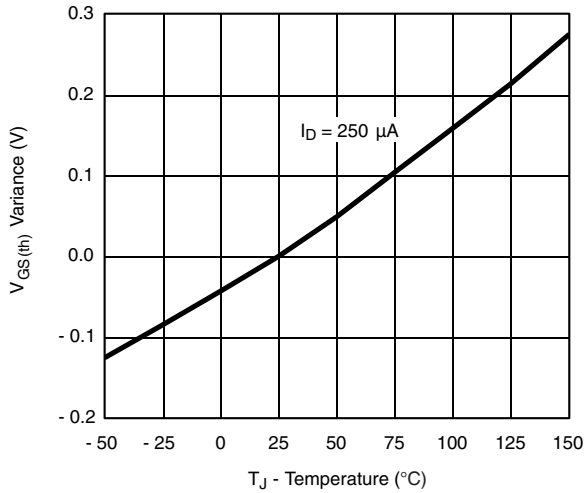


Source-Drain Diode Forward Voltage

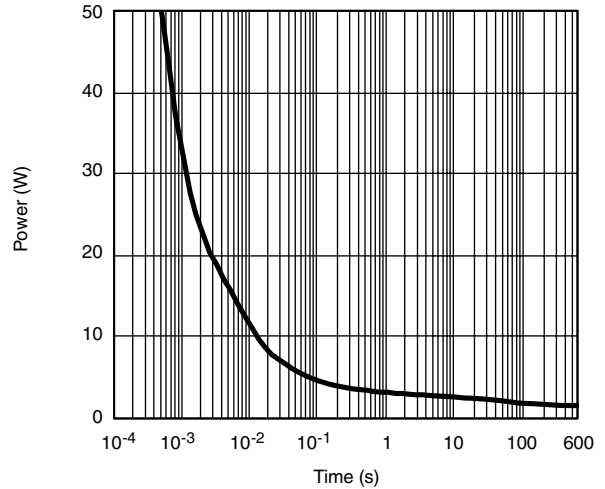


On-Resistance vs. Gate-to-Source Voltage

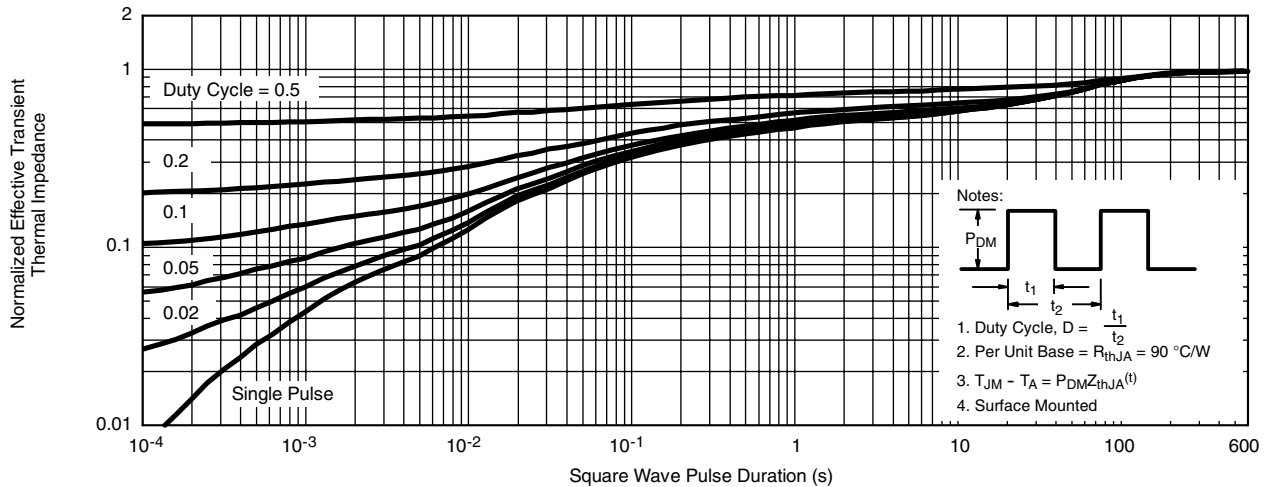
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



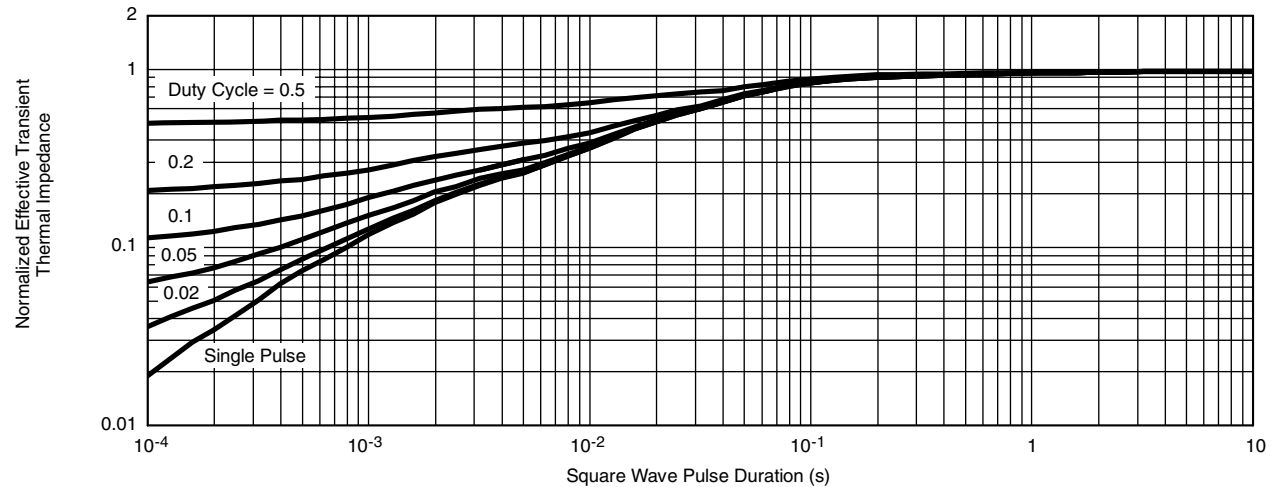
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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