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N-Channel 30 V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
30	0.013 at V _{GS} = 10 V	13.3
	0.015 at V _{GS} = 4.5 V	12.4
	0.022 at V _{GS} = 2.5 V	10.2

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

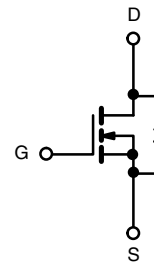
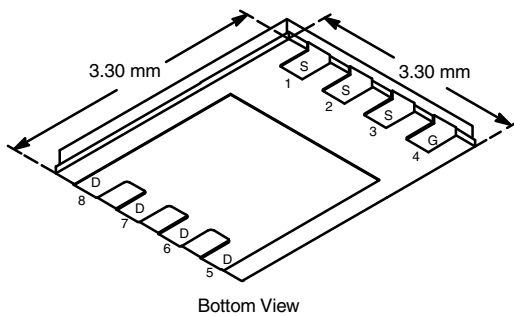


RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Li-Ion Battery Protection

PowerPAK® 1212-8



N-Channel MOSFET

Ordering Information: Si7404DN-T1-E3 (Lead (Pb)-free)
Si7404DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	30		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	13.3	8.5	A
		T _A = 70 °C	10.6	6.8	
Pulsed Drain Current	I _{DM}	40			
Single Avalanche Current	I _{AS}	15			
Single Avalanche Energy (Duty Cycle 1 %)	E _{AS}	11		mJ	
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3	A	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8	1.5	W
		T _A = 70 °C	2.0	0.8	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations ^{b,c}		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	26	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.4	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

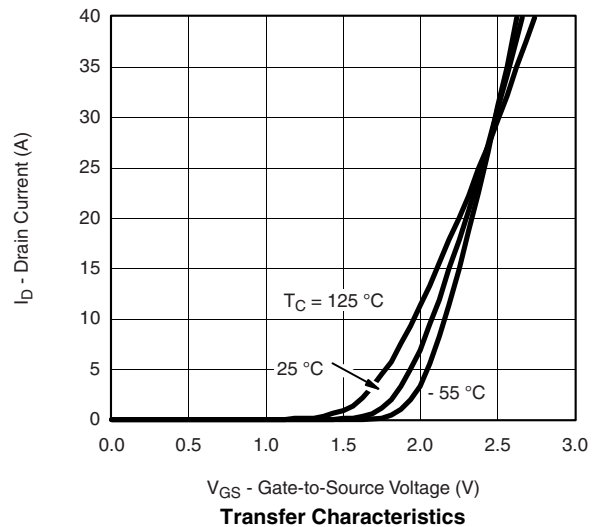
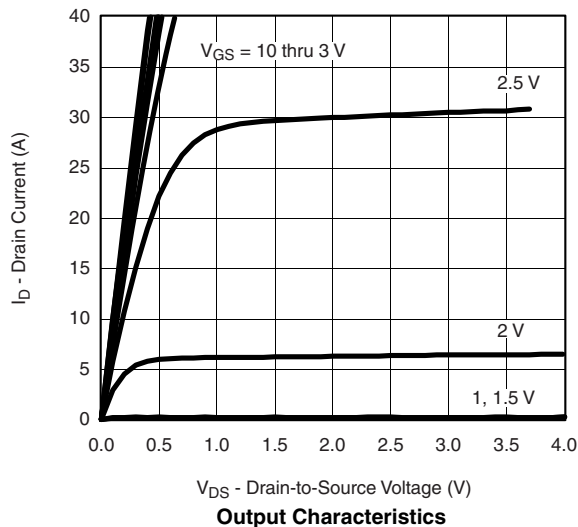
MOSFET SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 13.3\text{ A}$		0.010	0.013	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 12.4\text{ A}$		0.0125	0.015	
		$V_{GS} = 2.5\text{ V}, I_D = 5\text{ A}$		0.019	0.022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 13.3\text{ A}$		50		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 13.3\text{ A}$		20	30	nC
Gate-Source Charge	Q_{gs}			5.8		
Gate-Drain Charge	Q_{gd}			7.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$		27	40	ns
Rise Time	t_r			39	60	
Turn-Off Delay Time	$t_{d(off)}$			64	100	
Fall Time	t_f			33	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		45	90	

Notes:

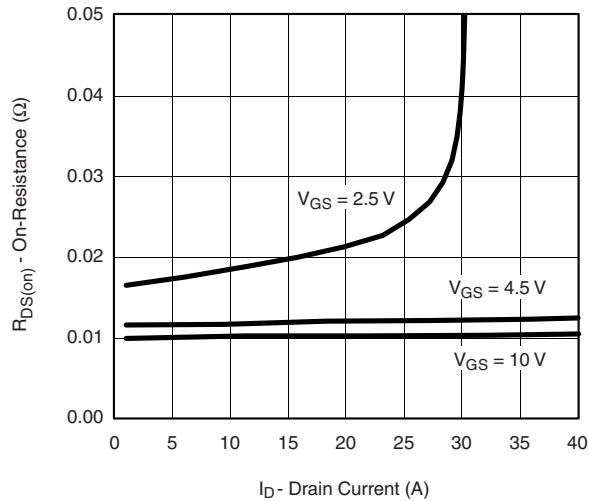
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

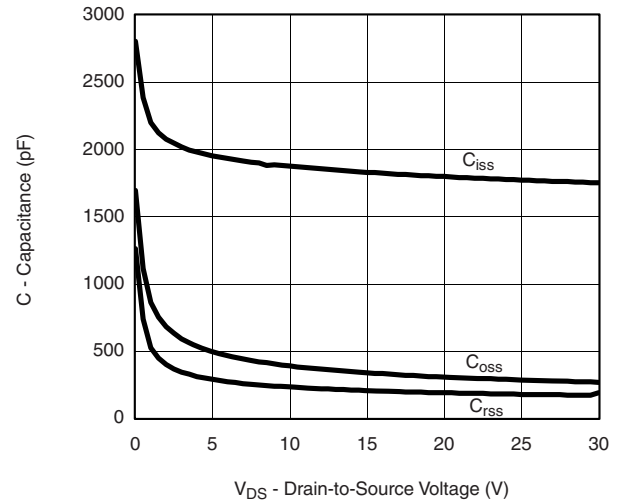
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



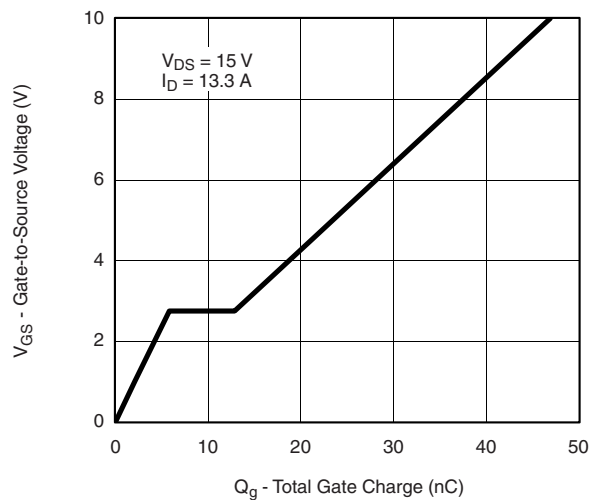
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



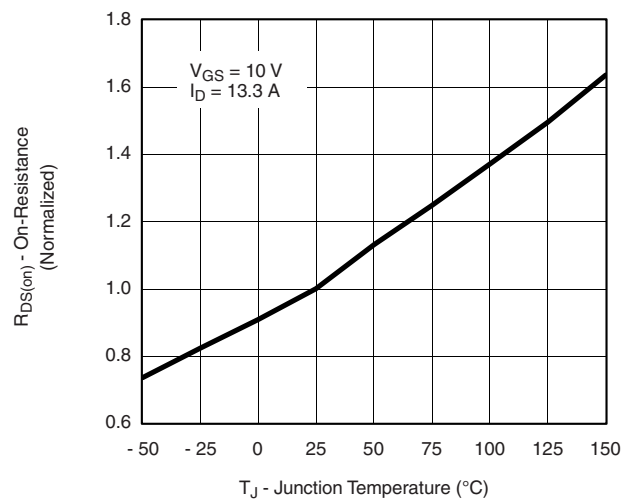
On-Resistance vs. Drain Current



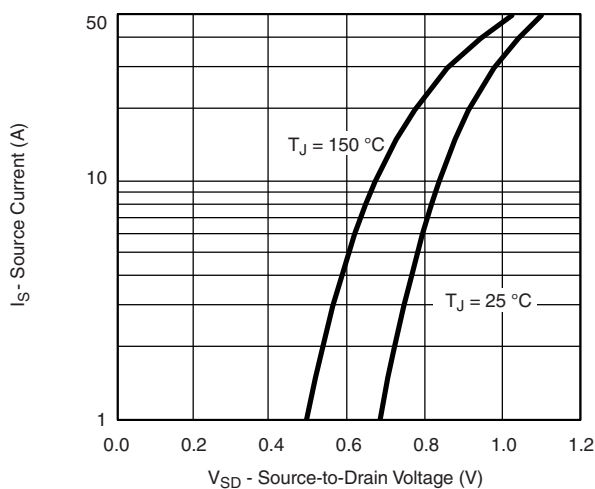
Capacitance



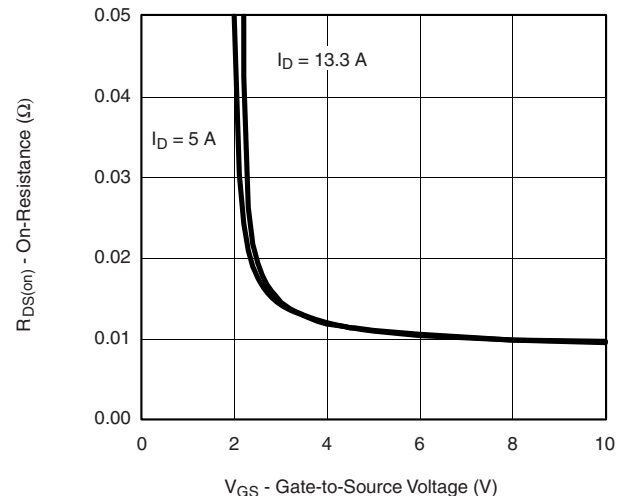
Gate Charge



On-Resistance vs. Junction Temperature

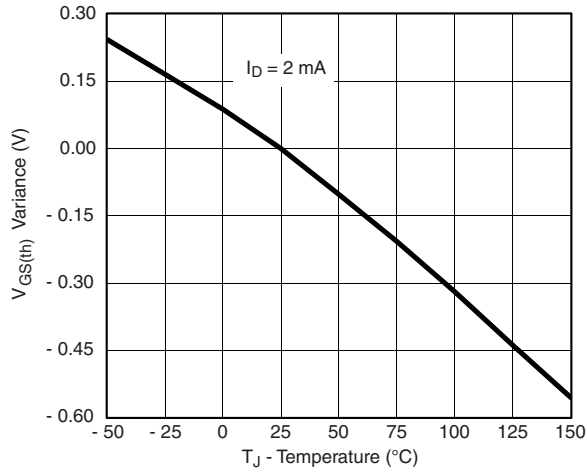


Source-Drain Diode Forward Voltage

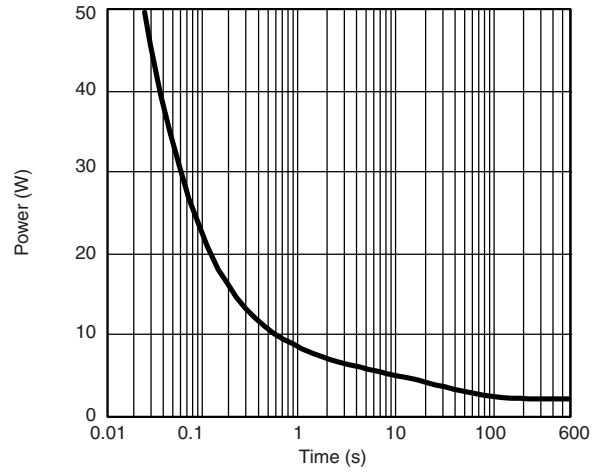


On-Resistance vs. Gate-to-Source Voltage

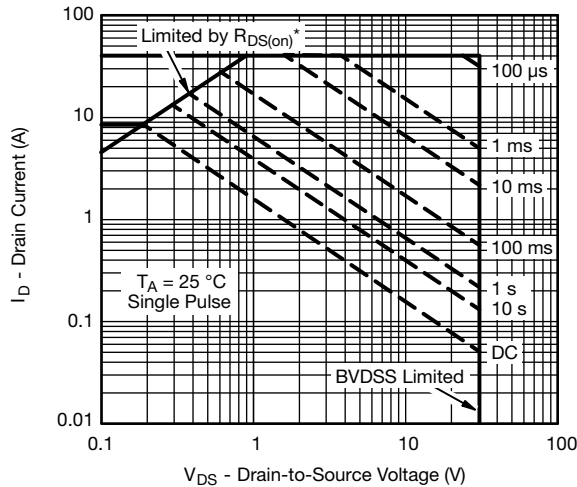
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Threshold Voltage

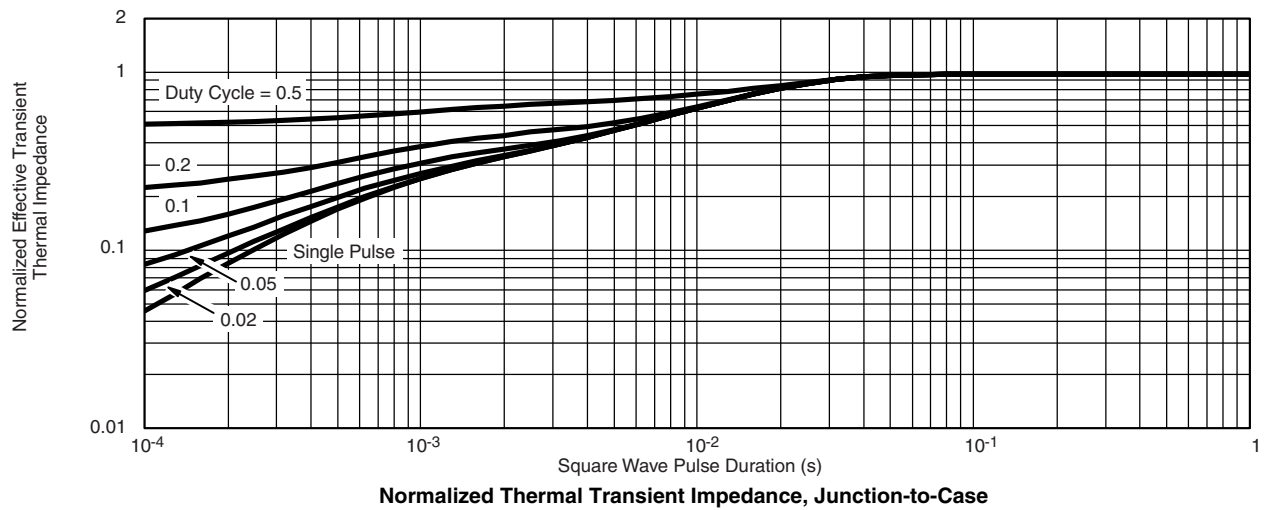
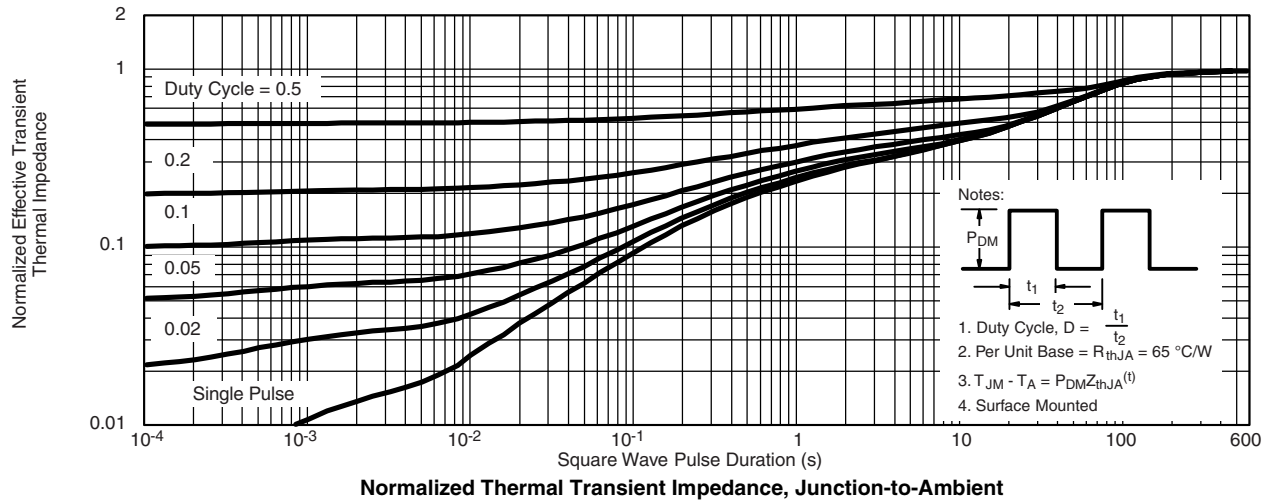


Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



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