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Vishay Siliconix

Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)		
30	0.022 at V _{GS} = 10 V	10		
	0.030 at V _{GS} = 4.5 V	8.5		

SCHOTTKY PRODUCT SUMMARY						
V _{DS} (V)	V _{SD} (V) Diode Forward Voltage	I _F (A)				
30	0.50 V at 1.0 A	3.0				

PowerPAK SO-8

6.15 mm

FEATURES

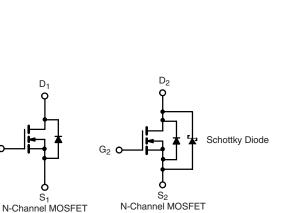
- Halogen-free According to IEC 61249-2-21
 Available
- LITTLE FOOT[®] Plus Schottky
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_a Tested

APPLICATIONS

• Bus and Logic DC-DC



FREE Available



Bottom View

Ordering Information: Si7842DP-T1-E3 (Lead (Pb)-free) Si7842DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

15 mm

Parameter	Symbol	10 s Steady Stat		Unit		
Drain-Source Voltage		V _{DS}	30		V	
Gate-Source Voltage		V _{GS}	± 20			
Continuous Droin Current (T 150 °C)a	T _A = 25 °C	1-	10	6.3		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	^I D	6.0	5.0		
Pulsed Drain Current		I _{DM}	30		A	
Continuous Source Current (Diode Conduction) ^a		ا _S	2.9	1.1		
Mauina Davia Diasia atiang	T _A = 25 °C	P _D	3.5	1.4	w	
Maximum Power Dissipation ^a	T _A = 70 °C	'D	2.2	0.9	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b,c}			260			

THERMAL RESISTANCE RATINGS

Parameter		barameter			MOSFET		Schottky		
Falanetei		Symbol	Typical	Maximum	Typical Maximum		Unit		
Maximum hungting to Anghingta	t ≤ 10 s	R _{thJA}	26	35	26	35			
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	60	85	60	85	°C/W		
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	3.9	5.5	3.9	5.5			

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

Vishay Siliconix



Parameter	Symbol	Test Condition		Min.	Typ. ^b	Max.	Unit
Static	<u> </u>						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$		0.8		2.4	V
Gate-Body Leakage	I _{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V				± 100	nA
		$V_{DS} = 30 V. V_{CS} = 0 V$	Ch-1			1	
Zero Gate Voltage Drain Current	I _{DSS}		Ch-2			100	
Zero Gale Vollage Dialit Current	USS	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 85 °C	Ch-1			15	μΑ
		VDS = 00 V, VGS = 0 V, VJ = 00 O	Ch-2			2000	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$		20			Α
	Б	V _{GS} = 10 V, I _D = 7.5 A			0.018	0.022	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 6.5 \text{ A}$		0.024	0.030		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 7.5 A			22		S
_	V _{SD}	$l_{s} = 1 A. V_{Gs} = 0 V$	Ch-1		0.8	1.2	
Diode Forward Voltage ^a			Ch-2		0.47	0.5	V
Dynamic ^b							
Total Gate Charge	Qg				13	20	
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 7.5 \text{ V}$	λ		2		nC
Gate-Drain Charge	Q _{gd}				2.7		
Gate Resistance	Rg			0.5	1.2	3.2	Ω
Turn-On Delay Time	t _{d(on)}				8	16	
Rise Time	t _r	$V_{DD} = 15 \text{ V, } \text{R}_{\text{L}} = 15 \Omega$ $\text{I}_{\text{D}} \cong 1 \text{ A, } \text{V}_{\text{GEN}} = 10 \text{ V, } \text{R}_{\text{g}} = 6 \Omega$			10	20	
Turn-Off Delay Time	t _{d(off)}				21	40	nc
Fall Time	t _f				10	20	ns
Source-Drain Reverse Recovery	+	L = 1.7 A dl/dt = 100 A/ma	Ch-1		40	80	
Time	t_{rr} $I_F = 1.7 \text{ A}, \text{ dl/dt} = 100 \text{ A/}\mu\text{s}$	Ch-2		32	70		

Notes: a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.

SCHOTTKY SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted								
Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit		
Forward Voltage Drop	V _F	I _F = 1.0 A		0.47	0.50	V		
		I _F = 1.0 A, T _J = 125 °C		0.36	0.42			
Maximum Reverse Leakage Current	I _{rm}	V _r = 30 V		0.004	0.100	mA		
		$V_r = 30 \text{ V}, \text{ T}_J = 100 ^\circ\text{C}$		0.7	10			
		$V_r = -30 \text{ V}, \text{ T}_J = 125 ^\circ\text{C}$		3.0	20			
Junction Capacitance	CT	V _r = 10 V		50		pF		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



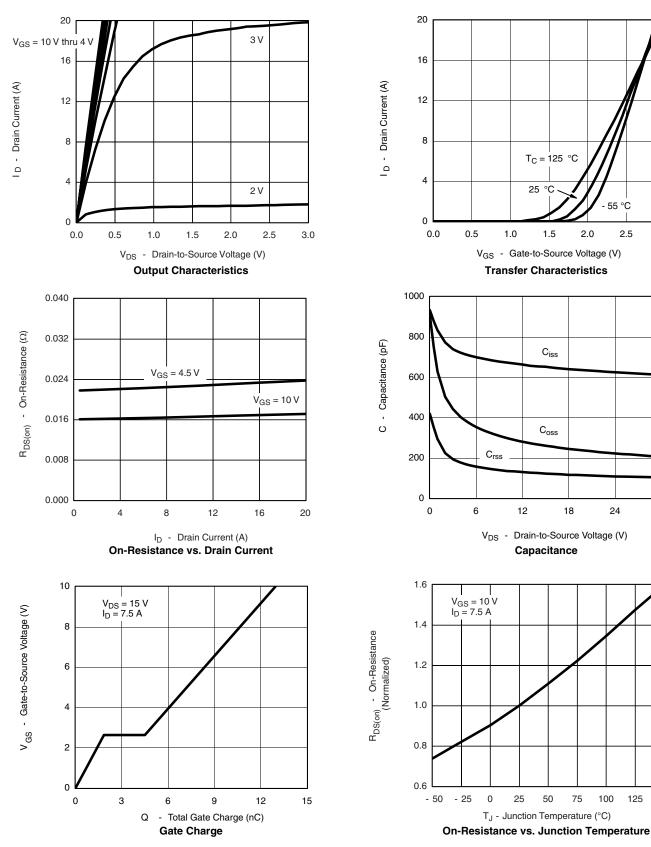
Si7842DP

3.0

30

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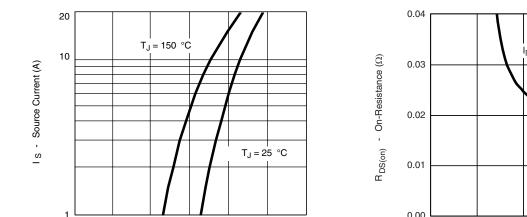
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



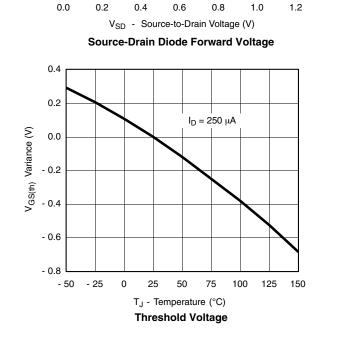
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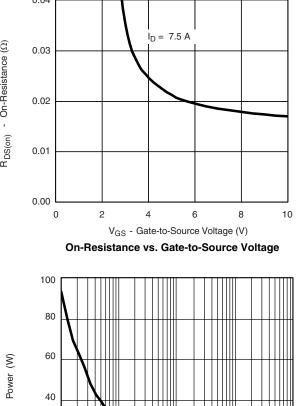
Si7842DP

Vishay Siliconix

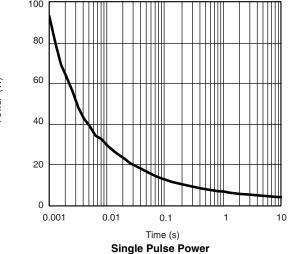


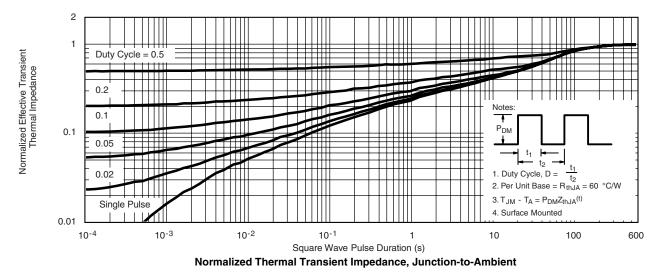
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

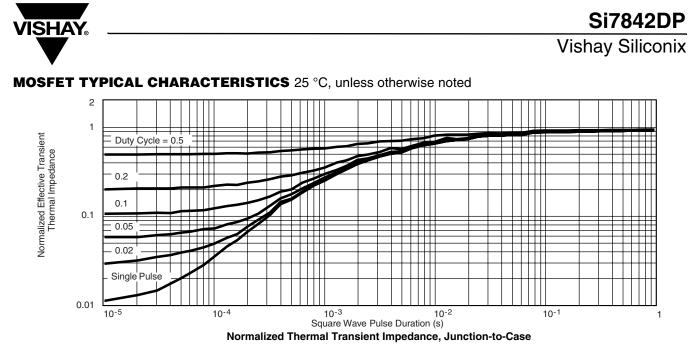




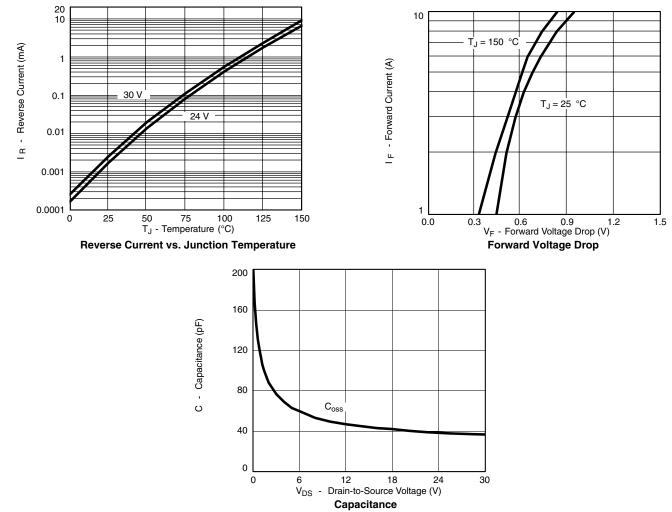
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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?71617</u>.



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