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Dual N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
20	0.030 at V _{GS} = 4.5 V	7.7		
	0.036 at V _{GS} = 2.5 V	7.0		
	0.045 at V _{GS} = 1.8 V	6.3		

FEATURES

- Halogen-free Option Available
- TrenchFET[®] Power MOSFETS: 1.8 V Rated
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile

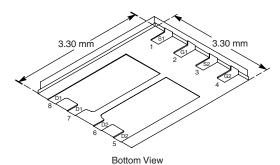


RoHS

APPLICATIONS

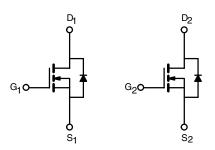
· HDD Spindle Drive

PowerPAK 1212-8



Ordering Information: Si7904DN-T1-E3 (Lead (Pb)-free)

Si7904DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

N-Channel MOSFET

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current /T 150 °C)a	T _A = 25 °C	- I _D	7.7	5.3	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 85 °C		5.5	3.8	
Pulsed Drain Current		I _{DM}	20		Α
Continuous Source Current (Diode Conduction) ^a		I _S	2.3	1.1	
Single Pulse Avalanche Current		I _{AS}	15		
Avalanche Energy	L = 0.1 mH	E _{AS}	11		mJ
Maniana Barra Biasinatian	T _A = 25 °C	D	2.8	1.3	W
Maximum Power Dissipation ^a	T _A = 85 °C	P _D	1.5	0.85	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations ^{b,c}		J	260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Manipular Landing to Audit 18	t ≤ 10 s	- R _{thJA}	35	44	°C/W	
Maximum Junction-to-Ambient ^a	Steady State		75	94		
Maximum Junction-to-Case	Steady State	R _{th,IC}	4	5]	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

Vishay Siliconix



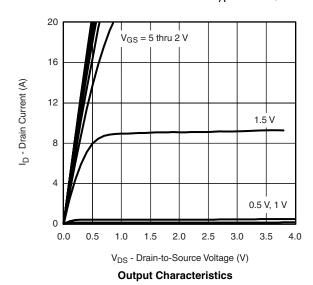
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					•		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 935 \mu\text{A}$	0.45		1.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current		V _{DS} = 20 V, V _{GS} = 0 V			1		
	IDSS	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			Α	
Drain-Source On-State Resistance ^a		$V_{GS} = 4.5 \text{ V}, I_D = 7.7 \text{ A}$		0.025	0.030	Ω	
	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 7.0 \text{ A}$		0.030	0.036		
		$V_{GS} = 1.8 \text{ V}, I_D = 1 \text{ A}$		0.037	0.045		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 7.7 A		23		S	
Diode Forward Voltage ^a	V _{SD}	I _S = 2.3 A, V _{GS} = 0 V		0.70	1.2	V	
Dynamic ^b	1 1		1	'		•	
Total Gate Charge	Qg			10.2	15		
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 7.7 \text{ A}$		1.3		nC	
Gate-Drain Charge	Q_{gd}			2.4			
Turn-On Delay Time	t _{d(on)}			15	23		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_{L} = 10 \Omega$		50	75		
Turn-Off DelayTime	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		60	90	ns	
Fall Time	t _f			45	68	1	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.3 A, dI/dt = 100 A/μs		40	80	1	

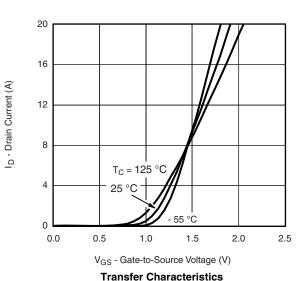
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25 \, ^{\circ}\text{C}$, unless otherwise noted



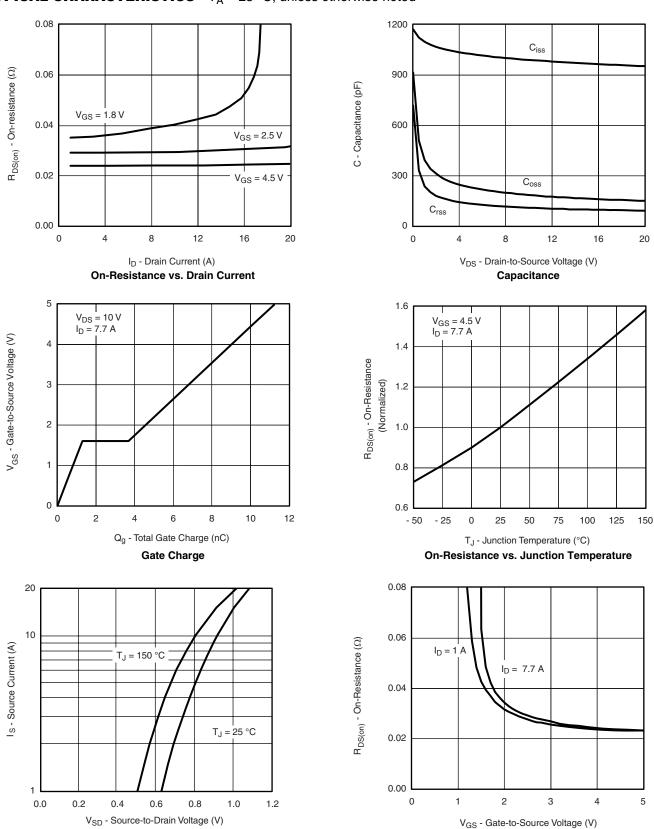








TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



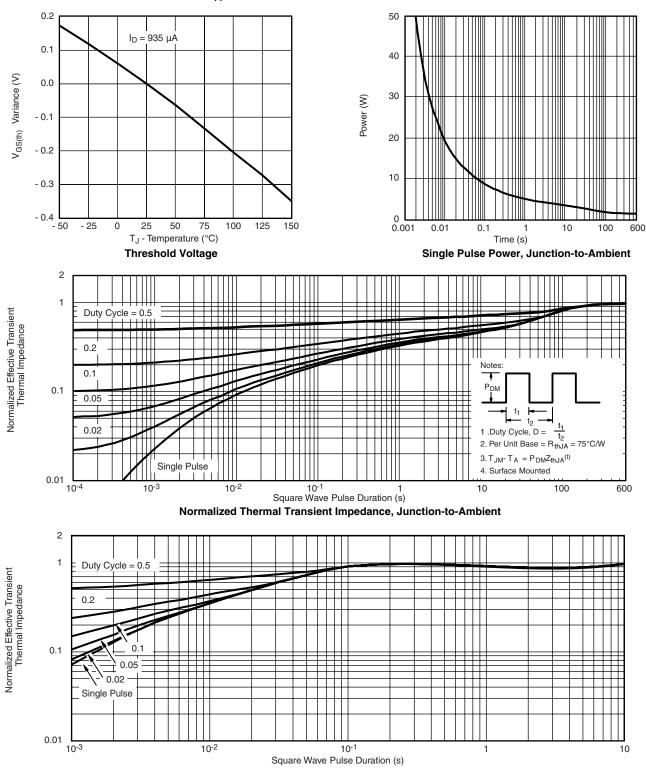
Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Vishay Siliconix

VISHAY

TYPICAL CHARACTERISTICS $T_A = 25 \, ^{\circ}C$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71643.



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